WAVETEK

MAINTENANCE MANUAL

Model 95

20 MHz Synthesized
Arb/Function Waveform

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20 MHz Synthesized Arb/Function Waveform

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SAFETY FIRST

Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wire carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adapters.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⊥).
- Don't hold your eyes extremely close to an RF output for a long time. The normally nonhazardous low-power RF energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

WARNING

This instrument normally contains a lithium battery. Where lithium is prohibited, such as aboard U.S. Navy ships, verify that the lithium battery has been removed.

Do not recharge, short circuit, disassemble, or apply heat to the lithium battery. Violating this rule could release potentially harmful lithium. Observe polarity when you replace the battery.

SECTION 1
HOW TO USE THIS MANUAL

1.1. INTRODUCTION

This manual contains information on the testing, calibration, and servicing of the Wavetek Model 95, 20 MHz Synthesized Arbitrary Function Generator.

1.2 WHAT IS IN THIS MANUAL

This manual contains the following sections:

Section 2 Routine Preventive Maintenance.
Section 3 Verification Procedure.
Section 4 Calibration Procedure.
Section 5 Circuit Description.
Section 6 Maintenance (Troubleshooting).
Section 7 The Drawing Package.
Appendix A. Product Description and Specification

1.3 HOW TO USE THIS MANUAL

The purpose of the maintenance manual is to support the technician in keeping the Model 95 functioning correctly. The material in this manual is organized in such a way as to aid the service technician in identifying and isolating a problem with the unit.

Spare And Replacement Parts

Users who plan on servicing the Model 95 may choose to order spare parts from Wavetek. Each assembly contains a parts list; see the drawing package, section 7. All parts listed may be ordered directly from Wavetek. In addition, a recommend spare parts package (Wavetek part number: 1200-00-3463) can be ordered from Wavetek.

Suspected Malfunctions

If the Model 95 does not operate correctly, check the instrument setup before trying to isolate the problem; see the *Model 95 Operator's Manual.* Or, perform an Autocal on the unit to see if the instrument will correct the problem itself; see section 4 of this manual. If there is a problem, performing Autocal causes the unit to return an error message.

If the problem is known, turn to the appropriate section and correct the fault. Use the Calibration procedure, section 4, when the Model 95 appears out of calibration. Also, the Model 95 provides error messages which can guide the technician to circuit blocks within the instrument; see section 6. Use the maintenance section, section 6, to isolate failures. Section 6 does not isolate problems down to the component level, but only to the circuit block. In addition to the Maintenance section, the Circuit Description, schematics, and assembly drawings all support problem isolation.

1.4 THE OPERATOR'S MANUAL

This manual does not cover the operation of the Model 95. The *Model 95 Operator's Manual* contains that information.

Product description and specifications - Section 1.
Routine Maintenance - Section 2.
Operation which includes both front panel and remote (GPIB) - Section 3.

SECTION 2
ROUTINE MAINTENANCE

This section covers routine tasks the Service Technician may perform on the Model 95.

2.1 CALIBRATION

Section 4 of this manual contains both the Autocal and Calibration Procedure instructions.

Autocal (automatic calibration) provides a quick method of calibrating the Model 95 without the use of external test equipment. Autocal automatically sets up the instrument and takes internal measurements using internal standards. The Model 95 calculates correction values and stores those values in memory. The Model 95 recalls and loads these correction values at power up. Use Autocal when Model 95 accuracy is critical, after long term instrument storage, or following drastic changes in the environment. Also, perform Autocal at anytime the Service Technician believes it is necessary. Performing Autocal will not erase the Arb active RAM.

The Calibration Procedure provides a more extensive method of Model 95 calibration. The Calibration Procedure uses external test equipment and requires opening the instrument for adjustments. Use the Calibration Procedure when the Model 95 displays "CAL REQUIRED" or "FAILED AUTO CAL", after repair, Performance Verification procedure (section 3) failure, or at routine scheduled calibration. Performing the Calibration Procedure erases the contents of the Model 95's Arb active memory.

2.2 FUSE REPLACEMENT

To replace the Model 95's fuse (rear panel) use the following instructions.

1. Disconnect the power cord at the instrument. Open the fuse holder cover door. Rotate the fuse-pull to the left to remove the fuse.

2. Replace the fuse with one having the same current and voltage ratings. The following table lists fuses used with different voltage ranges. Rotate the fuse pull lever back into the normal position. Insert the correct fuse in the fuse holder. Close the fuse holder cover door.

Card Position	**Input Vac**	**Fuse**
100	90 to 105	1A, 250 Vac, Slo Blo
120	108 to 126	1A, 250 Vac, Slo Blo
220	198 to 231	1/2A, 250 Vac, Slo Blo
240	216 to 252	1/2A, 250 Vac, Slo Blo

3. Connect the AC line cord to the mating connector at the rear of the unit and power source.

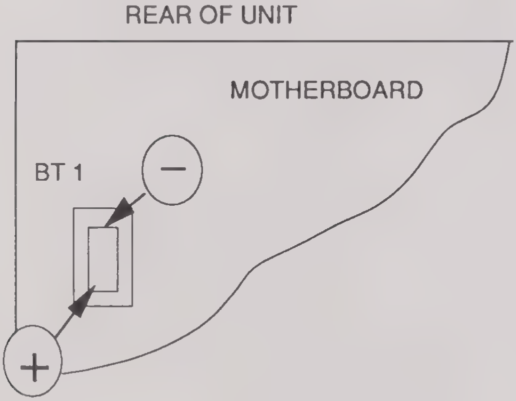
2.3 BATTERY REPLACEMENT

The Model 95 contains a Lithium battery (Panasonic BR-2/3A or equivalent) to power the unit's memory when power is off. This battery life is typically greater than three years. At power on, the Model 95 checks the battery's condition as part of the power-on Self-test. If Self-test detects a low battery, the display shows "LOW BAT X.XXXV". Replace the battery otherwise the contents of the memory could be lost when power is turned off.

To replace the battery,

1. Remove the top cover and shield. Remove the four screws in the top and the one screw at the rear of the cover. Slide the cover back.

2. With the power ON, replace the old battery, as shown in the following illustration, with a new battery. Observe the polarity of the battery when installing it. If the power is turned off while replacing the battery, all contents of the RAM will be lost.



3. Replace the top cover and shield. Secure them using the four screws in the top and the one screw in the rear of the cover.

2.4 FAN MAINTENANCE

The Model 95's fan contains a filter which should be cleaned about every month. Clean the filter more often if the unit is used in a dusty environment.

To clean the Filter,

1. Disconnect the Model 95 from the primary power source.
2. Using a screwdriver, gently pry off the Filter's grill.
3. Remove the foam filter.
4. Clean the foam filter using a mild soapy solution. Thoroughly rinse the filter, and allow it to dry.
5. Place the filter back in the unit, and snap in the Filter's grill.
6. Connect the Model 95 to the primary power source.

SECTION 3
VERIFICATION PROCEDURE

3.1 PERFORMANCE VERIFICATION

Performance verification tests the operation of every selectable parameter and input/output connector. Furthermore, it verifies the correct operation within each major specification. Use this procedure after a manual calibration (section 5) to confirm the units accuracy. All data obtained during the performance verification should be permanently recorded for future reference. The Verification Form, located at the end of this section, can be used as a master to generate copies. This procedure assumes the person making the tests has a good working knowledge of the Model 95's operation. For information on Model 95 operation, refer to the Model 95 Operator's Manual.

Required Test Equipment - Table 3-1 lists the test equipment required to perform the performance verification procedure. Always keep test equipment interconnecting cables as short as possible.

Table 3-1. Required Test Equipment

Test Equipment	Recommended Model
Scope	Tektronix 2465 or equivalent.
THD Analyzer	Hewlett Packard 8903B or equivalent.
DMM	Wavetek Model 1062 or equivalent.
Signal Source	Wavetek Model 23 or equivalent.
Counter/Timer	Hewlett Packard 5335A or equivalent.
Phase Meter	Hewlett Packard 3575A or equivalent.
Signal Source (Option 001)	Wavetek Model 178 or equivalent

Frequency Range

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters.

Table 3-2. Model 95 Default Conditions

Key	Condition
Frequency/Sample	1kHz (1ms)
Amplitude	5Vpp (2.5 Vp, 1.768 Vrms, 18 dBm)
Mode	Continuous
Offset	0V
Symmetry	50%
Store	Last location stored
Recall	Last location stored
Phase	0° (0 radians)
Trigger/Lock Source	Internal
Burst Counter	5
Filter	None
Function	Sine
Sweep Mode	Continuous Sweep
Sweep Start	1kHz
Sweep Stop	10 kHz
Time	1s Sweep
Linear/Logarithmic	Linear Sweep
Trigger Frequency	100 Hz
On/Off (Func Out)	Output Off (50Ω indicator flashes)
Select output	50Ω, Unbalanced
Knob	Disabled (ENABLED Indicator off)
Edit	Edit Off (Arb Not Active)

Note: The following keys are not affected by the RESET ALL key:

Arb Store
Calibrate
Address
Start Address
Data
Stop Address
Smooth
Z-Axis
Man trigger
Local
Sync Address
GPIB Address
Arb Reset
Cursors

2. Connect the Model 95 and test equipment as shown in figure 3-1.

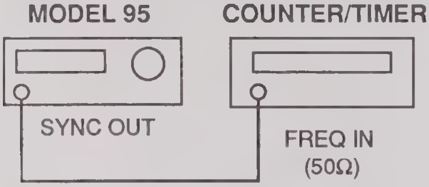


Figure 3-1. Frequency/Symmetry Measurement Setup

3. Program the frequency to the top frequency of each of the top seven decade frequency ranges (Verification Form - Frequency Ranges Synthesized Setting) using the FREQ/SAMP key and knob/keypad. Check the synthesized frequency accuracy per the Specified Value , and record the data on the form.

4. Select Continuous mode (MODE key), and set the frequency using the FREQ/SAMP key and knob/keypad(Verification Form - Unlocked FM Settings). Next, change to the FM mode (MODE key) and measure the frequency. Record the results on the form. Repeat the range measurements for all seven upper frequency ranges.

5. Select Continuous mode (MODE key), and set the frequency using the FREQ/SAMP key and knob/keypad(Verification Form - Unlocked Continuous Settings). Measure the frequency, and record the results on the form. Repeat the range measurements for the three lower frequency ranges.

Frequency Resolution

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters.

2. Connect the Model 95 and test equipment as shown in figure 3-1.

3. Set the Model 95's frequency as listed in the Verification Form - Frequency Resolution Setting using the FREQ/SAMP key and knob/keypad. Check the synthesized frequency accuracy per the Specified Value, and record the data on the form.

Symmetry

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters.

2. Connect the Model 95 and test equipment as shown in figure 3-1.

3. Program the symmetry as listed in the Verification Form - Symmetry Settings using the SHIFT and SYMMETRY keys and knob/keypad. Check the symmetry accuracy per the Specified Value. The specified value represents the time in µs for the the negative half of the cycle. Record the data on the form.

VCG/FM

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters.

2. Connect the Model 95 and test equipment as shown in figure 3-2.

3. Set the signal source for 0 Volts dc output. Set the Model 95 for FM mode (MODE key). Measure the Center Frequency (Verification Form - VCG/FM Setting Cener Frequency) as per the Specified Value (1kHz ± 3% frequency), and record the data on the form.

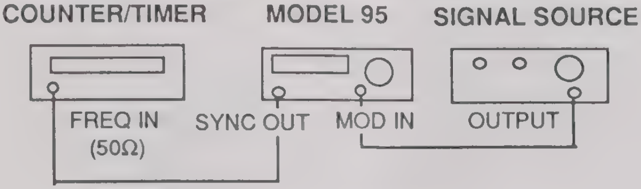


Figure 3-2. VCG/FM Setup

4. Set the signal source for +5 Volts dc output. Measure the Deviation Frequency (Verification Form - VCG/FM Setting Cener Frequency) as per the Specified Value (2kHz±3%), and record the data on the form.

Waveforms

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-3. Connect the Model 95's SYNC OUT to the scope's trigger input.

3. Set the Model 95 to the sine function (FUNCTION key). Verify the scope displays the sine wave (Verification Form - Waveform Setting Sine Wave), and record the results as per the Specified Value (Yes or No) on the form. Repeat this step for the triangle and square waves, as well as dc (Verification Form - Waveform Setting Triangle Wave, Square Wave, and DC).

Arbitrary Waveform and Z-Axis Output

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-3. Connect the Model 95's SYNC OUT to the scope's trigger input. Connect the Z-AXIS output, located on the rear of the Model 95, to the Z-Axis input on the scope.

3. Set the Model 95 to the ARB1 function (FUNCTION key). Press the SHIFT and ARB RESET keys to initialize the active RAM. This will not alter the Arb waveform stored in ARB1. The Arb reset places the start address and left cursor at 0 and the stop address and right cursor at 100.

4. Use the EDIT key to select "BLOCK EDIT +SINE". Select the Z-Axis (Z-AXIS key), and use the knob to step through the Z-Axis settings. Rotate the knob until the scope displays the highlighted cursors. Record the results (Record Yes or No) on the form (Verification Form - Arb Waveform and Z-Axis Output Setting Z-Axis).

5. Press EDIT key to return to the edit display. Press ENTER to place a digitized sine wave between the left and right cursors. Verify the scope displays the digitized sine wave, and record the results on the form (Verification Form - Arb Waveform and Z-Axis Output Setting Digitized Sine Wave).

6. To keep from replacing the waveform stored in ARB1 with the sine wave, select "ARB RESTORE" using the EDIT key.and press ENTER to revert to the original ARB1 waveform.

Sweep

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-3. Connect the Model 95's SYNC OUT to the scope's trigger input.

3. Set the Model 95 to the Sweep Mode (MODE key). Set the Sweep Mode to Continuous Sweep (SWEEP MODE key). Verify the scope displays a sweep output (1kHz to 10 kHz, 1 second sweep), and record the results on the

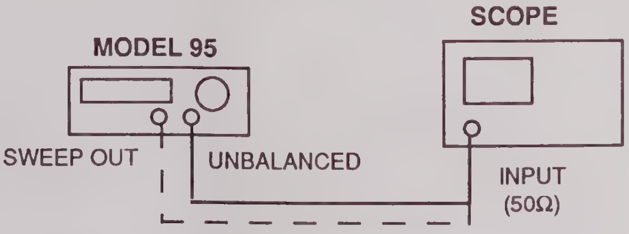


Figure 3-3. Waveforms/Sweep Verification

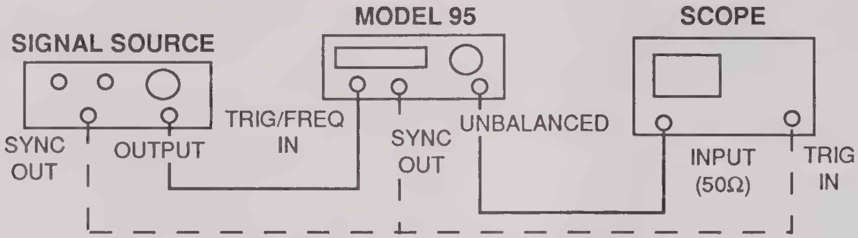


Figure 3-4. Trigger Measurement Setup

form (Verification Form - Sweep Setting Sweep Output).

4. Connect the Sweep Out to the scope input. Verify the scope displays a 1 second sweep ramp (600Ω impedance), and record the results on the form (Verification Form - Sweep Setting Sweep Ramp).

Continuous Mode

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-3. Connect the Model 95's SYNC OUT to the scope's trigger input.

3. Verify the scope displays a continuous 5Vpp sine wave. Record the results (Record Yes of No) on the form (Verification Form - Continuous Mode Setting Continuous 5Vpp Sine).

Triggered Mode

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-4. Connect the Model 95's SYNC OUT to the scope's trigger input.

3. Set the Model 95 to the (Internal) Triggered mode (MODE key). Internal trigger is the default. Verify the scope displays an internally triggered 5Vpp sine wave. Record (Record Yes or No) the results on the form (Verification Form - Triggered Mode Setting Internal Triggered Sine Wave).

4. Set the Model 95 to the External Triggered mode (TRIG/LOCK key). Set the signal source for a 100 Hz TTL square wave. Connect the signal source to the TRIG/FREQ IN connector. Synchronize the scope off the signal source.

5. Verify the scope displays an externally triggered 5Vpp sine wave. Record (Record Yes or No) the results on the form (Verification Form - Triggered Mode Setting External Triggered Sine Wave).

Gated Mode

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-4. Connect the Model 95's SYNC OUT to the scope's trigger input.

3. Set the Model 95 to the (Internal) Gate mode (MODE key). Internal gate is the default. Verify the scope displays an internally gated 5Vpp sine wave. Record (Record Yes or No) results on the form (Verification Form - Gate Mode Setting Internal Gated Sine Wave).

4. Set the Model 95 to the external triggered gate mode (TRIG/LOCK key). Set the signal source for a 100 Hz TTL square wave. Connect the signal source to the TRIG/FREQ IN connector. Synchronize the scope off the signal source.

5 Verify the scope displays an externally gated 5Vpp sine wave. Record (Record Yes or No) the results on the form (Verification Form - Gate Mode Setting External Gated Sine Wave)..

Burst Mode

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of

default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-4. Connect the Model 95's SYNC OUT to the scope's trigger input.

3. Set the Model 95 to the (Internal) Burst mode (MODE key). Internal burst is the default. Verify the scope displays an internal triggered burst of 5, 5Vpp sine waves. Record (Record Yes or No) the results on the form (Verification Form - Burst Mode Setting Internal Burst Sine Wave).

4. Set the Model 95 to the external triggered burst mode (TRIG/LOCK key). Set the signal source for a 100 Hz TTL square wave. Connect the signal source to the TRIG/FREQ IN connector. Synchronize the scope off the signal source.

5. Verify the scope displays an externally triggered burst of 5, 5Vpp sine waves. Record (Record yes or No) the results on the form (Verification Form - Burst Mode Setting External Gated Sine Wave).

Square Wave/Sync Out Transition Time

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-3. The Unbalanced Output must be terminated into a 50Ω feed-thru termination.

3. Set the Model 95 for 10 MHz square wave (FREQ/SAMP key and FUNCTION key). Measure rise time, fall time, positive-going transition peak-to-peak aberration in percent and negative-going transition peak-to-peak aberration in percent. Check the transition time and aberration as per the Specified Values, and record the results on the form (Verification Form - Square Wave/Sync Out Transition Time Unbalaced Output Setting Rise Time, Fall Time, Positive Transition % aberration, and Negative Transition Time % aberation).

4. Connect the Sync Out to the scope, and measure the peak-to-peak amplitude, rise time and fall time. Check the transition time as per the Specified Values, and record the results on the form (Verification Form - Square Wave/Sync Out Transition Time Sync Out Setting Rise Time and Fall Time).

Outputs

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-3.

3. Set the Model 95 for 50Ω, 75Ω and 600Ω output impedance (SHIFT and SELECT key). The Unbalanced Output must be terminated into a matching feed-thru termination. Verify the scope displays the normal waveform and amplitude into matching terminations (Verification Form - Outputs Unbalanced Output Setting 50Ω, 75Ω, and 600Ω). Record (Record Yes or No) the results on the form.

4. Connect the Model 95 and test equipment as shown in figure 3-5.

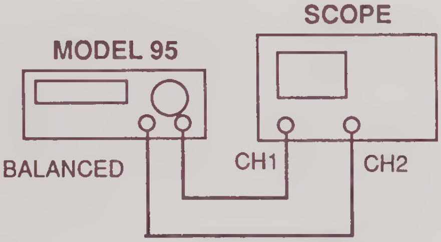


Figure 3-5. Balanced Output Setup

5. Synchronize the scope off channel 1. Place a 135Ω load resistor across the Balanced Output terminals. Select the Model 95's 135Ω Balanced Output (SHIFT and SELECT keys). Verify the scope displays on channel 1 and 2, two sine waves 180° out of phase. The amplitude of each sine wave will be one half of the Unbalanced Out sine wave (step 3). Record (Record Yes or No) the results on the form (Verification Form - Outputs Balanced Output Setting 135Ω).

6. Select the Balanced 600Ω Output. Place a 600Ω load resistor across the Balanced Output. Verify the scope displays on channel 1 and 2, two sine waves 180° out of phase. The

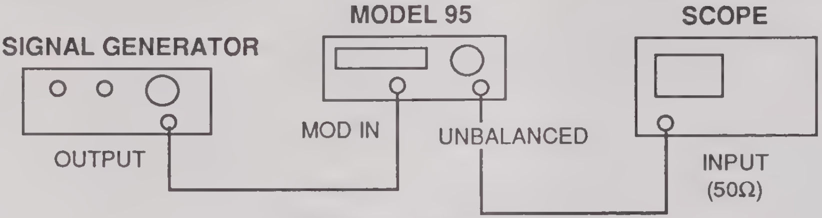


Figure 3-6. AM Setup

amplitude of each sine wave will be one half of the Unbalanced Out sine wave (step 3). Record (Record Yes or No) the results on the form (Verification Form - Outputs Balanced Output Setting 135Ω).

Amplitude Modulation

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-6.

3. Set the signal generator for a 1kHz, 2.7 Vpp (open circuit) sine wave. Set Model 95 for 100 kHz (FREQ/SAMP key and knob/keypad) and the AM mode (MODE key). Verify the scope displays normal amplitude modulation of approximately 100%. Record (Record Yes or No) the results on the form (Verification Form - Amplitude Modulation Setting 100% AM).

Suppressed Carrier

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-6.

3. Set Model 95 to the SCM mode (MODE key). With the MOD IN signal disconnected, verify the scope displays no output. Record the results on the form.

4. Set the signal source for +2Vdc. Connect the signal source output to the Model 95's MOD IN. Verify the scope displays a 4Vpp sine wave. Record (Record Yes or No) the results on the form (Verification Form - Suppressed Carrier Modulation Setting 4Vpp SCM).

Sine Wave Purity

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-7.

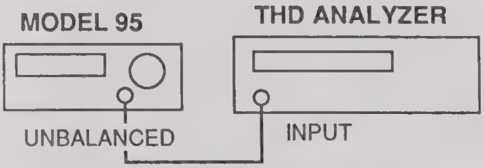


Figure 3-7. Sine Purity Setup

3. Measure the sine total harmonic distortion in dB. Measure the sine wave purity, and Record the results on the form (Verification Form - Sine Wave Purity Setting THD at 1kHz).

Amplitude Accuracy

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-8.

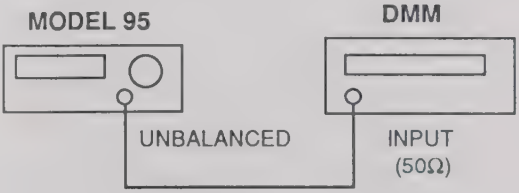


Figure 3-8. Amplitude Accuracy Setup

3. Set the amplitude as listed in the Verification Form - Amplitude Accuracy Sine Wave Setting using the AMPLITUDE key and knob/keypad. Measure the amplitude accuracy per the Specified Value, and record the data on the form.

4. Set the Model 95's function to Triangle wave (FUNCTION key). Set the amplitude as listed in the Verification Form - Amplitude Accuracy Triangle Wave Setting using the AMPLITUDE key and knob/keypad. Measure the amplitude accuracy per the Specified Value, and record the data on the form.

5. Set the Model 95's function to Square wave (FUNCTION key). Set the amplitude as listed in the Verification Form - Amplitude Accuracy Square Wave Setting using the AMPLITUDE key and knob/keypad. Measure the amplitude accuracy per the Specified Value, and record the data on the form.

DC Output and Attenuator Accuracy

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-8.

3. Set the Model 95 to the DC function (FUNCTION key), and program the dc offset (OFFSET key and keypad/knob) as listed in the Verification Form - DC Output Setting. Measure the dc offset accuracy as per the Specified Value. Record the data on the form.

External Lock

1. Initialize the Model 95 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 95 and test equipment as shown in figure 3-9, except leave the signal source disconnected.

3. Set the Model 95 to external lock (TRG/LOCK SOURCE key). Verify the Model 95 displays EXTLOC, the UNLOCK indicator flashes, and EXT indicator remains lit. Record (Record Yes or No) the results on the form (Verification Form - External Lock Setting Source Disconnected).

4. Set the signal source for a 10 kHz, 5Vpp sine wave. Connect the signal source to the Model 95's TRIG/FREQ IN connector. Verify the Model 95 displays EXTLOC 10.00 KHZ (approximate reading), UNLOCK indicator remains off, and the EXT indicator remain lit. Record (Record Yes or No) the results on the form (Verification Form - External Lock Setting Source Connected). The Model 95 automatically changes its frequency to match the frequency of the external source.

5. Set the Model 95 phase shift as listed in Verification Form - External Lock Phase Shift Setting. Measure the phase angle as per the Specificed Value, and record results on the form.

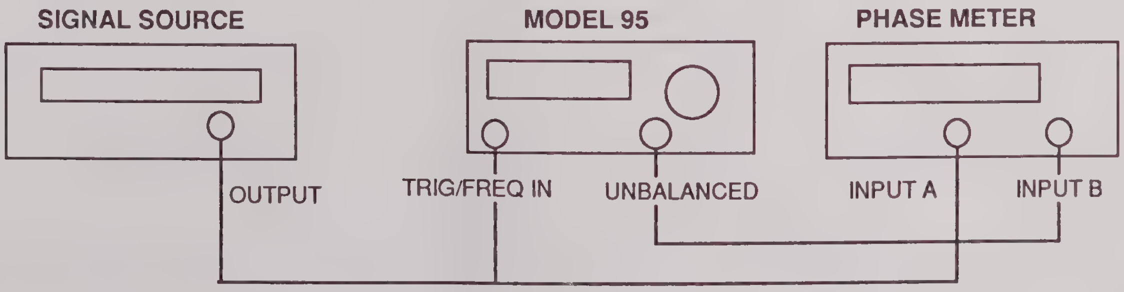


Figure 3-9. External Lock Measurement

Front Panel

Did the annunciators and the display perform correctly during the Verification Procedure. If so, record the results on the form.

Option 001 - High Frequency Stability Reference

Perform the following checks only if the Model 95 contains an Option 001.

1. Turn the Model 95s Power on.

2. Connect the Model 95's REF OUT, located on the rear panel, to a Counter/Timer.

3. Verify the REF OUT frequency (TCXO freq) measures within the Specified Value on the Verification Form. Record the results on the form.

4. Connect the Model 95's REF IN, located on the rear panel, to a signal source. Set the signal source (178 Freq) to 10.001 MHz, 1Vrms sine wave (always properly terminate the signal source). Measure the REF OUT frequency (Ref Out) as per the Specified Value, and record the results on the form.

Parameter	**Low Limit**	**High Limit**
TCXO Freq	9,999,990 Hz	10,000,010 Hz
178 Freq	10,000,000 Hz	10,002,000 Hz
Ref Out	178 Freq - 2 Hz	178 Freq + 2 Hz

SECTION 4
CALIBRATION PROCEDURE

4.1 CALIBRATION

Wavetek maintains a factory Customer Service department for those customers not possessing the necessary personnel or test equipment to calibrate or repair the instrument. Before returning the instrument, contact the Customer Service Department by calling or writing:

Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
TWX: (910) 335-2007
FAX (619) 565-9558

The Model 95 provides the user with two calibration methods: Autocal and Calibrate.

4.1.1 Autocal

Autocal (automatic calibration) provides a quick method of calibrating the Model 95 without using external test equipment. Autocal automatically sets up the instrument and takes internal measurements using internal standards. The Model 95 calculates correction values and stores those values in memory. These correction values are recalled from memory when the unit is powered up. Use Autocal when Model 95 accuracy is critical, after long term instrument storage, following drastic changes in the environment, or when the operator believes Autocal is necessary.

4.1.2. Calibration Procedure

The Calibration Procedure provides a more extensive method of calibration. The Calibration Procedure uses external test equipment and requires opening the instrument and making adjustments. Use the Calibration Procedure when the Model 95 displays "CAL REQUIRED" or "FAILED AUTOCAL", when the Model 95 has been repaired, fails the Performance Verification procedure (Section 3), or when routine calibration is scheduled. Paragraph 4.3 describes the Calibrate procedure. The adjustment values given in the calibration procedure are not necessarily the specified values. This calibration procedure will erase the contents of the Arb active memory.

4.2 AUTOCAL PROCEDURE

To Autocal the Model 95, perform the following steps. Autocal requires no external test equipment. In fact, no test equipment should be connected to the Model 95's input connectors, otherwise the Autocal circuitry could alter the calibration of the instrument. Also, disconnect all outputs from the instrument otherwise the sudden changes in the instrument's output waveforms could damage external equipment.

1. Turn on the Model 95 and allow it to warm up for 20 minutes. Pressing the CaliBRATE key during the 20 minute warm up time displays the count-down time, after the 20 minutes the Model 95 begins Autocal. Pressing any other key during the count down aborts Autocal and returns the instrument to normal operation.

   Remember to remove all input and output connections to the Model 95 before pressing Autocal.

2. After a 20 minute warm up, press the CalIBRATE key (SHIFT and CALIBRATE) and allow the unit time to complete the Autocal cycle. While running AutoCal,the Model 95 displays "CALIBRATING". When completed successfully, the Model 95 displays "AUTOCALIBRATED". Then the unit returns to its last operational setup. If the Autocal fails, the Model 95 displays an error message which identifies the parameter - ERR (*Keyword*); for example ERR VSINCAL. If this occurs occasionally, try to Calibrate the unit again. Note the error keywords and report the errors when the unit is returned for scheduled maintenance. Refer to paragraph 6.7.6 for a listing of error messages.

4.3 CALIBRATION PROCEDURE

The Model 95 Calibration Procedure contains a series of steps which the Model 95 will guide you through. During this procedure, the Model 95 automatically sets itself to the right conditions. Some calibration steps may require you to make changes using front panel controls.

CAUTION

Performing the Calibrate Procedure will erase the contents of the active Arb memory. To store the Arb waveform in the Arb waveform memory, refer to paragraph 3.5.20 of the *Model 95 Operator's Manual.*

Table 4-1. Recommended Test Equipment

Test Equipment	Requirements
Scope	Tektronix Model 2465 or equivalent
Distortion Analyzer	Hewlett Packard 8903B or equivalent.
Digital Voltmeter	Wavetek Model 1062 or equivalent.
Function Generator	Wavetek Model 23 or equivalent.
Frequency Counter	Hewlett Packard 5335A or equivalent.
Phase Meter	Hewlett Packard 3575A or equivalent.

NOTE

Use rear panel for all ground connections unless otherwise specified. All indications and waveforms are referenced to chassis ground unless otherwise specified.

Adjustments

Throughout this procedure are illustrations identifying the adjustments used in the steps. For a detailed view of the adjustment locations, refer to the assembly drawings located in section 7 of this manual. Figure 4-1 shows the individual board locations.

Keys

While performing the Calibration Procedure, the following keys perform the following functions.

CALIBRATE	Pressing this key during the Calibration Procedure will turn off the Calibration mode.
RESET	During the Calibration Procedure, this key resets all the calibration factors to their default values.
TRIG FREQ	During the Calibration Procedure, this key functions as the forward cursor. Pressing the TRIG FREQ key advances the procedure to the next calibration step.
MAN TRIG	During the Calibration Procedure, this key functions as the reverse cursor. Pressing the MAN TRIG key backs the procedure up to the previous calibration step.

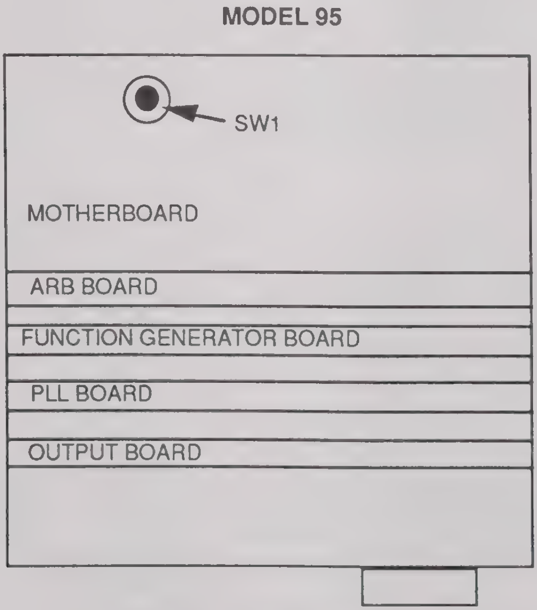


Figure 4-1. Board Locator

KNOB	During the Calibration Procedure, the KNOB is used to change and enter calibration data. It is also used to alternate between two functions in some steps.
KEYPAD	During the Calibration Procedure, the numeric keypad is used to enter calibration data.
ENTER	Use the ENTER key to accept data entered using the numeric keypad.

Calibration Cover

A calibration cover can be used when performing the calibration procedure. This cover replaces the Model 95s normal cover and helps maintain the unit's internal temperature while allowing access to the calibration adjustments. For more information on the calibration cover, contact Wavetek's Customer Service department

Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
TWX: (910) 335-2007
FAX (619) 565-9558

Precalibration Setup

Before beginning calibration, disconnect the Model 95 from its power source and remove five top cover screws. Slide the top cover off, and remove the inner shield. Slide the top cover back on to stabilize the unit's internal temperature.

NOTE

Keep the top cover in place during the procedures except when necessary to make an internal adjustment.

2. Perform the turn-on procedures as described in paragraph 2.4.3 of the *Model 95 Operator's Manual.*

WARNING

Dangerous voltages are present with the covers removed. Where maintenance can be performed without power applied, the power should be removed. Battery voltage is present even with AC power cable removed.

3. Connect the Model 95 to the power source, turn the power on, and allow the unit to warm up for 20 minutes (minimum).

Step 1 Adjust Frequency Reference

If calibrating a standard Model 95 (one without Option 001, TCXO Frequency Reference) perform items 1 through 4 of this step. If Option 001 is installed perform items 1, 5, and 6.

1. After warm up, reset the Model 95 by pressing the Model 95's SHIFT and RESET ALL keys.

2. Connect the test equipment as shown in figure 4-2.

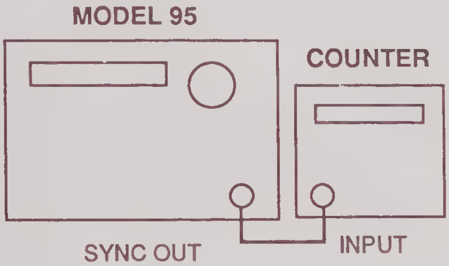


Figure 4-2. Frequency Reference Setup

3. Set up the Model 95 for a 1MHz output by pressing the FREQ/SAMP, 1 EXP 6, and ENTER keys. Press ON/OFF to turn on the output.

4. Measure the frequency at the Sync Out connector. Verify the counter reads 1MHz ±5Hz. If incorrect, slide the cover back, adjust C21 (see figure 4-3) until the counter reads 1MHz ±5Hz, and then slide the cover back on.

If the Option 001, TCXO Frequency Reference is installed, perform item 1 of this step and continue on using the following steps.

5. Connect the counter/timer to the Model 95's REF OUT connector, located on the rear panel.

6. Measure the frequency at the REF OUT connector. Verify the counter reads 10 MHz ±2Hz.

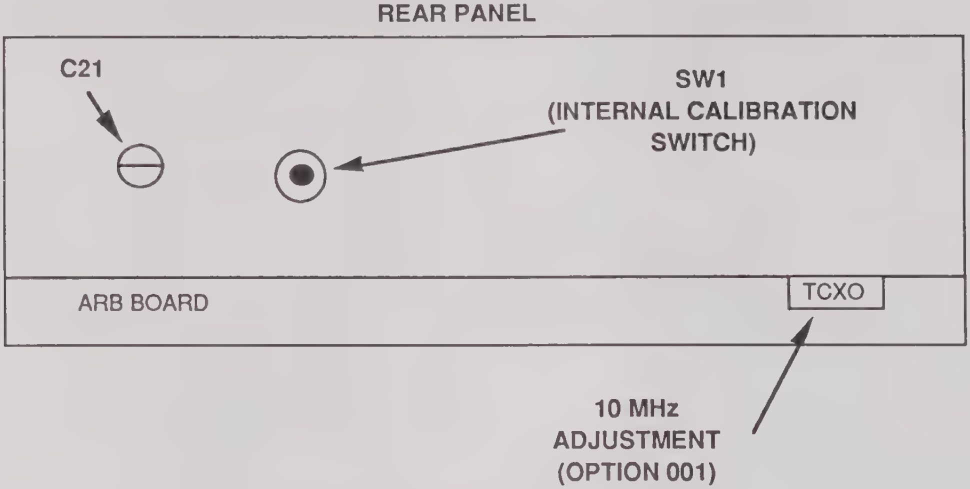

REAR PANEL
C21
SW1 (INTERNAL CALIBRATION SWITCH)
ARB BOARD
TCXO
10 MHz ADJUSTMENT (OPTION 001)

Figure 4-3. Frequency Reference/TCXO Locator

If incorrect, turn off the Model 95 and slide the cover back. Place the Arb board on an extender card. Turn the power back on. Remove the sticker from the TCXO and adjust the trimmer (see figure 4-3) until the counter reads 10 MHz ±2Hz.

When finished, turn off the power, replace the sticker on the TCXO, remove the extender card, and place the Arb board back in the unit. Slide the cover on. Then turn on the power.

Step 2 Initial Steps

1. After the unit is warmed up (20 minutes) slide the top cover back. Press and hold down the internal calibration switch SW1 (figure 4-3) while pressing the SHIFT and CALIBRATE keys. Slide the cover back on.

2. Verify the Model 95 display shows WVTK SN XXXXXXX or WVTK SN 0. XXXXXXXX represent the unit's serial number. If necessary, enter the unit's serial number using the keypad; the unit's serial number is located on the rear panel label. Press the front panel TRIG FREQ key to step to USER SN XXXX. To enter a user serial number, use the keypad.

3. Verify the Model 95 display flashes CALIBRATING and then shows USER SN XXXX or USER SN 0. USER SN allows the calibrator to enter an identification number using the keypad. Press the TRIG FREQ key to advance to R33,97, VSINE XXX. Pressing the TRIG FREQ key also stores the User Number.

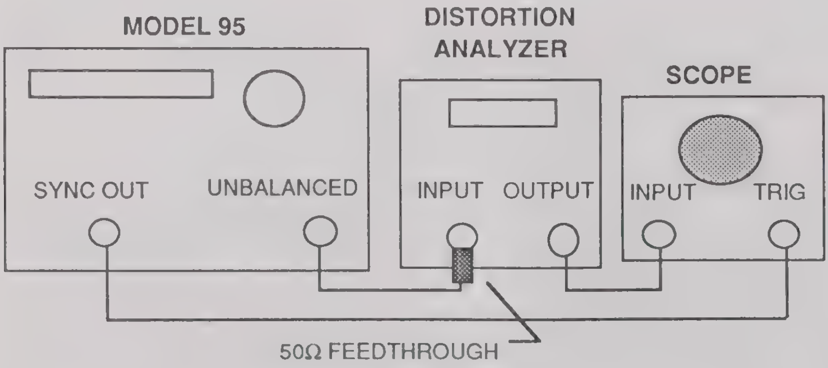

MODEL 95
DISTORTION ANALYZER
SCOPE
SYNC OUT
UNBALANCED
INPUT
OUTPUT
INPUT
TRIG
50Ω FEEDTHROUGH

Figure 4-4. Sine Wave Adjust Setup

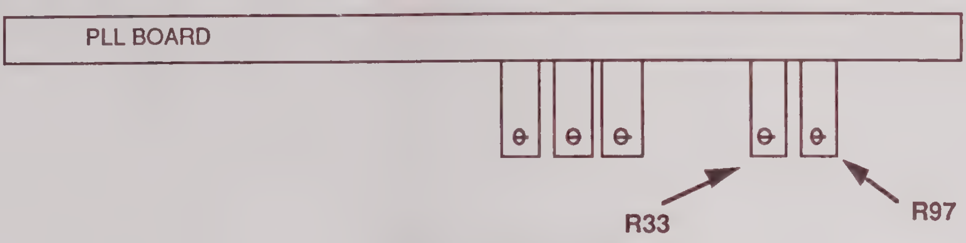


Figure 4-5. R33/R97 Locator

Step 3. Adjust Sine Wave.

1. The Model 95 displays R33, 97, VSINE XXX where XXX represents the internal programmed value of the VSINE dc control voltage. Connect the test equipment as shown in figure 4-4.

2. Set the distortion analyzer controls to display the Model 95 output signal Total Harmonic Distortion (THD) in dB.

3. On the Model 95, slowly adjust the Model 95s front panel Knob for minimum THD as displayed on the scope. Verify that reading is ≤ – 50 dB (approximately 0.32%) at 10 kHz.

4. If the reading is >– 50 dB , set the scope controls to display the distortion analyzer output. Slide the cover back. Adjust R33 (figure 4-5) until waveform peaks are clearly visible in the residue.

   Adjust R97 (figure 4-5) until waveform peaks are symmetrical, one above the average value of the residue signal and one below.

5. Adjust R33 until the peaks disappear back into the residue.

6. Observe the overall ripple in the residue displayed on the scope. Turn the Model 95 Knob CW until the waveform peaks are clearly visible in the residue and repeat step 5.

   If the overall ripple has decreased, continue the procedure always turning the front panel Knob CW.

   If the overall ripple has increased, continue the procedure always turning the front panel Knob CCW.

7. Repeat steps 5 and 6 until:

   The amplitude of the overall ripple in the residue signal is minimum as displayed on the scope. The THD as measured on the distortion analyzer is ≤ – 50 dB.

8. Disconnect the test equipment and slide the cover back on.

9. On the Model 95, press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING and then shows SCM NULL -XXX.

Step 4. SCM Null

1. The Model 95 displays SCM NULL -XXX, where -XXX represent the SCM null value.

2. Connect the test equipment as shown in figure 4-6. Set the scope to 50 mV/div.

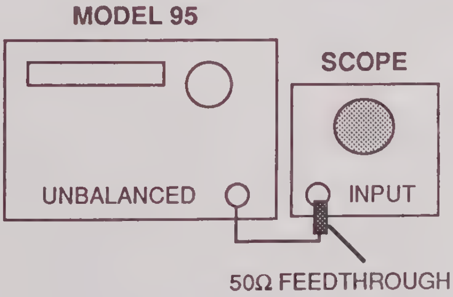


Figure 4-6. SCM Null Setup

3. View the carrier null signal on the scope. If necessary, slide the cover back and adjust R146 (see figure 4-7) to center the display. Then use the Knob to adjust for best square

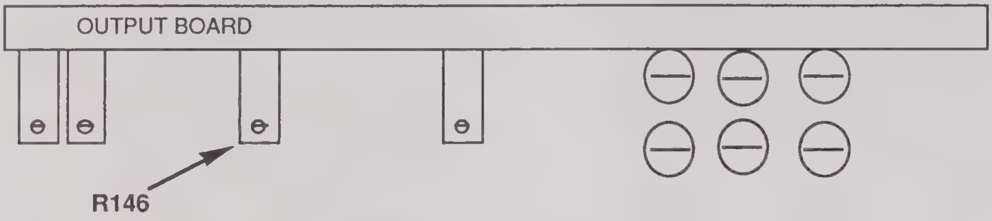


Figure 4-7. R146 Locator

wave signal null. Slide the top cover back on.

4. Press the TRIG FREQ key to step to TRI NULL R25 2.

Step 5 Null Triangle

1. The Model 95 displays TRI NULL R25 2. Connect test equipment as shown in figure 4-8. Set the DVM to measure Vdc.

2. The DVM measures the dc offset value of the 2Vpp triangle.

3. Rotate the Knob on the Model 95 until display shows TRI NULL R25 15. The DVM measures the dc offset value of the 15 Vpp triangle.

4. Use the Knob to move between "2" and "15".

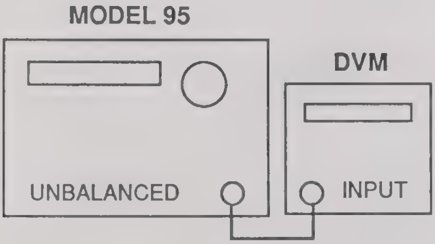


Figure 4-8. Triangle Null Setup

Slide the cover back, and adjust the Output board's R25 (see figure 4-9) until the dc offset change between 2 and 15 is less than 2mV at both amplitudes. Slide the cover back on.

5. Press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING and then shows TRI OFFSET R146.

Step 6 Adjust Triangle Offset

1. The Model 95 displays TRI OFFSET R146. Leave the test equipment connected as shown in figure 4-8.

2. Slide the cover back, and adjust the Output board's R146 (see figure 4-10) until the DVM reads 0Vdc ±2mVdc of triangle offset. Slide the cover back on.

3. Press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING then shows SINE NULL R64.

Step 7 Null Sine Wave

1. The Model 95 displays SINE NULL R64. Leave the test equipment connected as shown in figure 4-8.

2. Slide the cover back, and adjust the PLL board's R64 (see figure 4-11) until the DVM reads 0Vdc ±2mVdc of sine offset. Slide the cover back on.

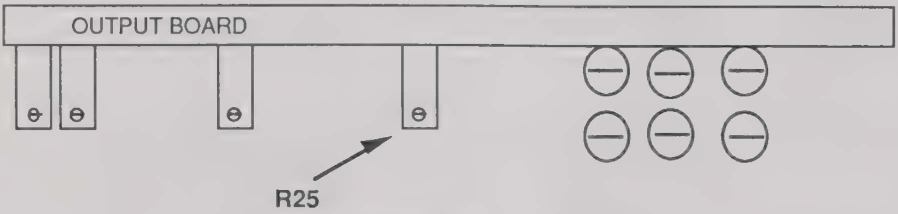


Figure 4-9. R25 Locator

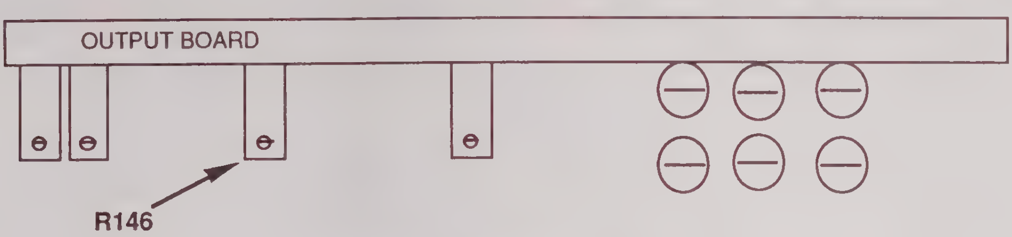


Figure 4-10. R146 Locator

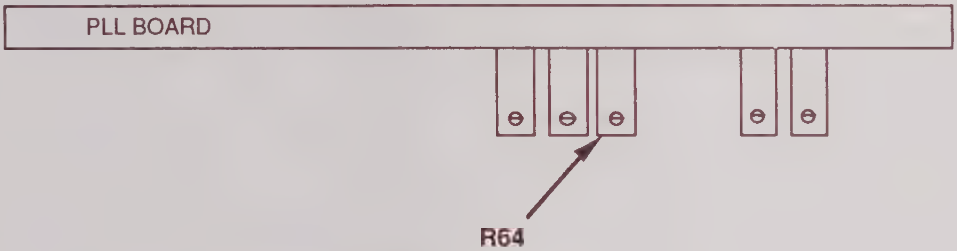


Figure 4-11. R64 Locator

3. On the Model 95, press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING and then shows ARB NULL NF XX.

Step 8 Null Arb - No Filter

1. The Model 95 displays ARB NULL NF XX where XX represent a calibration value. Leave the test equipment connected as shown in figure 4-8.

2. On the Model 95, adjust the Model 95s front panel Knob for 0Vdc ±2mVdc.

3. On the Model 95, press the TRIG FREQ key to advance to the next step. Pressing TRIG FREQ key stores the calibration value in internal memory. Verify the display flashes CALIBRATING then shows ARB NULL 50K XX.

Step 9 Null Arb - 50 kHz Filter

1. The Model 95 displays ARB NULL 50K XX. Leave the test equipment connected as shown in figure 4-8.

2. On the Model 95, adjust the Model 95s front panel Knob for 0Vdc ±2mVdc.

3. On the Model 95, press the TRIG FREQ key to advance to the next step. Pressing TRIG FREQ key stores a correction value in internal memory. Verify the display flashes CALIBRATING then shows ARB NULL 5M XX.

Step 10 Null Arb - 5MHz Filter

1. The Model 95 displays ARB NULL 5M XX where XX represents a calibration value. Leave the test equipment connected as shown in figure 4-8.

2. On the Model 95, adjust the Model 95s front panel Knob for 0Vdc ±2mVdc.

3. On the Model 95, press the TRIG FREQ key to advance to the next step. Pressing TRIG FREQ key stores the calibration value in internal memory. Verify the display flashes CALIBRATING then shows SQUARE 0 R158.

Step 11 Null Square

1. The Model 95 displays SQUARE 0 R158. Leave the test equipment connected as shown in figure 4-8.

2. Slide the cover back, and adjust the Output board's R158 (see figure 4-12) until the DVM reads 0Vdc ±2mVdc of square offset. Slide the cover back on.

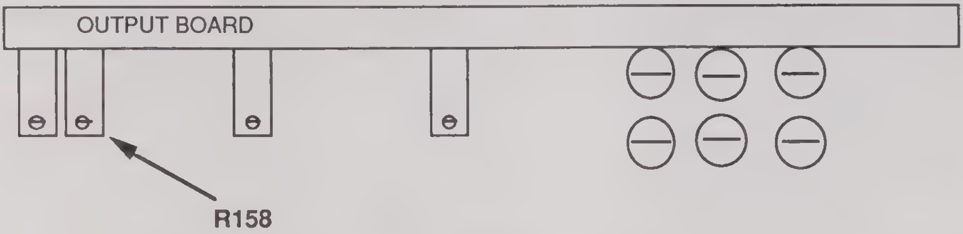


Figure 4-12. R158 Locator

3. Press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING then shows TRI AMPL R211 1.

Step 12 Adjust Triangle Amplitude

1. The Model 95 displays TRI AMPL R211 1. Connect test equipment as shown in figure 4-13 and set the scope to measure Vdc. Note the amplitude of the triangle wave.

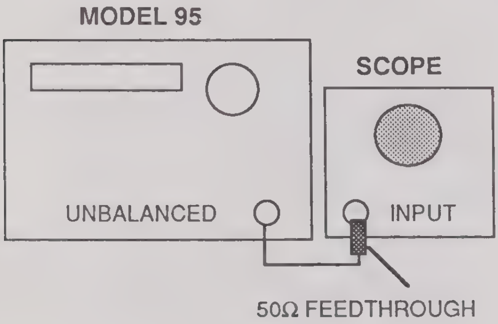


Figure 4-13. Triangle Amplitude Setup

2. On the Model 95, rotate the Knob until display shows TRI AMPL R211 2. Note the amplitude of the square wave.
3. Use the Knob to step between the triangle and square waves. Slide the cover back. Adjust R211 (see figure 4-14) on the PLL board until the peak to peak amplitude of the triangle matches the peak to peak amplitude of the square wave. Slide the cover back on.
4. Press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING then shows SIN AMPL R208 0.

Step 13 Adjust Sine Amplitude

1. The Model 95 displays SIN AMPL R208 0. Leave the test equipment connected as shown in figure 4-13.
2. On the Model 95, rotate the front panel Knob until display shows SIN AMPL R208 2. Note the amplitude of the square wave.
3. Use the Knob to step between the sine and square waves. Slide the cover back. Adjust R208 on the PLL board (see figure 4-15) until the peak to peak amplitude of the sine wave matches the peak to peak amplitude of the square wave. Slide the cover back on.
4. Press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING then shows HF SYM R9.

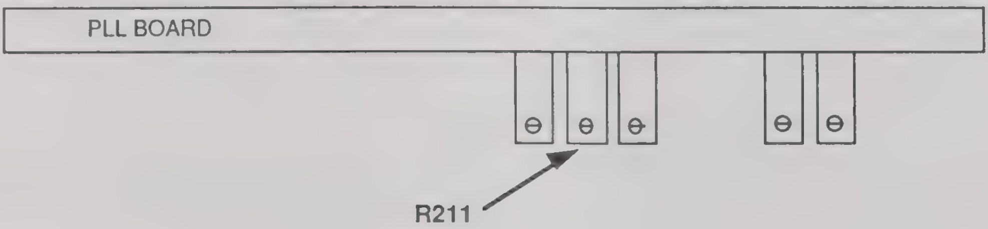


Figure 4-14. R211 Locator

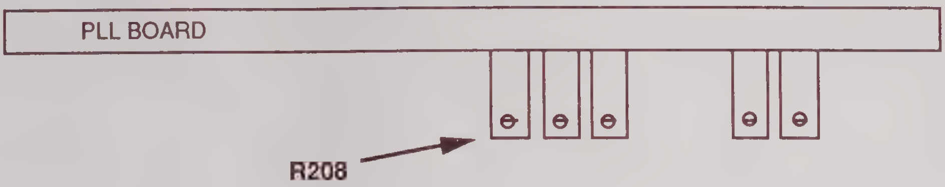

PLL BOARD
R208

Figure 4-15. R208 Locator

Step 14 Adjust High Frequency Symmetry

1. The Model 95 displays HF SYM R9. Leave the test equipment connected as shown in figure 4-13.

2. Slide the cover back, and adjust R9 on the output board (see figure 4-16) while observing the scope. Use the scopes delta time cursors to measure the two halves of the square's time symmetry between the 50% points. Adjust R9 until the time symmetry is equal ±0.5 ns. Slide the cover back on.

3. Press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING then shows HFQ R67;69;70;86;87.

Step 15 Adjust High Frequency Waveform Quality

1. The Model 95 displays HFQ R67;69;70;86;87. Leave test equipment as shown in figure 4-13.

2. Slide the cover back. Adjust R67, R69, R70, R84, R86, and R87 on the output board (see figure 4-17) for best time symmetry and aberrations. The leading and trailing edge transition time must be less than 7.5ns. Transition time is measured between the 10% and 90% points of the square wave. Aberration must be less than 4%. The Model 95 unbalanced output must be terminated with 3 feet of coax cable and the cable terminated with a 50Ω terminator for specified waveform quality. Slide the cover back on.

3. Press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING then shows PHASEOY XXXXX.

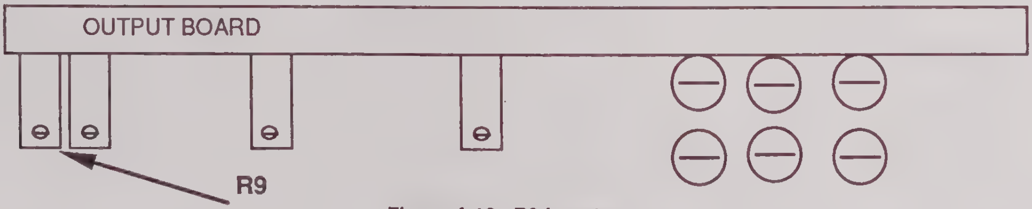

OUTPUT BOARD
R9

Figure 4-16. R9 Locator

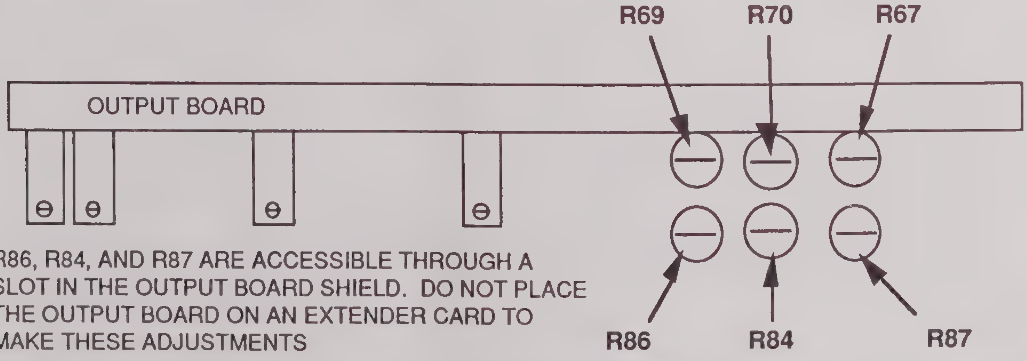

R69
R70
R67
OUTPUT BOARD
R86, R84, AND R87 ARE ACCESSIBLE THROUGH A SLOT IN THE OUTPUT BOARD SHIELD. DO NOT PLACE THE OUTPUT BOARD ON AN EXTENDER CARD TO MAKE THESE ADJUSTMENTS
R86
R84
R87

Figure 4-17. R67, R69, R70, R84, R86, and R87 Locator

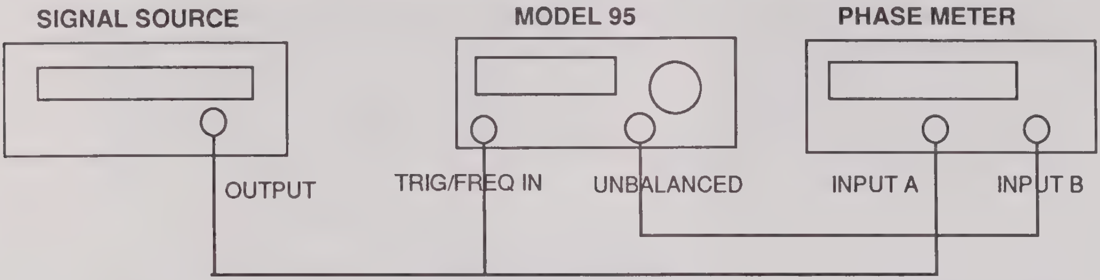


Figure 4-18. Phase Setup

Step 16 Adjust Phase 0°

1. The Model 95 displays PHASE0Y XXXXX where XXXXX represents a calibration value. Connect the test equipment as shown in figure 4-18. Appendix B contains an alternate method of calibrating phase using a scope.

2. Set the signal source controls as follows:
   Set Function to Sine.
   Frequency to 2.01 kHz.
   Output Level to 5Vpp.

3. On the Model 95,
   Adjust the Knob to until the phase meter read 0°.
   Press the TRIG FREQ key. Verify that the display flashes CALIBRATING for then displays PHASE+180Y XXXXX. Pressing TRIG FREQ key stores the calibration value in internal memory.

Step 17 Adjust Phase +180°

1. The Model 95 displays PHASE+180Y XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure 4-18. Do not change the signal source. Appendix B contains an alternate method of calibrating phase using a scope.

2. On the Model 95,
   Adjust the Knob to until the phase meter reads +180°.
   Press the TRIG FREQ key advance to the next step. Verify the display flashes CALIBRATING and then displays PHASE–180Y XXXXX. Pressing TRIG FREQ key stores the calibration value in internal memory.

Step 18 Adjust Phase -180°

1. The Model 95 displays PHASE-180Y XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure 4-18. Do not change the signal source. Appendix B contains an alternate method of calibrating phase using a scope.

2. On the Model 95,
   Adjust the Knob to until the phase meter reads -180°
   Press TRIG FREQ key to advance to the next step. Verify that the display flashes CALIBRATING and then displays SQ PHASE 0 XXXXX. Pressing TRIG FREQ key stores the calibration value in internal memory.

Step 19 Adjust Square Phase 0°

1. The Model 95 displays SQ PHASE 0 XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure 4-18. Do not change the signal source. Appendix B contains an alternate method of calibrating phase using a scope.

2. On the Model 95,
   Adjust the Knob until the phase meter reads 0°.
   Press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING and then displays CONFIDENCE. Pressing TRIG FREQ key stores the calibration value in internal memory.

Step 20. Confidence Check

1. The Model 95 displays CONFIDENCE which tests and verifies the accuracy of the Model

95's voltage reference, DVM, and output amplifier. Connect test equipment as shown in figure 4-19 (no termination).

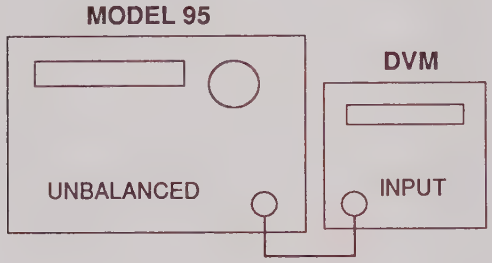


Figure 4-19. Confidence Check Setup

2. Measure the Model 95's unloaded output dc voltage with the DVM. Verify the output voltage measures between +9.8 and +10.2 Vdc.

3. On the Model 95, press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING and then displays AUTOCAL ENABLE.

Step 21. Autocal Enable/Disable

1. The Model 95 displays AUTOCAL ENABLE. Use the Knob to step between AUTOCAL ENABLE and AUTOCAL DISABLE. When Autocal is enabled, the operator can Autocal the Model 95 as described in paragraph 4.2. When Autocal is disabled the operator cannot run the Autocal procedure. If Autocal is selected (SHIFT and CALIBRATE), the Model 95 displays the message AUTOCAL DISABLED.

2. On the Model 95, press the CALIBRATE key. Verify the Model 95 displays END CAL. The Calibration Procedure is now complete.

CAUTION

Failing to perform Step 21 item 2 will keep the calibration parameters from being stored in memory, and the units calibration will be corrupted.

Step 22. Wrap up Calibration

1. Remove the power and disconnect the test equipment.

2. Install the shield and top cover using the five screws.

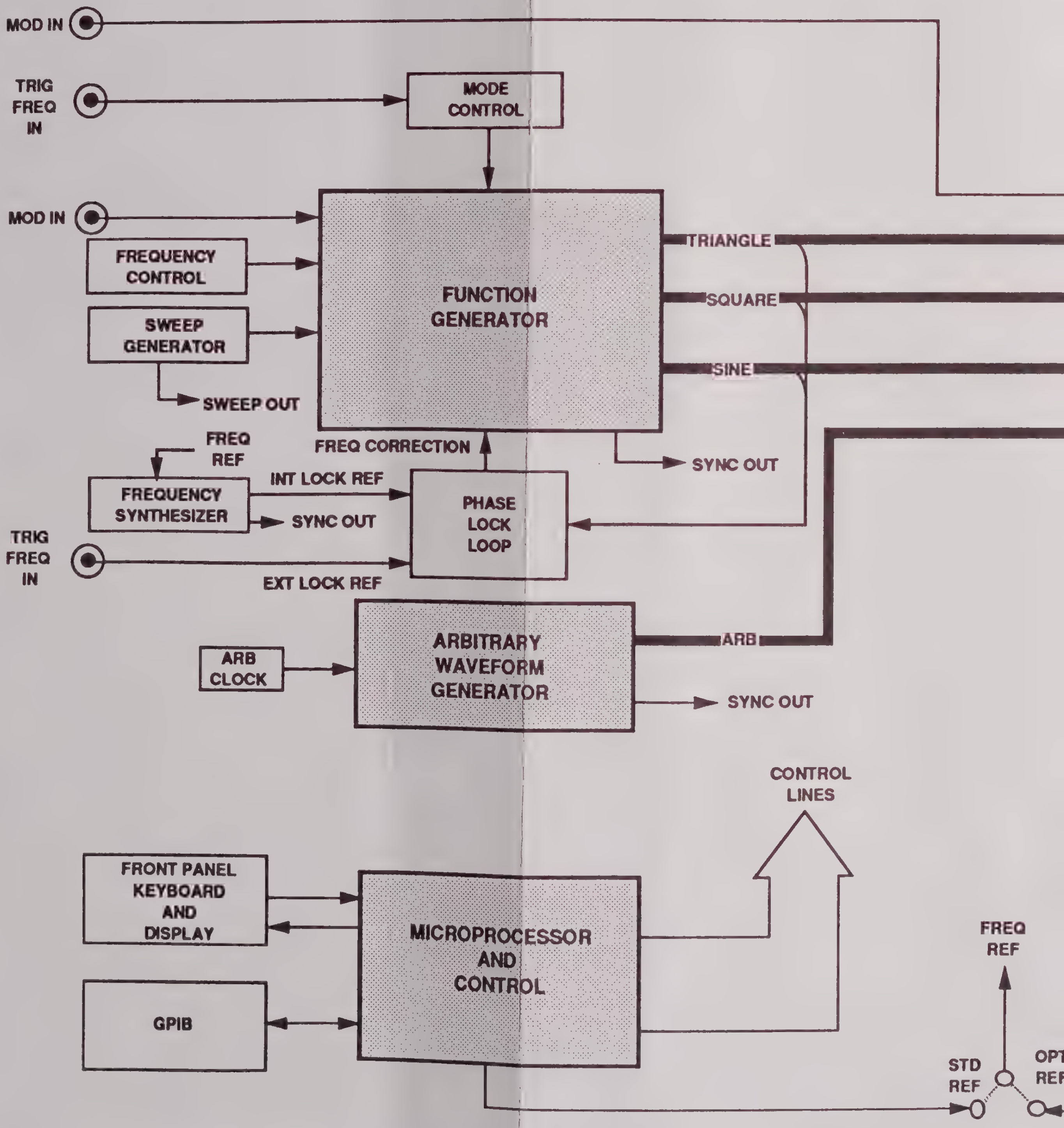
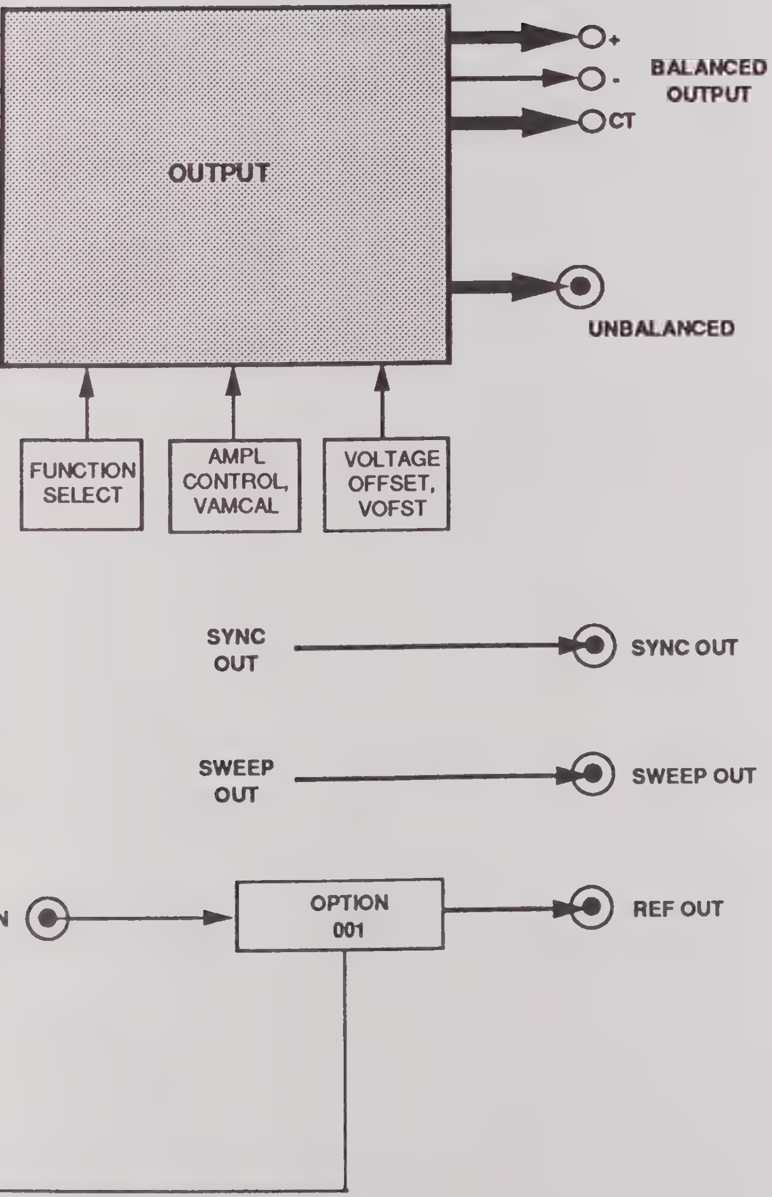

MOD IN
TRIG FREQ IN
MODE CONTROL
MOD IN
FREQUENCY CONTROL
SWEEP GENERATOR
SWEEP OUT
FUNCTION GENERATOR
TRIANGLE
SQUARE
SINE
FREQ REF
FREQ CORRECTION
INT LOCK REF
FREQUENCY SYNTHESIZER
SYNC OUT
PHASE LOCK LOOP
SYNC OUT
TRIG FREQ IN
EXT LOCK REF
ARB CLOCK
ARBITRARY WAVEFORM GENERATOR
ARB
SYNC OUT
CONTROL LINES
FRONT PANEL KEYBOARD AND DISPLAY
MICROPROCESSOR AND CONTROL
GPIB
FREQ REF
STD REF
OPT
REF

FIGURE 5-1 Model 95 Functional Blocks.


OUTPUT
+
-
BALANCED OUTPUT
CT
UNBALANCED
FUNCTION SELECT
AMPL CONTROL, VAMCAL
VOLTAGE OFFSET, VOFST
SYNC OUT
SYNC OUT
SWEEP OUT
SWEEP OUT
N
OPTION 001
REF OUT

SECTION 5
CIRCUIT DESCRIPTION

5.1 THE MODEL 95

This section describes the the Model 95 Synthesized Arbitrary Function Generator. Section 5 is divided into two parts: the basic functional block description and the detailed block descriptions. The intent is to provide an insight into signal flow through the Model 95, as well as, what controls that signal flow.

In this description, functional blocks are organized by signal flow rather than actual assemblies. The Model 95 consists of four major functional blocks (Function Generator, Arbitrary Waveform Generator, Output, and Microprocessor Section) as shown in figure 5-1. The waveforms originate from the Function Generator and Arbitrary Waveform Generator block and are routed to the Output block. All functional blocks are contained in six separate assemblies (Motherboard, Output board, Function Generator board, Phase Lock Loop board, Arb board, and Front Panel). The motherboard links all blocks within the Model 95.

The Function Generator block produces the triangle, square and sine waves supplied by the Model 95. Also, it provides frequency and symmetry control of the waveforms. Frequency of the Function Generator is controlled by one of four inputs: Frequency Control, Sweep Generator, Phase Lock Loop, and external Modulation Input.

Frequency Control sets up the generator's fixed frequency. If a synthesizer mode is selected, the Phase Lock Loop supplies a frequency correction voltage which locks the Function Generator's frequency to an internal or external frequency. The Phase Lock Loop receives its internal frequency input from the Frequency Synthesizer which is referenced to the Freq Ref or optional reference. The phase lock loop gets its external frequency from Trig Freq In connector which allows phase shift of the output waveform relative to the source. If the sweep mode is selected, the Sweep Generator sets the stop frequency and sweep length; Frequency Control sets the start frequency. Another frequency control input, Mod In, allows external modulation of the frequency.

The Mode Control controls the operating mode of the Function Generator. It allows the Function Generator to produce continuous waveforms, single cycled triggered waveforms, and multiple cycled gated and burst waveforms. Burst allows a user-defined number of cycles to be produced.

The Arbitrary Waveform Generator permits the user to create and edit unique waveforms and store as many of these waveforms as will fit in its four 8K blocks. The Arb Generator selects the Arb waveform and routes it to the Output block.

The Output block selects the waveform, controls the output level and offset, and drives the external devices. The output level can be fixed or modulated (Amplitude Modulated or Suppressed Carrier Modulated).

The Microprocessor Section provides the processing and interfacing for the Model 95. It supplies the analog control voltages like the frequency control voltage or amplitude control voltage. It also supplies the digital control lines that control the signal routing through out the Model 95. The Microprocessor Section interfaces with the display/keyboard and the GPIB interface.

5.2 FUNCTION GENERATOR

5.2.1 Introduction

The function generator section produces the Model 95's square and triangle waves, as well as, the sine wave. The Function Generator block includes:

VCG Summing Amplifier,
Symmetry Control,
Function Generator Loop (current sources, frequency range capacitors, capacitance multiplier, triangle buffer, comparator, and diode gates),
High Frequency Compensation,
Sine Convertor,
Trigger (Mode) Control.

Figure 5-2 illustrates the Function Generator Block. The heavy line through the diagram indicates signal flow.

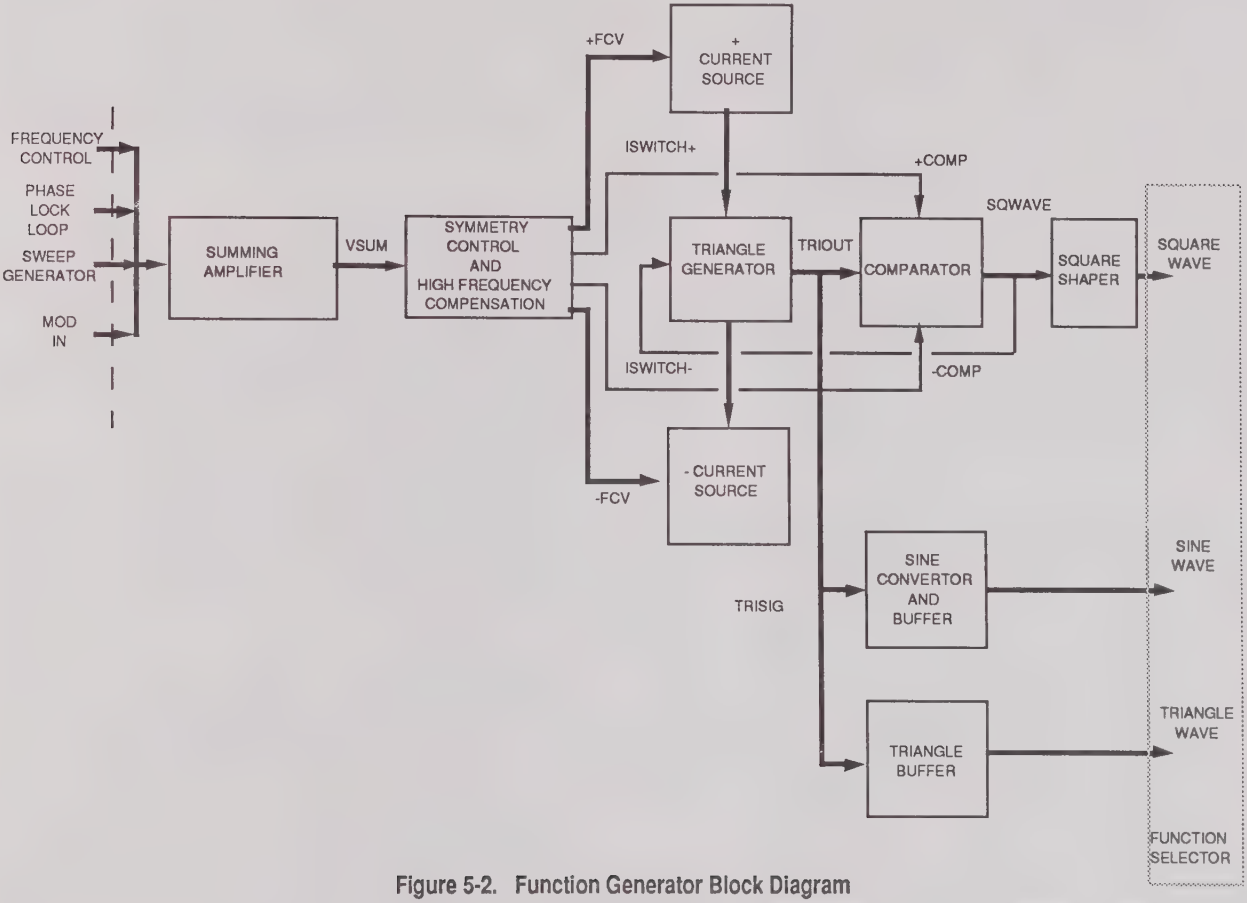

+FCV
+ CURRENT SOURCE
FREQUENCY CONTROL
PHASE LOCK LOOP
SWEEP GENERATOR
MOD IN
SUMMING AMPLIFIER
VSUM
SYMMETRY CONTROL AND HIGH FREQUENCY COMPENSATION
ISWITCH+
+COMP
SQWAVE
TRIANGLE GENERATOR
TRIOUT
COMPARATOR
SQUARE SHAPER
SQUARE WAVE
ISWITCH-
-COMP
- CURRENT SOURCE
-FCV
SINE CONVERTOR AND BUFFER
SINE WAVE
TRISIG
TRIANGLE BUFFER
TRIANGLE WAVE
FUNCTION SELECTOR

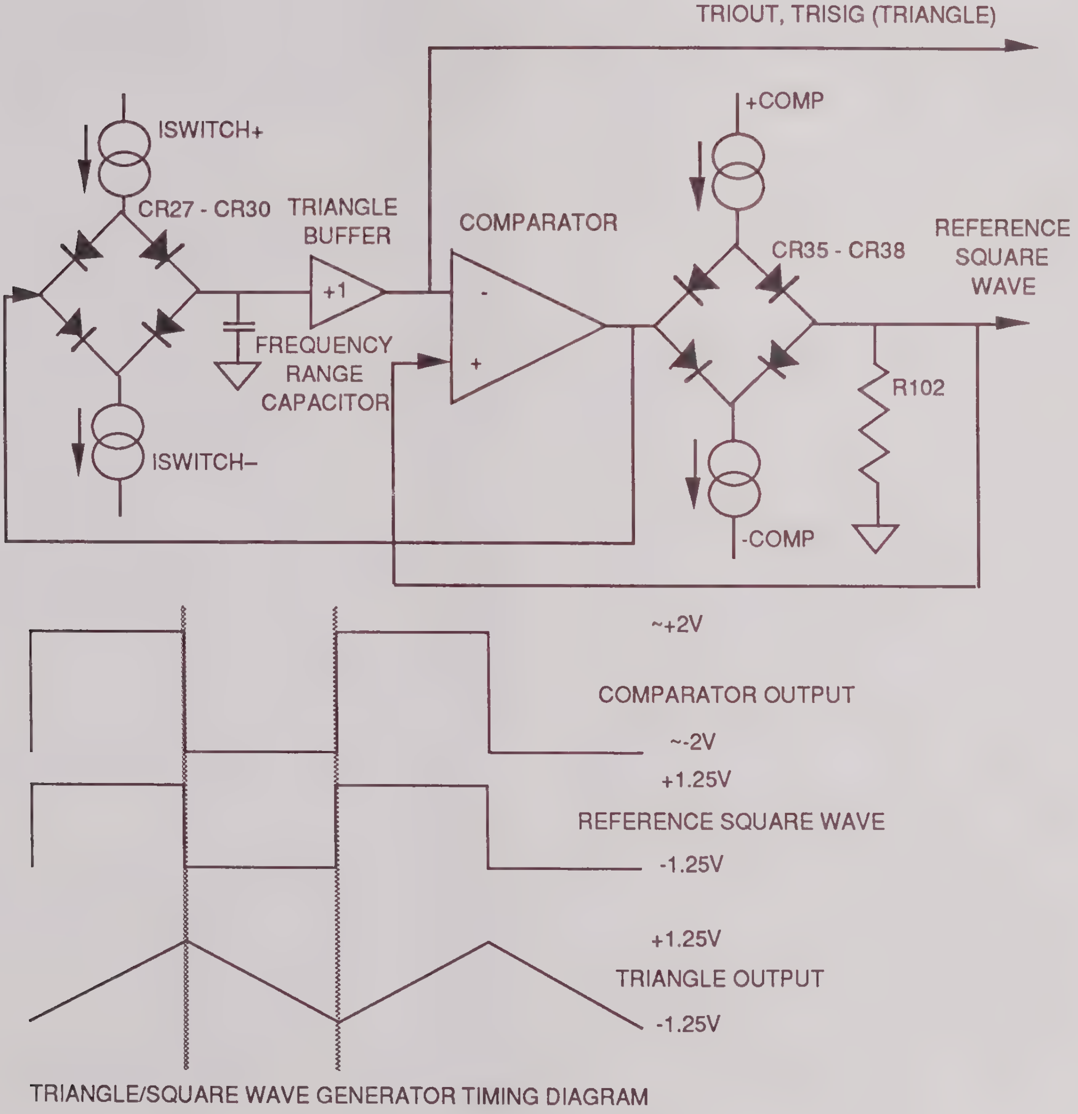
Figure 5-2. Function Generator Block Diagram

The Phase Lock Loop, Frequency Control, Sweep Generator, and Mod In provide either dc or ac plus dc voltage to the VCG Summing amplifier. These inputs control the instantaneous frequency of the waveform. The VCG Summing Amplifier produces an output, VSUM, which is the summation of all four inputs. VSUM drives the Symmetry Control which produces two voltages, +FCV and –FCV, which will control the VCG (constant) Current Sources. When the waveform symmetry is 50%, the two voltages, +FCV and -FCV, will be equal but opposite polarity. However when the symmetry is anything but 50%, the voltages, +FCV and -FCV will be unequal. The VCG Current Sources controls the charge and discharge rate of the the Function Generator Loop's Frequency Range Capacitors. The Function Generator Loop produces two output signals: the square wave and the triangle wave. The square wave runs directly to the Square Shaper (paragraph 5.4.2). The triangle wave drives the Triangle Buffer or the Sine Convertor. The outputs from the Sine Converter and Triangle Buffer drive the Function Selector (paragraph 5.4.2). The High Frequency Compensation circuit makes allowances for delays in the Function Generator Loop at the higher frequencies. Trigger Control turns on or off the Function Generator Loop based on the mode selected.

5.2.2 Function Generator Loop

The Function Generator Loop consists of the VCG Current Sources, Frequency Range Capacitors, Capacitance Multiplier, Triangle Buffer, Comparator, and Diode Gates. The Function Generator Loop produces the unit's square and triangle waves.

The following example illustrates how the function generator loop operates. See figure 5-3. First, assume the comparator's output is high. This biases diode gate CR35 - CR38 to allow the current +COMP to flow into the resistor (R102) establishing the positive reference square wave voltage. The positive reference voltage is about +1.25V (V=+ICOMP x R102). Also, when the comparator output is high, the diode gate (CR27 - CR30) is biased to allow the current, ISWITCH+, to charge the Frequency Range Capacitor. Charging the capacitor with a constant current produces a linear ramp. The Triangle Buffer isolates the Frequency


TRIOUT, TRISIG (TRIANGLE)
ISWITCH+
+COMP
CR27 - CR30
TRIANGLE BUFFER
COMPARATOR
CR35 - CR38
REFERENCE SQUARE WAVE
+1
-
+
FREQUENCY RANGE CAPACITOR
R102
ISWITCH–
-COMP
~+2V
COMPARATOR OUTPUT
~-2V
+1.25V
REFERENCE SQUARE WAVE
-1.25V
+1.25V
TRIANGLE OUTPUT
-1.25V

TRIANGLE/SQUARE WAVE GENERATOR TIMING DIAGRAM

Figure 5-3. Function Generator Loop

Range Capacitor from the Comparator. When the ramp voltage reaches the positive reference square voltage, the Comparator output switches low. When the comparator's output is low, diode gate (CR35 - CR38) switches and allows the current -COMP to flow from resistor (R102) establishing the negative reference square wave voltage - about –1.25V. At the same time, the comparator switches diode gate (CR27 - CR30) and allows the current ISWITCH– to discharge the Frequency Range Capacitor. This cycle repeats producing simultaneous triangle and square waves. The timing diagram with figure 5-3 illustrates waveform timing.

The VCG Summing Amplifier and Symmetry control the magnitude of the currents ISWITCH+ and ISWTCH-. The Frequency Range Capacitor determines the waveform's frequency range. Increasing the currents increases the frequency. Increasing the Frequency Range Capacitor decreases the frequency. The opposite of each is also true.

Normally, the current sources, ISWITCH+ and ISWITCH- produce equal but opposite polarity currents. To change the symmetry (duty cycle) of the waveform, the Model 95 changes the ratio of the current sources. For example, the ISWITCH+ source may supply more than half of the current, while the ISWITCH– source may supply less than half of the current.

Comparator

The Comparator (schematic 1104-00-3342 sheet 7 of 7) compares the output from the triangle buffer, TRIOUT, to the reference square wave level and produces an output that drives both diode gates. Figure 5-4 provides a simplified comparator circuit.

The transistors (Q14 and Q15), connected as a differential pair, compare the TRIOUT (base Q14) to the reference square wave. The level shifter (Q19, Q20, Q21, Q22. Q23) converts the input from Q14 and Q15 collector signals into a bipolar signal that can drive the diode gates and the SQWAVE output. Diode gate (CR27, CR28, CR29, CR30) switches between the compensation current sources (+COMP and –COMP) to generate the reference square wave (ICOMP x R102). The compensation current source is adjustable over a small range in order to provide high-frequency compensation (paragraph 5.2.5). The comparator also drives the other diode gate (CR35, CR36, CR37, CR38) which switches the VCG current sources (ISWITCH+ and ISWITCH–). These currents charge and discharge the Frequency Range Capacitor. Two JFETs (Q25 and Q26) buffer the diode gate (CR27 - CR30) from the ISWITCH+ and ISWITCH– current sources.

VCG Current Sources

The VCG current sources (schematic 1104-00-3342 sheet 3 of 7) convert the two symmetry control voltages, +FCV and –FCV, into two currents ISWITCH + and ISWITCH –. Because the the current sources are mirror images, only the positive current source will be described.

The positive current source consists of two amplifiers (U13 and U14) and two transistors (Q1 and Q2). U13 and Q1 form a voltage to current converter. U13 forces the voltage across R31 to produce the the current, I_{R31}. The current I_{R31} also flows through the resistor R30 producing a voltage drop equal to +FCV. The current mirror stage (U14 and Q2) forces a voltage drop across R36 equal to +FCV. The current through R36 is ISWITCH+ and drives the diode switch (CR35 - CR38). Another output from this current source, VSOURCE, drives the Trigger Baseline Compensation circuit.

The negative current source (U17, Q3, U18, Q4) is identical to the positive current source. U17 and Q3 form the voltage to current converter, and U18 and Q4 forms the current mirror.

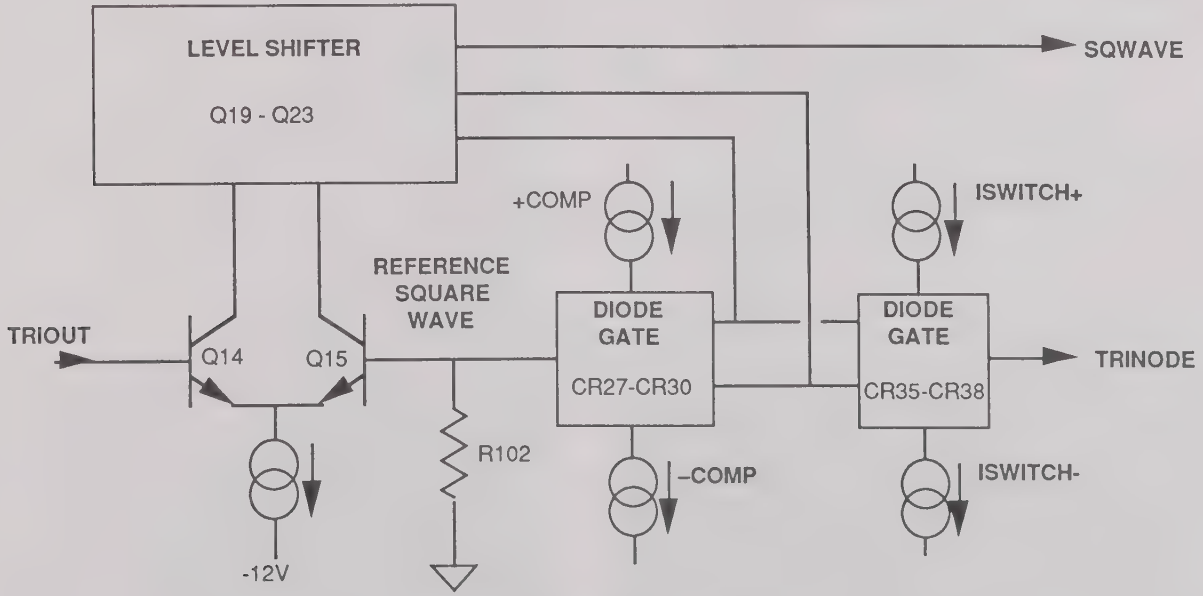


Figure 5-4. Simplified Comparator

During symmetrical operation (50%) the two resistors (R31 and R32) connect directly to ground. But selecting variable symmetry places R131 between the junction of R31 and R32 and ground which allows the connecting node to "move". The control line $\overline{\text{SYM ON}}$switches R131.

Frequency Range Capacitors and Ranges

The frequency range switches (schematic 1104-00-3342 sheet 5 of 7) change the four frequency range capacitors to the TRINODE line. On the 20 MHz range, the timing capacitance is made up of a 15 pF capacitor (C67) and stray capacitance about 50 pF total; all other capacitors are switched out. For the 2 MHz through 200 Hz ranges, capacitance is added by relay or transistor switches, table 5-1 lists the capacitance for each range. Below 200 Hz, the capacitance multiplier controls the "capacitance".

When the continuous, AM, or SCM mode is selected, the Model 95 uses only the top decade of each frequency range which allows a 10:1 frequency change. But when the FM/VCG or Sweep mode is selected, the Model 95 locks the range switching to the frequency range of the programmed upper frequency and allows the frequency to be changed a full three decades or 1000:1 frequency change. Table 5-1 lists the frequency range for both types of conditions.

Capacitance for the 2MHz, 200 kHz, 20 kHz, and 2kHz ranges is controlled by relay or transistor switches which are enabled by control lines from the boards interface logic. When a control line goes low, the capacitor is switched in. Table 5-1 lists the control lines and their associated ranges and capacitors. Paragraph 5.7.4 describes the function generator interface logic. When non-symmetrical waveforms are selected, the Model 95 switches to the next higher range to compensate for a 1/10th decrease in current source output.

Capacitance Multiplier

Lower frequencies require larger capacitors that often fail to maintain the precise value over time needed for accurate frequencies. To eliminate the need for large capacitors, the Model 95 uses a Capacitance Multiplier (schematic 1104-00-3342 sheet 6 of 7) to simulate large capacitors by dividing the current at the TRINODE. When the VCG Current Source supplies current, ISWITCH+, to the Frequency Range Capacitor, the Capacitance Multiplier draws a portion of the current from TRINODE to decrease the charging time. When the VCG Current Source draws current, SWITCH–, from the Frequency Range Capacitor, the capacitance multiplier adds current to TRINODE to decrease the discharging time.

The capacitance multiplier consists of two amplifiers (U23 and U24). The amplifier (U23) acts as a non-inverting amplifier that generates an amplified version of the TRINODE triangle waveform on one side of C62. A capacitor converts a constant slope voltage into a constant current, thus the capacitor (C62) converts the triangle voltage into a current "square wave" at the inverting input of the amplifier (U24). The output of U24, TP11, contains a square wave which is 180° out of phase with the function generator's triangle (figure 5-3). The signal at TP11 is a composite of the out-of -phase square wave and the in phase triangle because the triangle connects directly to the non-inverting input of U24. The output from U24 drives the resistor (R129) with the composite signal. But since both sides of R129 have a triangle signal, the differential signal will be the square wave which causes constant current in R129 in alternating directions with the square wave. When the ISWITCH+ is selected by the diode bridge, most of the charging current is drawn out of the TRINODE through R129 to the negative portion of TP11's square wave. When ISWITCH- is selected, the positive portion of

Table 5-1. Range Control and Values

Frequency Range			
CW, AM, and SCM 10:1 - Top Decade	**VCG/FM and Sweep 1000:1 Three Decades**	**Capacitance**	**Control Lines**
20 -2 MHz	20 MHz - 20 kHz	50 pF - (15 pF + Stray) C67	None
2MHz - 200 kHz	2MHz - 2kHz	490 pF - C57, C58, C67	≤$\overline{\text{FR8}}$
200 kHz - 20 kHz	200 kHz - 200 Hz	0.00519 µF - C55,C57, C58, C67	≤$\overline{\text{FR7}}$, ≤$\overline{\text{FR8}}$
20 kHz - 2kHz	20 kHz - 20 Hz	0.05219 µF - C53,C55,C57, C58, C67	≤$\overline{\text{FR6}}$, ≤$\overline{\text{FR7}}$, ≤$\overline{\text{FR8}}$
2kHz - 200 Hz	2kHz - 2Hz	0.52219 µF - C52, C53,C55, C57, C58, C67	≤$\overline{\text{FR5}}$, ≤$\overline{\text{FR6}}$, ≤$\overline{\text{FR7}}$ ≤$\overline{\text{FR8}}$

TP11's square wave sources current through R129 to TRINODE. The net effect is the frequency range capacitor is charged and discharged at a slower rate when the relay (K4) switches the Capacitance Multiplier to the TRINODE. Resistors R67, R68, R69, and R71 determine the square current to inverted square voltage gain of U24, and generate the bottom four frequency ranges of the function generator. Refer to table 5-2.

When the continuous, AM, or SCM mode is selected, the Model 95 uses only the top decade of each frequency range which allows a 10:1 frequency change. But when the FM/VCG or Sweep mode is selected, the Model 95 locks the range switching to the frequency range of the programmed upper frequency and allows the frequency to be changed a full three decades or 1000:1 frequency change. Table 5-2 lists the frequency range for both types of conditions.

Triangle Buffer

The triangle buffer (schematic 1104-00-3342 sheet 6 of 7) isolates the triangle node, TRINODE, from the buffer's output, TRIOUT. The triangle buffer consists of a source follower (Q11) buffered by an emitter follower (Q12). The circuit provides dc stability by monitoring the input and outputs with U25 and controlling the drain to source current in Q11 so V_{CS} = 0V. Q13 is the controlled current source.

The Auto cal circuit measures the triangle balance, TRIBAL, relative to the ground, TRICOM, and produces a triangle balance voltage, VTRIBAL. The Model 95 stores the VRTIBAL value in memory and applies it to the comparator as a correction voltage.

5.2.3 VCG Summing Amplifier

The VCG Summing Amplifier (U5 - schematic 1104-00-3342 sheet 2 of 7) algebraically adds the MOD IN, VFREQ, SWEEP, and VLOOP inputs. These input signals control the frequency of the function generator's waveform. MOD IN is the FM/VGC input which can be an ac or dc signal. VFREQ is a dc value representing the function generator's fixed frequency. The DAC Sample and Hold Network on the Motherboard (schematic 1104-00-3395 sheet 5 of 10) supplies the VFREQ signal. The Sweep Generator (schematic 1104-00-3342 sheet 2 of 7) produces a ramp that drives the SWEEP input. VLOOP is an analog frequency correction signal supplied by the phase lock loop. Another input, VCGZERO, is an Auto cal correction voltage supplied by the DAC Sample and Hold Network on the Motherboard. Output from the VCG Summing amplifier, VSUM, drives the Symmetry Control (paragraph 5.2.4).

Normally (Continuous, AM, and SCM modes), the VCG Summing Amplifier controls the generator's frequency over a 10:1 frequency change. But, the VCG Summing Amplifier can control the frequency range over a 1000:1 change when FM/VCG or Sweep modes are selected by locking the generator to the range of the upper frequency selected. See paragraph 5.2.2: Frequency Range Capacitors and Capacitance Multiplier.

Most inputs to the VCG Summing Amplifier are connected by analog switches (U4A - U4D). Each switch is controlled by a control line from the board's interface logic. The MOD IN signal connects to the amplifier when $\overline{\text{FM}}$ line (U4A) goes low. At the same time, the FM line goes high disconnecting (U4D) the FM/VCG input

Table 5-2. Range Control and Values

Frequency Range			
CW, AM, and SCM Modes 10:1 - Top Decade	**VCG/FM and Sweep Modes 1000:1 Three Decades**	**Resistance**	**Control Lines**
200 Hz - 20 Hz	200 Hz -	10 kΩ - R67	$\overline{\text{FR4}}$
20 Hz - 2Hz	20 Hz - 20 mHz	110 kΩ - R67, R68	$\overline{\text{FR4}}$, $\overline{\text{FR3}}$
2Hz - 200 mHz	2Hz - 2mHz	1.11 MΩ - R67, R68, R69	$\overline{\text{FR4}}$, $\overline{\text{FR3}}$, $\overline{\text{FR2}}$
200 mHz - 20 mHz	200 mHz - 2mHz	11.11 MΩ - R67, R68, R69, R71	All high
20 mHz - 2mHz	20 mHz - 2mHz	See Note	See Note

Note:
The Model 95 does not switch to the 20 mHz range. It actually keeps the same range capacitors as the 200 mHz range, but it decreases the input to the VCG Summing Amplifier by 1/10th effectively dropping down a decade range by switching in, $\overline{\text{SCALE}}$, an additional input resistor (R8) in series with the VFREQ input.

resistor (R3) from ground. When FM/VCG is not selected, switch (U4D) is closed. Control line $\leq\overline{\text{FR7}}$ switches in added phase lock filtering at 200 kHz and below. When the frequency is set to <20 mHz (FR0) or symmetry is not 50%, the control line $\overline{\text{SCALE}}$ inserts a resistor (R8) which divides the VFREQ input by 10 allowing the unit to operate on the middle decade of the selected frequency range. All control lines used in the VCG Summing Amplifier are supplied from the Function Generator Input Logic (paragraph 5.7.4.1).

5.2.4 Symmetry Control

Symmetry Control (schematic 1104-00-3342 sheet 3 of 7) controls the symmetry of the function generator waveform. The input, VSUM, from the VCG Summing Amplifier drives two similar circuits, one controlling the charging time (U7C) and the other controlling the discharging time (U7D). The two outputs from the circuit (+FCV and -FCV) supply equal but opposite polarity (50% symmetry) voltages. These two voltages drive the VCG Current Sources, as well as, the High Frequency Compensation circuit.

The +FCV circuit consists of the inverting amplifier (U9) with the DAC (U7C, U10) that controls the gain of the circuit. The DAC (U12B, U11A) provides an offset adjustment. The Microprocessor Section on the Motherboard loads the data values into the DACs.

The –FCV circuit consists of the non-inverting amplifier (U15) with the DAC (U7D, U16) controlling the gain. The DAC (U12A, U11B) provides an offset adjustment. The Microprocessor Section on the Motherboard loads the data values into the DACs.

At 50% symmetry (symmetrical waveform), each circuit provides equal outputs. As the symmetry setting changes away from 50% in either direction, one circuit provides greater amplification and the other less amplification. The DACs by themselves provide linear gain, but placing them in the feedback paths of U9 and U14 provides an overall circuit gain of the inverse function of the symmetry setting.

The Auto cal circuit measures the +FCV and –FCV voltage and provides correction values to the offsetDAC's data lines.

5.2.5 High Frequency Compensation

The High Frequency Compensation circuit (schematic 1104-00-3342 sheet 4 of 7) corrects for internal circuit time delays of the function generator loop on the 200 kHz to 2 MHz and 2 MHz to 20 MHz frequency ranges by decreasing the current, +COMP and –COMP, which decreases the reference square wave voltages. This causes the Comparator to switch sooner, cancelling the tendency of the triangle to grow in frequency as the frequency increases.

The High Frequency Compensation circuit consists of two DACs (U12C, U12D). The DACs use the +FCV and –FCV voltage as reference voltages. The microprocessor section provides the DACs with data which adjusts the gain of the output. Outputs from the DACs (+COMP and –COMP) will be scaled from the +FCV and –FCV.

Trigger Baseline Compensation

Trigger Baseline Compensation (schematic 1104-00-3342 sheet 4 of 7) controls the quiescent baseline level during non-continuous modes of operation. A single line, RUN, from Mode control (paragraph 5.6) controls the generation of the triangle wave by either forcing the TRINODE line to "ground" (trigger, gate, and burst modes) or "open" (continuous mode). With the RUN line low, the TRINODE line is forced to ground; with RUN high, the system operates in the normal manner.

The Trigger Baseline Compensation circuit consists of amplifiers (U19 and U20) and transistors (Q5, Q6, and Q7). Amplifier (U19) and transistor (Q5) form a voltage to current converter. A voltage equal to VSOURCE appears across the resistor (R38) producing a current I_{R30}. The current mirror (U20, Q7) reflects the current I_{R30} off the –VCG supply. The drop across R39 also equals +FCV. U20 forces a drop equal to +FCV across R40, but R40 is half the value of R39 which produces a current equal to 2(ISWITCH+). When RUN goes high, the current, 2(ISWITCH+), flows through the diode (CR10) reverse biasing diodes CR7 and CR8. This releases the TRINODE line and allows the function generator to run.

When the RUN line goes low, the diode (CR10) is reversed biased and the current flows through diodes CR8 and CR9. A current equal to ISWITCH+ flows through each diode. This forces the TRINODE to ground potential and stops the function generator. The Mode Control and Bust Counter logic on the Arb Board controls the RUN line.

5.3 ARBITRARY WAVEFORM GENERATOR

5.3.1 Introduction

The Arbitrary Waveform Generator, Arb, consists of three major blocks: the counter, random access memory (RAM), and digital to analog convertor (DAC). See figure 5-5. The RAM contains the waveform data. The counter sequences through the RAM addresses. The RAM produces the waveform data which the DAC converts into analog levels. Filters following the DACs smooth the waveform.

5.3.2 Counter and Address Arbitrator

The counter (schematic 1104-00-3327 sheet 3 of 8, U14 and U15) is a presettable 16-bit binary scanner. The preset lines, S0 - S15, determine the start address of the waveform. The counter counts up from the preset address until either a LOAD or RSTOP signal is received. At this time, the counter resets to the latest S0 - S15 address. The arbitrator (U24, U25, U26, and U27) determines the source of the data for the RAM address lines, A0 - A16. The counter is used to address RAM when generating the waveform, and the microprocessor RAM address lines are used when editing the waveform. The control line, $\overline{\mathrm{ACOE}}$, determines whether U26 and U27 send Microprocessor data or U24 and U25 send the Address Counter contents to the RAM address.

5.3.3 Active and Storage RAM

The active and storage RAM (schematic 1104-00-3327 sheet 3, U16 - U19) store up to four arbitrary waveforms. The active RAM (U16 and U18) uses the scanning address lines (A0 - A14) to step through the RAM's data. The microprocessor controls address lines (A0 - A16) when editing Arb waveforms. The storage RAM (U17 and U19) stores up to four waveforms as developed in the active RAM. When a stored waveform is to be used, it is first transferred to the active RAM. All RAM outputs are transferred on data lines, D0 - D11, which drives the DAC Register.

The control line, $\overline{\mathrm{OE8}}$, from the Arb I/O enables the active RAM's output. Two lines ($\overline{\mathrm{WEL8}}$ and $\overline{\mathrm{WEH8}}$ from the programmable array logic, PAL) supply write enable lines to the active RAM. The storage RAMs also have similar control lines: $\overline{\mathrm{OE32}}$ (output enable), and $\overline{\mathrm{WEL32}}$ and $\overline{\mathrm{WEH32}}$ (write enable).

5.3.4 DAC Register

The DAC register (schematic 1104-00-3327 sheet 3, U20 and U21) isolates the Arb data lines, D0 - D11, from the DAC data lines, RD0 - RD11. The ACK1 line from the mode control clocks the data into the register. The DAC Register synchronizes the RAM data lines to the Counter clock.

5.3.5 ARB DAC and Filters

The waveform DAC (schematic 1104-00-3327 sheet 5, U30) converts the digital data (RD0 - RD11) from the DAC register into an analog signal. The DAC uses the -12V dc supply to provide a -5Vdc operating voltage and a -1.2 V dc reference voltage. The ACK1 line from the mode control clocks the data into the DAC.

The offset DAC (schematic 1104-00-3327 sheet 5, U40) zeros the offset of the signal developed by the waveform DAC, amplifier, and filters. The value (data lines AQ0 - AQ7) for the offset DAC is determined during calibration. The Model 95 clocks the data into the DAC ($\overline{\mathrm{FOSTB}}$ goes low) at power on or when a different filter is selected. The waveform DAC and the offset DAC drive the differential amplifier (U31).

The ARB filters (schematic 1104-00-3327 sheet 5) provide three possible Arb signal paths. One path, no filter, bypasses via relay (K1) the filter routing the Arb signal directly to the Arb output OBSIG. The other paths route the Arb signal through two low pass, three-pole Bessel filters. One filter has 50 kHz cut off frequency and the other has 5MHz cut off frequency. The relay (K2) selects a filter's output and routes it to the Arb output OBSIG. Two control lines, $\overline{\mathrm{FILT1}}$ and $\overline{\mathrm{FILT2}}$, select the filters. With $\overline{\mathrm{FILT1}}$ and FILT2 high, no filter is selected. Closing the relay (K1) while leaving the relay (K2) open selects the 5MHz filter ($\overline{\mathrm{FILT1}}$ high and $\overline{\mathrm{FILT2}}$ low). Closing both relays (K1 and K2) selects the 50 kHz filter ($\overline{\mathrm{FILT1}}$ and $\overline{\mathrm{FILT2}}$ low). The Arb signal, OBSIG, is routed to the Function Selector.

5.3.6 RAM Battery Control

The RAM battery control circuit (schematic 1104-00-3327 sheet 7) uses a nonvolatile controller (U39) to select either the dc power supply or the backup battery, RVCC, to power the storage RAM. The microprocessor supplies the RAM chip enable, RC32, to the controller whose output is the storage RAM's chip select line, CS32. If the power supplied to the controller is out of limits, the controller inhibits the CS32. A Model 95 may contain one or two batteries, depending on the RAM installed.

5.3.7 Z-Axis Driver

The Z-Axis Driver (schematic 1104-00-3327 sheet 4 of 8) converts the RZBIT from the DAC register into a 50Ω signal. A three bit DAC (Q5, Q6, Q7, and Q8) controls the level of the signal. Three lines; ZAC0, ZAC1, and ZAC2; sets the DAC's level. The duty-cycle of the

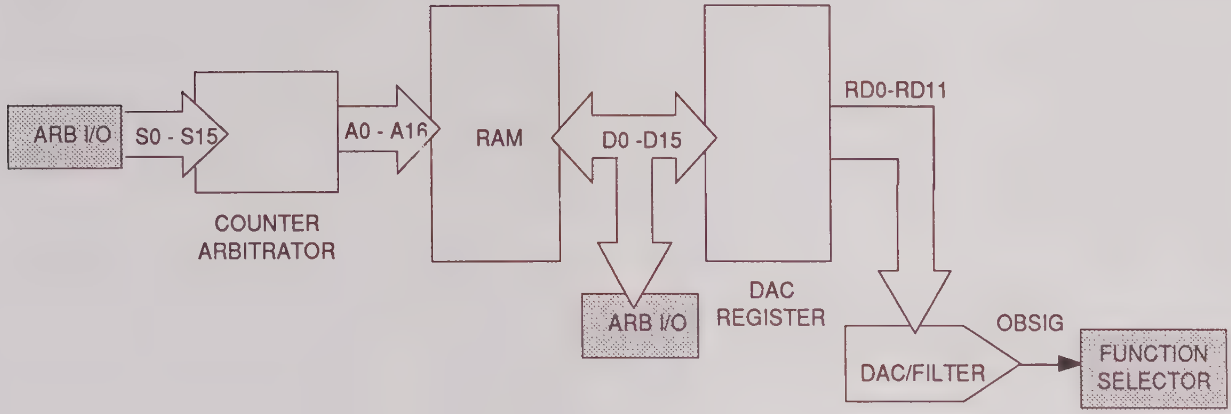

ARB I/O
S0 - S15
COUNTER
ARBITRATOR
A0 - A16
RAM
D0 -D15
ARB I/O
DAC
REGISTER
RD0-RD11
DAC/FILTER
OBSIG
FUNCTION
SELECTOR

Figure 5-5. Simplified Arb Waveform Generator

RZBIT signal may be complemented using the front panel controls or GPIB commands (*Model 95 Operator's Manual*). The Z-Axis output is active only when an Arb function and Arb edit is selected.

5.4 OUTPUT SECTION

5.4.1 General

The Model 95's output section (see figure 5-6 consists of of nine circuit blocks: the Function Selector with Square Shaper, XY Multiplier, AM Summing Amplifier, Preamplifier, Power Amplifier, 0/20 dB Attenuator, Balanced Output Driver, Unbalanced Output Attenuator Network and Impedance Control, and Balanced Output Attenuator network and Impedance Control. The output section, shown in figure 5-6, is located on three separate assemblies in the Model 95: Phase Lock Loop board, Output board and Motherboard. In figure 5-6, the bold lines represent the signal flow through the Output section. The waveform, selected by the Function Selector, flows through the XY Multiplier where its amplitude is determined by the amplitude controlling signal. The waveform is then amplified and routed through attenuators to the selected output connector.

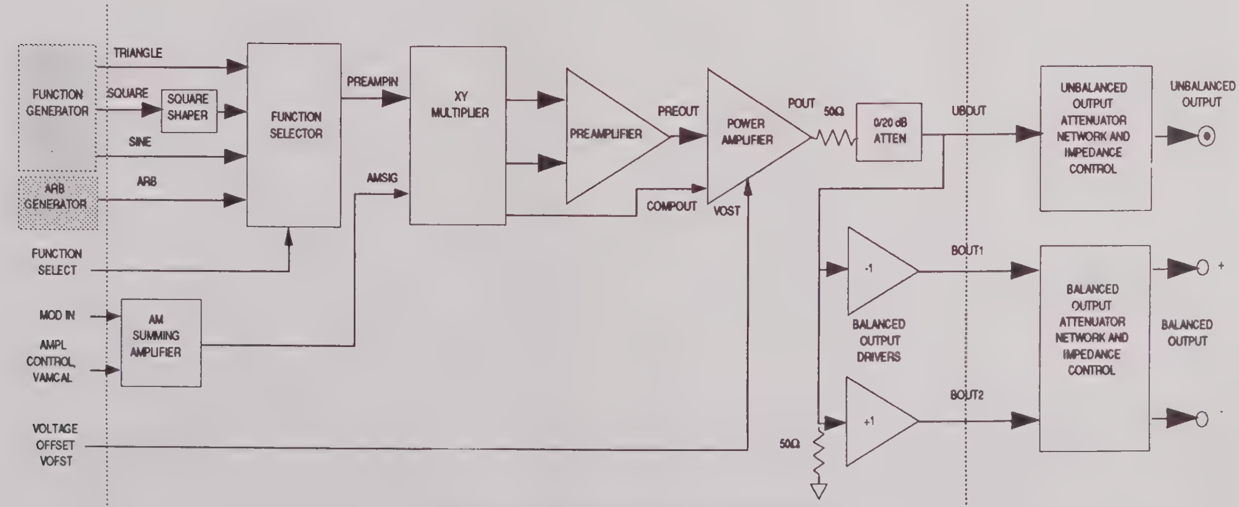

FUNCTION GENERATOR
TRIANGLE
SQUARE
SQUARE SHAPER
SINE
ARB
ARB GENERATOR
FUNCTION SELECTOR
FUNCTION SELECT
PREAMPIN
AMSIG
XY MULTIPLIER
MOD IN
AMPL CONTROL, VAMCAL
AM SUMMING AMPLIFIER
PREAMPLIFIER
PREOUT
COMPOUT
POWER AMPLIFIER
VOST
POUT
50Ω
0/20 dB ATTEN
UBOUT
UNBALANCED OUTPUT ATTENUATOR NETWORK AND IMPEDANCE CONTROL
UNBALANCED OUTPUT
-1
+1
BALANCED OUTPUT DRIVERS
BOUT1
BOUT2
50Ω
BALANCED OUTPUT ATTENUATOR NETWORK AND IMPEDANCE CONTROL
+
-
BALANCED OUTPUT
VOLTAGE OFFSET VOFST

Figure 5-6. Output Section Block Diagram

5.4.2 Square Shaper and Function Selector

The square shaper (schematic 1104-00-3335 sheet 2 of 5) converts the TTL level square wave signal (SQWAVE) from the Function Generator section to a bipolar, 2Vpp square wave. The shaper's input is a non-saturating input transistor (Q1), which produces fast switching edges. This transistor drives the level shifter (Q5 and Q6) whose output is a 3Vpp square wave which switches the diode gate (CR3 - CR6). The gate switches the positive and negative current sources which drive the load resistor (R16T). The +2 amplifier (U11) buffers the square wave and drives the Function Selector. The square wave level is approximately 1Vpp at R16T. The two transistors Q2 and Q4 are used to enable and disable the Square Shaper. When the SQRON line goes high, the Square Shaper is enabled.

The function selector circuit selects and routes either the Sine (SIN1), Triangle (TRIOUT), square (2Vpp SQUARE), or Arb (OPTSIG) waveform to the preamplifier (PREAMPIN). The function selector, located on the Output board, consists of four relays (K1 - triangle, K2 - square, K3 - sine, and K4 - Arb (schematic 1104-00-3335 sheet 2 of 6)). Microprocessor Section (schematic 1104-00-3395 sheet 3 of 10) switches the relays via the interface latch (U2 - schematic 0104-00-3335 sheet 1 of 6). When one of the relay control lines ($\overline{\text{SINSEL}}$, $\overline{\text{TRISEL}}$, $\overline{\text{SQSEL}}$, $\overline{\text{OPSEL}}$) goes low, the relay will be closed. Only one relay will close at a time. In addition, the function selector terminates each waveform input and sets the amplitude of each waveform to approximately 1Vpp using resistor networks.

5.4.3 XY Multiplier and Preamplifier

The XY Multiplier and Preamplifier (schematic 1104-00-3335 sheet 3 of 5) controls or modulates the amplitude of the selected function. The multiplier's Y input receives it's input (PREAMPIN) from the function selector. All function levels are about 1Vpp. The AM Summing Amplifier on the Phase Locked Loop board (schematic 1104-00-3341 sheet 6 of 6) supplies the multiplier's X input (AMSIG). A dc level at the X input controls the generator's amplitude level, and an ac signal modulates the generator's amplitude. The ±6V Supplies (U14A, U14D, Q27, and Q26) provides the power for the XY Multiplier.

The multiplier (U4) is a wide-band device producing differential output currents which are the product of the PREAMPIN signal and the AMSIG input. The resistors (R33 and R34) convert the multiplier's output current into voltage. A pair of Darlington emitter followers (Q22, Q23, Q24, and Q25) buffer the signal from the XY Multiplier's output and drives the differential amplifier (U5). The differential amplifier (U5) converts the differential output from the emitter followers to a single-ended output (PREOUT) of about 6Vpp (full amplitude). PREOUT is offset about +3.5 Vdc to compensate for offsets in the multiplier circuit. The multiplier offset circuit (U14C and U12) supplies a compensation voltage, COMPOUT, to the output amplifier which compensates for offset in the PREOUT signal.

5.4.4 Output Amplifier

The power amplifier (schematic 1104-00-3335 sheet 4 of 6) is a fixed gain, wide-band inverting amplifier with a push-pull complimentary symmetry output stage. This amplifier provides the gain and drive needed to drive the unit's outputs. The Output Amplifier has three signal inputs: PREOUT, COMPOUT, and VOFST. PREOUT is the selected function from the Preamplifier. COMPOUT is the multiplier compensating voltage from the multiplier's offset circuit. VOFST supplies the offset voltage to either dc offset the waveform or dc output level. VOFST is generated by the DAC Sample and Hold Network on the Motherboard. Both the COMPOUT and VOFST inputs contain inductors which improve the transient response.

The Output Amplifier has two distinct signal paths: the ac path and the dc path. The ac path provides the wide-band and high speed required by the unit's output (schematic 1104-00-3335 sheet 4 of 6). The ac path routes the signal through C36, C49, and the emitter followers Q12 and Q16 to the current sources Q13 and Q17. The emitter followers Q14, Q15, Q18, and Q19 buffer the current source from the PAOUT and feedback resistor R79 and R80. The dc path provides the low frequency path and dc stability of the output amplifier. The dc path runs through the differential amplifier Q9 and Q10. DC gain rolls off with frequency (about 80 kHz). The RC network C31 and R47 determines the roll-off frequency. The differential amplifier (Q9 and Q10) drives the inverting stage of Q11 whose output adjusts the dc bias of the current source. The amplifier's 50Ω output impedance is set by the resistors R95, R96, and R97. PAOUT also drives the Output Board's Peak Detector.

5.4.5 –20 dB Attenuator

The –20 dB attenuator circuit (schematic 1104-00-3335 sheet 5 of 6) together with the XY Multiplier and -40 dB Attenuators (Motherboard) controls the level of the output waveform. The -20 dB attenuator attenuates the power amplifier's PA OUT signal by switching in or out resistors R98 through R108. The microprocessor circuit via the Output board's data register (U3) closes the relay (K5) when the $\overline{\text{ATTEN-20}}$ goes low. R169T and C105T improves the transient response of the attenuator.

5.4.6 Balanced Drivers

The relay (K6 - schematic 1104-00-3335 sheet 5 OF 6) selects either the Balanced or Unbalanced output and routes the signal from the –20 dB attenuator to either the Unbalanced Output Attenuator Network and Impedance Network or to the Balanced Drivers. If balanced output is selected, the signal is routed through two amplifiers which produces two 180° out of phase signals, BOUT1 and BOUT2. The amplifier (U6) is a unity gain inverting amplifier. The other amplifier (U7) is a unity gain, non-inverting amplifier. The 50Ω source and load (R104 - R108) reduce the input level by 1/2 which produces a net gain of ±1/2 in the two amplifiers. The two outputs, BOUT2 and BOUT1, are routed to the Balanced Output Attenuator Network and Impedance Control (Motherboard). Both signals also drive the Peak Detector.

The balanced/unbalanced relay (K6) is controlled by the BAL-UB line from the latch (U3). When the BAL–UB line goes low, the Unbalanced output is selected. When the line goes high, the Balanced output is selected.

5.4.7 Unbalanced Output Attenuator Network and Impedance Control

The Unbalanced Output Attenuator Network and Impedance Control block on the Motherboard (schematic 1104-00-3395 sheet 7 of 10) serves two functions. It selects the output impedance of the instrument and provides 0dB or -40 dB of attenuation.

If the unbalanced output is selected, the UBOUT signal from the Balanced Driver is routed through a -40 dB attenuator (K1 – R69 through 74). The relays (K2 and K3) and their associated resistors select the output impedance (50Ω, 75Ω, or 600Ω). The relay (K6) opens the output when the Unbalanced Output is turned off. The output from this block drives the front panel's Unbalanced Output connector.

The attenuator relay (K1) is switched when U30-pin 15 goes low. When K2 and K3 are disabled (U30 pins 14 and 13 high), the output impedance is 50Ω. When relay K2 is disabled (U30 pin 14 high) and relay (K3) is enabled (U30-pin 13 low), the output impedance is 75Ω. When both K2 and K3 are enabled (U30 - pins 14 and 13 low), the output impedance is 600Ω.

5.4.8 Balanced Output Attenuator Network and Impedance Control

The Balanced Output Attenuator Network and Impedance Control block on the Motherboard (schematic 1104-00-3395 sheet 7 of 10) serves two functions. It selects the output impedance of the instrument and provides 0dB or –40 dB of attenuation.

If the balanced output is selected, the BOUT 1 and BOUT2 signals from the Balanced Driver are routed through the –40 dB attenuator (K4 along with resistors R80 through R89). The relay (K5 and its resistors) select the output impedance (135Ω and 600Ω). The output from this block drives the front panel's Balanced Output connectors.

The attenuator relay (K4) is switched when U30-pin 19 goes low. When K5 is disabled (U30-pin 12 high), the balanced output impedance is 135Ω. When K5 is enabled (U30-pin 12 low), the output impedance is 600Ω.

The control line, $\overline{\text{POE}}$, from the Microprocessor resets the attenuators to -40 dB at power up or power down.

5.5 FREQUENCY CONTROL

5.5.1 Introduction

Frequency Control covers those items that affect the frequency of the Model 95. These items include the primary frequency control - VFREQ, the sweep generator, the phase lock loop and synthesizer, and Mod In (FM/VCG).

5.5.2 VFREQ

The VFREQ line is the Model 95's basic frequency control. The line originates at the Motherboard's DAC Sample and Hold Network (paragraph 5.7.5) and runs to the Function Generator's VCG Summing Amplifier (paragraph 5.2.3). The VFRQ is a dc voltage between +8Vdc and +0.8 Vdc which represents the programmed frequency of the unit. VFREQ controls the frequency in the Continuous, CW, and AM modes. For FM, VFREQ sets the center frequency. For VCG, VFREQ sets the minimum frequency. For sweep mode, the VFREQ sets the start frequency.

5.5.3 Sweep Generator

The Sweep Generator (schematic 1104-00-3342 sheet 2 of 7) consists of an 8-bit DAC (U7A) and its buffer amplifier (U8) which produces the sweep voltage (0 to +8V) for the function generator. Another part of the sweep generator, DAC (U7B), supplies the sweep output ramp to the Sweep Out connector. VFREQ from the DAC Sample and Hold Network sets the Function Generator to the start frequency (paragraphs 5.5.2 and 5.2.3). Another dc voltage from the DAC Sample and

Hold Network, VSLEN, provides the reference for the sweep DAC (U7A). To produce the sweep, the Microprocessor sends sweep DAC data (0000 0000 to 1111 1111 for sweep up and 1111 1111 to 0000 0000 for sweep down) representing the sweep voltage for the function generator. Sweep time determines microprocessor generated data rate. The Microprocessor's data also determines the sweep shape: linear sweep or logarithmic sweep. The sweep DAC is hardwired in the write mode. The sweep DAC receives data input when the $A/\overline{B}$ and $\overline{\text{DS2}}$ lines are high, and the $\overline{\text{DS1}}$ line is low.

The DAC (U7B), part of the Sweep Generator DAC, and amplifier (U6B) supplies the SWEEP OUT ramp. The Microprocessor writes data (0000 0000 to 1111 1111 for sweep up or 1111 1111 to 0000 0000 for sweep down) to the DAC when the $\overline{\text{DS1}}$ and $A/\overline{B}$ lines are low, and $\overline{\text{DS2}}$ line is high. The shape of the output will always be linear regardless of whether linear or log sweep is selected. The sweep time determines the rate of the data from the Microprocessor. The DACs reference voltage, supplied by Zener diode (CR1) is –6Vdc.

5.5.4 Phase Lock Loop/Synthesizer

5.5.4.1 Introduction

Figure 5-7 provides a simplified illustration of the Phase Lock Loop and Synthesizer. This circuit controls the frequency of the function generator when the Model 95 operates as a synthesizer or variable phase generator. The circuit consists of six blocks located on several assemblies. The Frequency Synthesizer supplies the accurate, stable 20 Hz to 20 MHz frequency reference for the Phase Detector when internal lock is selected. For external lock, the Phase Detector receives its reference via the TRIG/FREQ IN connector on the front panel.

The variable frequency input to the phase detector closes the loop back to the function generator. The frequency input selected depends on the function selected. Either the sine or triangle wave is routed through the Zero Crossing Detector producing a square wave output. The square wave frequency runs directly into the phase detector. The phase lock loop's output, VLOOP, provides one input to the function generator's VCG Summing Amplifier.

5.5.4.2 Frequency Reference

There are two frequency references used in the phase lock loop: the internal frequency synthesizer and the external TRIG/FREQ IN. The internal frequency synthesizer produces a 20 Hz to 20 MHz TTL level output, SYNTH. The frequency synthesizer circuit (figure 5-8) consists of a 500 kHz reference, reference divider, phase detector, low pass filter, voltage controlled oscillator, ÷N divider, and ÷M divider. The frequency synthesizer circuit is located on the Motherboard (schematic 1104-0-3395 sheet 4 of 10).

The Voltage Controlled Oscillator - VCO (U15) produces an output between 10 and 20 MHz. The ÷2 and ÷N divider (part of U13) divides the VCO's output to 500 Hz which drives the variable frequency input to the phase detector (part of U13). The reference frequency, SHCLK, for the phase detector originates in the Microprocessor Section and is divided by the Reference Divider (part of U13) to 500 Hz. The phase detector's output drives the VCO input via the Low Pass Filter (U14) forcing the VCO's output to 2N times 500 Hz. The capacitor (C42) sets the frequency range of the VCO. The ÷M Counter (U17) divides the VCO output down to the programmed frequency. The Microprocessor Section loads serial data, SDATA, through the ÷N Divider to the ÷M Counter; both are enabled by the SEN line.

The external reference originates at the TRIG/FREQ IN (EXT FREQ INPUT) connector and runs through the Secondary Input/Output (schematic 1104-00-3395 sheet 6 of 10) to the Source Selector.

5.5.4.3 Sine/Tri Z-Crossing Detector

The Sine/Triangle Zero Crossing Detector (schematic 1104-00-3341 sheet 2 of 6) converts the sine wave or triangle signal, ZCSIG into a square wave. As the signal passes through its zero crossing point, the crossing detector dc output level changes high or low producing a square wave. This output is one of the input signals, Z-CROSS, to the source selector circuit. The zero crossing detector consists of a high speed comparator. Its feedback resistors (R2 and R3) ensure noise immunity. Two control lines, SELA and SELB, enable the Zero Crossing Detector.

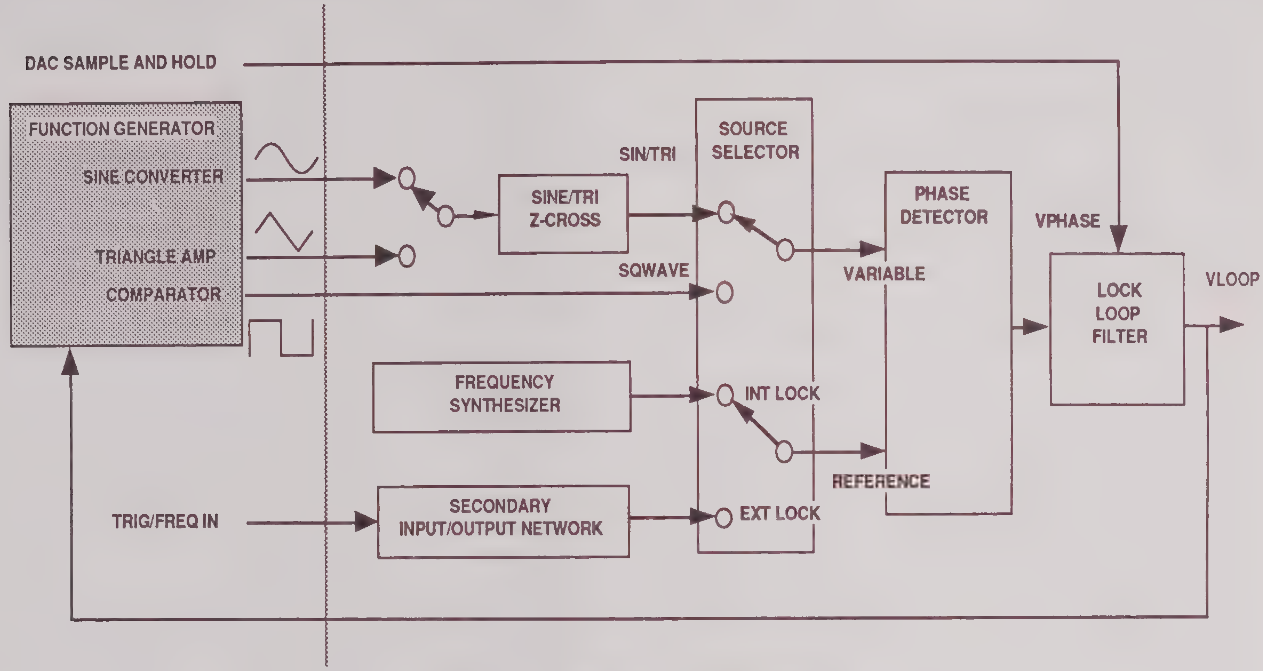

DAC SAMPLE AND HOLD
FUNCTION GENERATOR
SINE CONVERTER
TRIANGLE AMP
COMPARATOR
SIN/TRI
SINE/TRI
Z-CROSS
SOURCE
SELECTOR
SQWAVE
PHASE
DETECTOR
VPHASE
VARIABLE
LOCK
LOOP
FILTER
VLOOP
FREQUENCY
SYNTHESIZER
INT LOCK
REFERENCE
TRIG/FREQ IN
SECONDARY
INPUT/OUTPUT NETWORK
EXT LOCK

Figure 5-7. Phase Lock Loop/Synthesizer

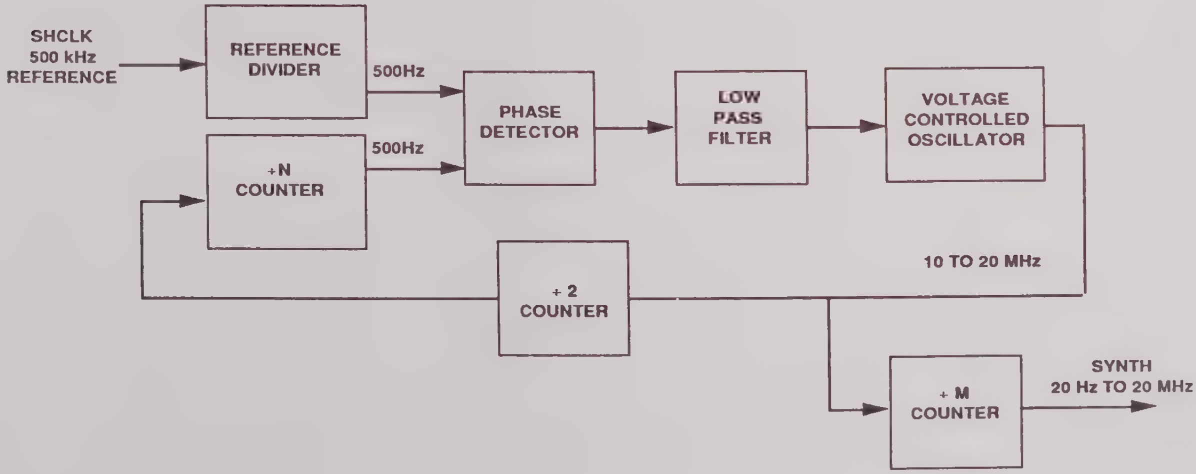

SHCLK
500 kHz
REFERENCE
REFERENCE
DIVIDER
500Hz
500Hz
÷N
COUNTER
PHASE
DETECTOR
LOW
PASS
FILTER
VOLTAGE
CONTROLLED
OSCILLATOR
10 TO 20 MHz
÷ 2
COUNTER
÷ M
COUNTER
SYNTH
20 Hz TO 20 MHz

Figure 5-8. Frequency Synthesizer

5.5.4.4 Source Selector

The source selector circuit (schematic 1104-00-3341 sheet 2 of 6) selects one of each set of frequency sources as inputs for the phase detector.

- Reference Frequency Sources
  - SYNTH - internal frequency synthesizer
  - BXFREQ - external reference source (TRIG/FREQ IN connector)
- Variable Frequency Sources
  - SQWAVE - square wave
  - PLS/SQR - Arb Sync - not used
  - Z-CROSS - sine or triangle wave converted to square wave

Two control lines, SELA and SELB., to the Source Selector choose the frequency sources. One reference frequency source and one variable frequency source will be selected. When SYNTH is selected, SQWAVE will also be selected. When BXFREQ is selected, either of the three variable frequency waveforms can be selected. The $\overline{\text{LOCK}}$ line enables (low) the Source Selector.

5.5.4.5 Phase Detector

The Phase Detector consists of two biquinary (÷2 and ÷5) Counters, the Phase Comparator, and the Charge Pump (schematic 1104-00-3341 sheets 2 and 3 of 6). Each input to the Phase Comparator runs through the ÷10 (20 - 2MHz range) or the ÷2 (all other ranges) counters (U4A and U4B) prescaling the input frequency. The phase comparator, a PAL, compares the reference frequency signal and the variable frequency signal, and produces an output based on edge arrival times of each monitored signal. The comparator generates one of three possible output conditions using the VLAGR and VLEADR lines. These lines drive the charge pump.

The Charge Pump (schematic 1104-00-3341 sheet 3) controls the current to and from the Lock Loop Filter. The Charge Pump consists of a diode gate (CR2 - CR5), a positive current source (Q1), and a negative current source (Q2). The diodes (CR1 and CR6) provide temperature compensation for their respective current sources. The VLAGR and VLEADR inputs from the phase comparator switch the charge pump current. The duration and direction of current represents the phase difference between the selected reference frequency signal and the variable frequency signal. The time difference between the edges determines the amount of current pumped into the lock loop filter. The phase difference between the edges determines the direction of current flow. When the signals arrive concurrently, no current is pumped to the Lock Loop Filter.

5.5.4.6 Lock Loop Filter

The Lock Loop Filter circuit (schematic 1104-00-3341 sheet 3 of 6) converts the pulsating current from the Charge Pump into a dc error voltage, VLOOP. The error voltage, VLOOP, gradually changes the VCG Summing Amplifier output signal, VSUM, to match the generator frequency and phase with the reference frequency.

When the reference to generator frequency difference is too large for the system to handle, the UNLOCK indicator on the front panel will flash. When FM or sweep modulation is selected, the $\overline{\text{LOCK}}$ line is high, opening the VLOOP line, and the UNLOCK indicator remains on.

The filter characteristics of the circuit are controlled by the Microprocessor Section, based on the signal frequency. Solid state switches (U17A - U17D) select the various filter circuit combinations. VPHASE supplies the voltage that varies the phase (PHASE key or PHASE command).

5.6 MODE CONTROL

5.6.1 Introduction

Mode Control (schematic 1104-00-3327 sheet 2) turns on and off the Function Generator Loop (paragraph 5.2.2) via the control line, RUN. The Mode Control consists of the Mode Control GAL (U9), Burst Counter (U13), and Trigger Control (U12A), as well as the board I/O logic (schematic 1104-00-3327 sheet 2 of 8).

5.6.2 Mode Control

The Mode Control (U9) is a programmed GAL that serves several functions: function generator mode control and Arb clock control.

To control the function generator's operating mode, Mode Control decodes lines from the board I/O to control the Trigger Control (U12A). The input lines, MCNTL1 and MCNTL2 select the operating mode, and the input line, SRCNTL, selects the trigger source. SRCNTL low selects External Source, BXFEQ, and SRCNTL high selects Internal Source, SYNTH. Another line, MANTRIG, represents pressing the MAN TRIG key or its GPIB equivalent. The BURST line from the Burst Counter controls Mode Control in the burst and internal gate modes. Table 5-3 describes the relationship between the Mode Control input control lines and the selected modes. Mode Control produces three control lines; RSET, JSET, and KSET; for the trigger control.

Table 5-3. Mode Control

Control Line	Cont	Trig	Int Gate	Ext Gate	Burst
MCNTL1	0	0	1	0	1
MCNTL2	0	1	1	1	1

The Mode Control also supplies the ARB clocks, ACK1 and ACK2. CLKSEL1 and CLKSEL2 selects the input source for the ARB clocks from the SQWAVE, SYNTH, BXFREQ, or $\overline{\text{LCLK}}$ inputs.

5.6.3 Trigger Control

Trigger Control (U12A), a JK Flip Flop, provides the RUN line that controls the operation of the Function Generator (Trigger Baseline Compensation-paragraph 5.2.5).

Continuous Mode. To place the function generator in the continuous mode, the Mode Control holds its RSET line low which forces the Trigger Control's RUN line high and allows the function generator to run.

Triggered Mode. For the triggered mode, the Mode Control strobes the RSET line low to start the function generator after a triggering event. Also, the Mode Control holds JSET line low and KSET line high. The next negative transition of the SQR (square) from the function generator clocks the Trigger Control, which changes the RUN line to low and turns off the function generator. The function generator will always complete a full cycle.

Internal Gate and Burst Mode. Internal gate mode is actually a burst mode. The Model 95 determines what should be the correct number of cycles for 50% duty cycle of the internal gate frequency, and sets up the Burst Counter. The Mode Control strobes the RSET line low which starts the function generator. Also, the Mode Control places JSET high and KSET low. Once the Burst Counter determines the correct number of cycles has occurred, it places the Mode Controls BURST high which sets JSET low and KSET high until the Trigger Control's QNOT line goes high.

External Gate. The Mode Control strobes the RSET line low which starts the function generator. Also, the Mode Control holds JSET high and KSET low as long as the trigger input is true. When the trigger input goes false, JSET goes low and KSET goes high until the QNOT goes high.

5.6.4 Burst Counter

The Burst Counter (U13),a programmable ÷N down counter, signals the Mode Control when the programmed number of cycles is completed. The Microprocessor loads the serial data, BRSDIN, into the Burst Counter using the serial clock, BRCLK when the serial input is enabled, SRSEN. The counter, when clocked, BRCP, counts down to zero and the BURST line to the Mode Control goes low, indicating that the burst has been completed.

5.7 MICROPROCESSOR AND INTERFACES

5.7.1 Introduction

The Microprocessor and its interfaces provides the data processing and routing throughout the Model 95. This block includes the Microprocessor Section, Function Generator Interface, Arb Board Interface, Phase Lock Board Interface, Output Board Interface, Front Panel (Keyboard and Display) Interface, and the GPIB Interface. All interfaces, except the GPIB interface, are located on individual boards. Also, the DAC Sample and Hold Network and Internal Calibration Network operate with the Microprocessor Section. Figure 5-9 illustrates the relationship between the Microprocessor Section and Interfaces, as well as lists the Interface's enabling lines and data busses.

5.7.2 Microprocessor Section

The Microprocessor Section (schematic 1104-00-3395 sheet 3 of 10) controls all operations within the Model 95. The Microprocessor Section consists of the Microprocessor, Read Only Memory - ROM, Calibration/Scratch Pad Memory, and Processor Support Chip, plus support circuits. The Microprocessor section receives its input data from the front panel or GPIB interface, processes the data, and provides data and control lines for internal operation. Figure 5-10 provides a simplified look at the Microprocessor Section.

The microprocessor (U6) executes operating instructions based on firmware stored in the ROM (U12). Another memory, the Calibration/Scratch Pad Memory (U11) - a Random Access Memory - RAM, stores the calibration data taken during Auto cal and manual calibration. This memory also stores the instrument setup at power off and ten stored settings, as well as, providing a temporary storage register during data processing. The RAM accepts data (writes) when its

WE line goes low. If the WE line is high, the microprocessor section reads data from the RAM. A RAM backup battery (BT1) prevents the loss of data when power is turned off. A flashing life light verifies microprocessor sequencing. The PAL (U35) provides additional address decoding for the ROM (U12) expanding the memory size for the Model 95's firmware.

The Processor Support Chip (U7) controls the interfacing with other parts of the Model 95, as well as, decoding the lower eight address lines, A0 - A7. Seven card select lines from the Processor Support Chip enable interfaces in the Model 95.

$\overline{\text{GPIB}}$	GPIB interface
$\overline{\text{ROM}}$	ROM via U35
$\overline{\text{RAM}}$	RAM via U35
$\overline{\text{FPSTB}}$	Front Panel
$\overline{\text{OBSTB}}$	Output Board
$\overline{\text{FGSTB}}$	Function Generator
$\overline{\text{OXSTB}}$	Arb Board

Four Quiet Address Lines, QA0 - QA3, address the board interfaces in the Model 95. In addition, the Processor Support Chip connects the eight Quiet Data Lines, QD0 - QD7, to the board interfaces in the Model

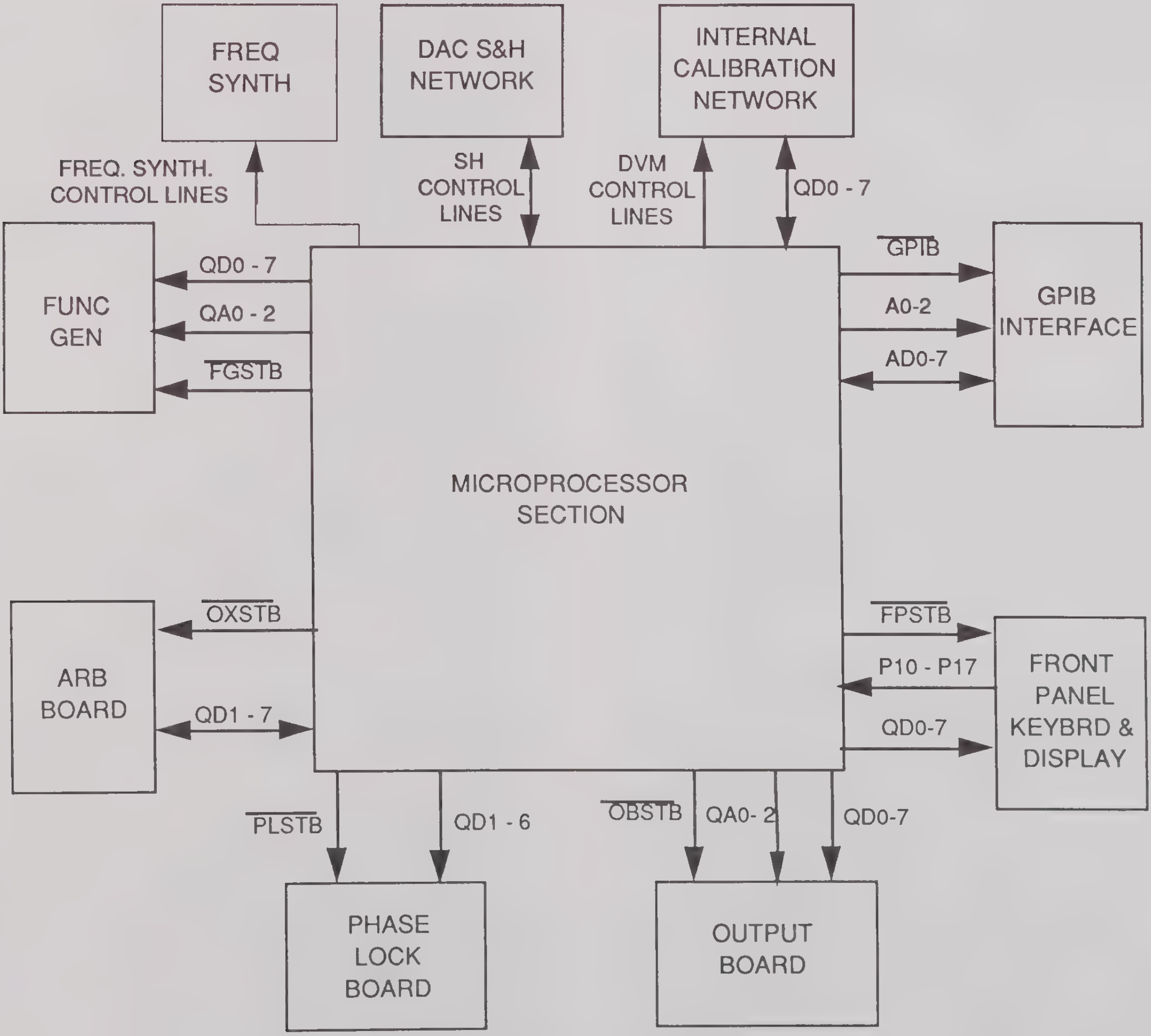

FREQ SYNTH
DAC S&H NETWORK
INTERNAL CALIBRATION NETWORK
FREQ. SYNTH. CONTROL LINES
SH CONTROL LINES
DVM CONTROL LINES
QD0 - 7
FUNC GEN
QD0 - 7
QA0 - 2
FGSTB
GPIB
A0-2
AD0-7
GPIB INTERFACE
MICROPROCESSOR SECTION
ARB BOARD
OXSTB
QD1 - 7
FPSTB
P10 - P17
QD0-7
FRONT PANEL KEYBRD & DISPLAY
PLSTB
QD1 - 6
OBSTB
QA0- 2
QD0-7
PHASE LOCK BOARD
OUTPUT BOARD

Figure 5-9. Microprocessor and Interfaces

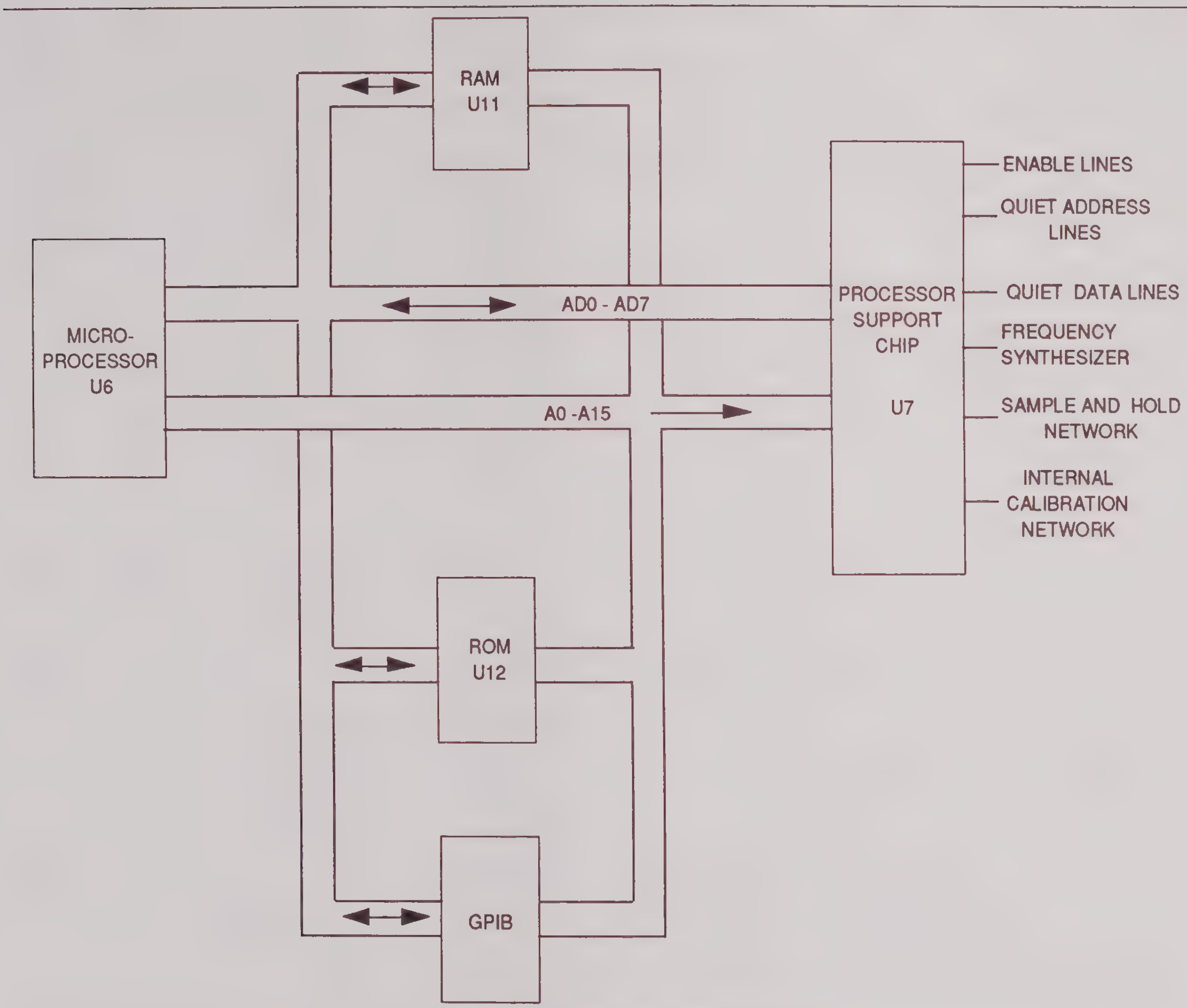

RAM
U11
MICRO-
PROCESSOR
U6
AD0 - AD7
A0 -A15
PROCESSOR
SUPPORT
CHIP
U7
ENABLE LINES
QUIET ADDRESS LINES
QUIET DATA LINES
FREQUENCY SYNTHESIZER
SAMPLE AND HOLD NETWORK
INTERNAL CALIBRATION NETWORK
ROM
U12
GPIB

Figure 5-10. Microprocessor Section

95. These lines are bidirectional and active when the microprocessor needs to communicate with the board interfaces.

Also, the Processor Support Chip controls the frequency synthesizer via the SEN, SDATA, and SCLK lines. SEN enables the synthesizer, SDATA supplies serial data which loads the synthesizer's ÷M and ÷ N counters. SCLK clocks the data into the counters.

The Processor Support Chip also produces five sets of control lines for the Sample and Hold Network. The SHEN line enables the network's DAC. SHDATA supplies the serial data that loads the DAC, and SHCLK clocks the data into the DAC. SHSEQM enables the sample and hold selector channel. Three lines; SHSEL0, SHSEL, and SHSEL2; select the sample and hold selector channels.

Another set of lines control the voltage measurement portion of the Model 95's internal calibration network. The lines, DVM0 - DVM5, select the inputs to the internal calibration network. $\overline{\text{DVM LB}}$ and $\overline{\text{DVM HB}}$ selects either the higher or lower order byte to be read by the microprocessor. DVMRUN instructs the DVM to run. DVM_RDY tells the microprocessor it has data to send. During the frequency related portion of the Auto cal cycle, the Processor Support Chip and microprocessor measures the SQWAVE, BXFREQ, and SYNTH frequency, period and symmetry. The FREQOUT line connects the Processor Support Chip and the microprocessor.

Two lines, RKA and RKB, decode the rotary encoder's (front panel control knob) rotation.

5.7.3 GPIB Interface

The GPIB interface circuit (schematic 1104-00-3390 sheet 10) allows remote operation of the Model 95 using an external IEEE-488 compatible controller. All functions except power and GPIB address are programmable using the interface. The GPIB circuit consists of a GPIB controller and two transceivers.

The GPIB controller (U8) functions as a traffic controller, permitting data to flow in either direction when the correct control information is received. The 'handshaking' routine will ensure neither the signal generator nor the remote controller will send data faster than the other can use. The controller has internal registers where control, data, and address words are loaded and stored until needed or requested. The controller bus connects to the microprocessor circuit address bus A0 - A2. The identification address of an instrument is determined by five bits in the controller address register. The default address (09) automatically loads into the controller from RAM at first (cold start) turn-on. A new address can be entered using the front panel keyboard. The GPIB line from the processor support chip enables the GPIB interface. The E clock from the microprocessor supplies the timing for the GPIB controller. The $R/\overline{W}$ line (read - high, write - low) controls the direction of data flow through the GPIB controller.

The transceivers (U9 and U10) permit bidirectional data flow. They have sufficient input sensitivity to minimize false signals and sufficient drive current to minimize signal loss. The transceiver (U9) handles the GPIB data lines, and the transceiver (U10) handles the GPIB control lines. Direction of data flow through the transceivers is controlled by the GPIB interface chip's T/R2 line.

5.7.4 Board Interfaces

Th following boards have interface logic circuits that converts data lines into control lines for use on that board.

Function Generator board
  Schematic 1104-00-3342 1 of 7,
Phase Lock Loop Board
  Schematic 1104-00-3341 1 of 6.
Arb Board
  Schematic 1104-00-3327 1 of 8.
Output board
  Schematic 1104-00-3335 1 of 6.
Display /keyboard of Front Panel
  Schematic 0103-00-3001 3 of 3.

5.7.4.1 Function Generator Interface

The function generator's interface logic consists of the input decoder (U1) and data registers (U2 and U3).

The decoder (U1) generates the clocks, CLK0 - CLK5, that will be used on the function generator board. The decoder inputs (QA0, QA1, and QA2) originate from the Microprocessor Section. The data clock selected by the address lines goes low at the the decoder when $\overline{\text{FGSTB}}$ card select line goes low. Two enable lines of the decoder (G1 and G2A) are hardwired enabled. After the $\overline{\text{FGSTB}}$ card select line returns high, all decoder outputs return high. Table 5-4 provides a truth table for the decoder and defines the CLK outputs for the function generator board interface logic.

The registers (U2 and U3) latch data on their inputs on the rising edge of their clocks. The data is generated by the Microprocessor Section. The register (U3) supplies the frequency range control lines for the Frequency Range Switches and Capacitance Multiplier.

5.7.4.2 Phase Lock Loop Interface

The phase lock loop board's interface logic consists of a single Octal data register (U1). The register latches the data on its input lines, QD0 - QD7, on the rising edge of the $\overline{\text{PLSTB}}$ card select line. The function generator interface supplies the card select line, and the Microprocessor Section supplies the data lines.

5.7.4.3 Arb Board Interface

The Arb board interface logic consists of two input decoders (U1 and U2), a data buffer (U28), eight octal data registers (U3 - U6, U26, U27, U23, and U29), and two bidirectional data buffers (U7 and U8).

The decoder (U1) selects the eight registers clocks. The other decoder provides strobe lines for the Arb. Table 5-5 defines the decoder outputs. When a decoder is enabled and $\overline{\text{OXSTB}}$ pulses low, a low pulse occurs on the decoder output line selected by QA0 - QA2. However, the decoder (U1) is enabled when the QA3 is high, and decoder (U2) is enabled when QA3 goes low. The data buffer (U28) isolates the quiet data lines, QD0 - QD7, from the registers. The registers latch data, AQD0 - AQD7, on the rising edge of their respective clocks.

Table 5-4. Function Generator Decoder

Decoder Inputs				Output	Function
QA0	QA1	QA2	$\overline{\text{FGSTB}}$		
0	0	0	⊔	CLK0	Clocks Data Register U2
1	0	0	⊔	CLK1	Clocks $\overline{\text{DS1}}$ Sweep Generator
0	1	0	⊔	CLK2	Clocks $\overline{\text{DS2}}$ Sweep Generator
1	1	0	⊔	CLK3	Clocks $\overline{\text{DS1}}$ Symmetry Control
0	0	1	⊔	CLK4	Clocks $\overline{\text{DS2}}$ Symmetry Control
1	0	1	⊔	CLK5	Clocks Range Register U3
0	1	1	⊔	$\overline{\text{PLSTB}}$	Card select for Phase Lock Loop Interface

Table 5-5. Arb Decoder

Decoder Inputs					Output	Function
QA0	QA1	QA2	QA3	$\overline{\text{OXSTB}}$		
U1						
0	0	0	1	⊔	$\overline{\text{CLK0}}$	Clocks Data Register U3
1	0	0	1	⊔	$\overline{\text{CLK1}}$	Clock Data Resister U4
0	1	0	1	⊔	$\overline{\text{CLK2}}$	Clocks Data Register U6
1	1	0	1	⊔	$\overline{\text{CLK3}}$	Clocks Data Register U5
0	0	1	1	⊔	$\overline{\text{CLK4}}$	Clocks Data Register U23
1	0	1	1	⊔	$\overline{\text{CLK5}}$	Clocks Data Register U27
0	1	1	1	⊔	$\overline{\text{CLK6}}$	Clocks Data Register U26
1	1	1	1	⊔	$\overline{\text{CLK7}}$	Clocks Data Register U29
U2						
0	0	0	0	⊔	$\overline{\text{HIGHSTB}}$	Enables Bidirectional Data Buffer U8
1	0	0	0	⊔	$\overline{\text{LOWSTB}}$	Enables Bidirectional Data Buffer U7
0	1	0	0	⊔	$\overline{\text{COPYSTB}}$	Drives Arb Gen PAL U22
1	1	0	0	⊔	$\overline{\text{LCLK}}$	Drives Mode PAL U9
0	0	1	0	⊔	$\overline{\text{FOSTB}}$	Clocks Arb Offset DAC U40

5.7.4.4 Output Board Interface

The output board's interface logic consists of the input decoder (U1) and data registers (U2 and U3). The input decoder produces the clocks which drive the data registers. The decoder inputs originate from the Microprocessor Section. When the decoder is enabled and $\overline{OBSTB}$ pulse goes low, a low pulse occurs on the decoder output line selected by QA0 - QA2. The registers latch data, QD0 - QD7, on the rising edge of their respective clocks. Table 5-6 defines the decoder outputs.

5.7.4.5 Front Panel (Keyboard and Display)

The front panel provides local operator interface to the function generator. This assembly contains the following circuits:

Control Knob Circuit
Display
Keyboard Circuit
Annunciator Circuit

Control Knob The control knob (SW1 - schematic 1104-00-3001 sheet 1 of 3) rotates continuously in both directions. Control knob values per degree of turn depend on the function, mode, and range selected. Rotating the knob pulses its two output lines, RKA and RKB, with TTL logic levels. The Microprocessor Section on the motherboard counts these pulses to determine the amount of change and compares the phase relationship of the output lines to determine the direction of rotation.

Display The display (schematic 0103-00-3001 sheet 1 of 3) consists of the display driver (U1), Vacuum Fluorescent display (VFD1), and data latch (U3). The VFD is a triode vacuum tube with phosphorus coated anode that illuminates when electrons strike it. Each digit consists of 16 anodes with one grid. Elements of a digit lights when both the anode (+15V) and grid (+15V) are biased on. A -24V biases the grids off. The display driver (U1) controls the multiplexed arrangement of anodes and grids.

The driver receives clocked, DSCLK, serial data, DSDATA, from the input latch (U3) via the level shifters (Q1 and Q2). Another line to the driver, DSPOR, provides a power on reset to the driver.

The display circuit is powered by its own +15 V dc regulator (VR1) which uses the +22 V dc for its input. The fluorescent display filament ($8V_{rms}$ superimposed on -15 Vdc) receives its power from the FILA and FILB lines. All power is supplied from the motherboard.

Keyboard The keyboard circuit (schematic 0103-00-3001 sheet 1 of 3) consists of an eight-column, six-row matrix, input data register (U3), and decoder (U2). Control signal, FPREG, latches the quiet data bus, QD0-QD2, lines into the latch which drives the decoder. The decoder steps through the six rows, making each row high (+5V) one at a time. When a key is pressed, the high appears on the column associated with that switch. The column lines (P10 - P17) connect directly to the microprocessor circuit. The microprocessor determines which key has been pressed by analyzing the row/column status.

Annunciator Circuit The Light Emitting Diode, LED, circuit (schematic 1104-00-3344 sheets 2 and 3) consists of LEDs (CR4 - CR27), decoder (U4), and data register (U5 - U7). The LEDs identify the selected mode and function. Two other LEDs (CR1 and CR2) connected to the data register (U3) are also part of the LED circuit. The decoder (U4) converts quiet addresses, QA0 and QA1, into clocks for the four registers. Each of four registers (U3, U5 - U7) reads the quiet data bus, QD0 - QD7, and when any of the latches goes low, the LED annunciator lights. Conversely, when a latch output goes high, the LED annunciator remains off.

5.7.5 DAC Sample and Hold Network

The DAC/Sample and Hold Network (schematic 1104-00-3395 sheet 5 of 10) provides the various control voltages required throughout the Model 95. The values for these control voltages are determined during Auto cal and calibration. This circuit consists of the 16 bit DAC (U18), the 1 of 8 selector (U19), and the eight hold capacitors (C49 - 56) and buffers.

The microprocessor section loads serial data, SHDATA, using the clock, SHCLK. The line, SHEN, enables the DAC. Output from the DAC drives the selector. The

Table 5-6. Output Decoder

Decoder Inputs				Output	Function
QA0	QA1	QA2	$\overline{OBSTB}$		
0	0	0	⊔	CLK0	Clocks Attenuator Selector (Motherboard)
1	0	0	⊔	CLK1	Clocks Data Register U3
1	1	0	⊔	CLK33	Clock Data Register U2

microprocessor section's SHSEL0 - SHSEL2 lines select the channel. The voltage from the selector charges the selected capacitor (C49 - C56). The microprocessor section updates the DAC and selects the next channel. Thus, the microprocessor cycles through channels continuously refreshing the capacitors. Buffers (U20 - U24) provide a high impedance which hold the charge on the capacitors.

The DAC supplies a maximum output of ±3 Vdc. Some control voltages require voltages greater than the ±3 Vdc, therefore, some control voltages are amplified.

5.7.6 Internal Calibration Network

During Autocal, the Internal Calibration Network in conjunction with circuits on other boards, makes various voltage and frequency measurements and stores correction data in memory. On power up, these correction values are recalled from memory and, via the Sample and Hold Network, routed to control circuits within the Model 95. Each of the test points may have more than one value; for example frequency related test points may have different values for different frequency ranges. Figure 5-11 illustrates the entire internal calibration network used with in the Model 95. The network shown can simply be thought of as a series of selector switches that ultimately route a single test point to the DVM. The calibration network consists of two parts: the voltage measurement section (schematic 1104-00-3395 sheet 2 of 10) and the frequency mea-

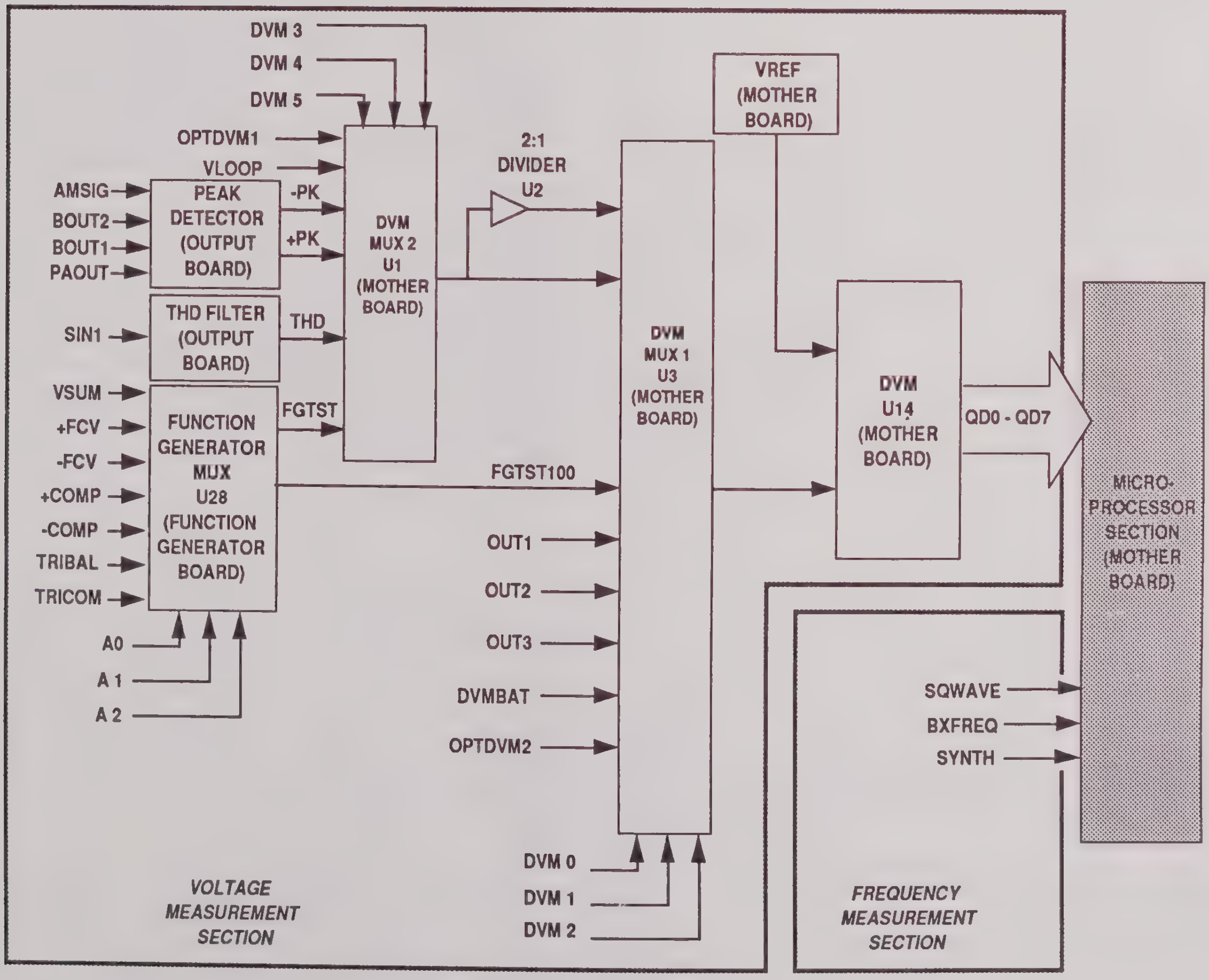

DVM 3
DVM 4
DVM 5
OPTDVM1
VLOOP
AMSIG
BOUT2
BOUT1
PAOUT
PEAK DETECTOR (OUTPUT BOARD)
-PK
+PK
DVM MUX 2 U1 (MOTHER BOARD)
2:1 DIVIDER U2
VREF (MOTHER BOARD)
SIN1
THD FILTER (OUTPUT BOARD)
THD
VSUM
+FCV
-FCV
+COMP
-COMP
TRIBAL
TRICOM
FUNCTION GENERATOR MUX U28 (FUNCTION GENERATOR BOARD)
FGTST
FGTST100
DVM MUX 1 U3 (MOTHER BOARD)
DVM U14 (MOTHER BOARD)
QD0 - QD7
MICRO-PROCESSOR SECTION (MOTHER BOARD)
A0
A 1
A 2
OUT1
OUT2
OUT3
DVMBAT
OPTDVM2
SQWAVE
BXFREQ
SYNTH
DVM 0
DVM 1
DVM 2
VOLTAGE MEASUREMENT SECTION
FREQUENCY MEASUREMENT SECTION

Figure 5-11. Internal Calibration

surement section (schematic 1104-00-3395 sheet 3 of 10). Both sections provide inputs to the Microprocessor section, or to be more specific, the Processor Support Chip.

The heart of the voltage measurement section is the DVM (U4 - Motherboard). The DVM receives a single dc voltage from the Multiplexer, Mux, (U3). The DVM is referenced to the +10Vdc voltage reference (U32 - schematic 1104-00-3395 sheet 8 of 10).

The DVM MUX 1 (U3 - schematic 1104-00-3395 sheet 2 of 10) selects one of its eight inputs for the DVM. Table 5-7 control lines, inputs and the function of the Mux inputs.

The DVM MUX 2 (U1 - Schematic 1104-00-3395 sheet 2 of 10) also selects one of eight inputs. But, its inputs originate on the Output, Phase Lock Loop, and Function Generator boards. Table 5-8 describes the inputs and the control lines (DVM3, DVM4, and DVM5) that

The function generator's Autocalibration circuit (schematic 1104-00-3342 sheet 4 of 7) consists of an analog multiplexer (U28) which selects one of eight test points on the function generator board. The amplifier, U29A buffers the multiplexer's output. Another amplifier, U29B, amplifies the lower level signals by X101. The two amplifier outputs (FSTST and FGTST100) drives the Internal Calibration Network's DVM MUX 2. Table 5-9 describes the inputs and the control lines (A0, A1, and A2) that selects them.

Table 5-7. DVM Mux 1

DVM0	DVM1	DVM2	Name	Function
0	0	0	OUT1	Unbalanced output from "Unbalanced Output and Impedance Network
1	0	0	OUT2	BAL OUT (+) from "Balanced Output Attenuator Network and Impedance Control
0	1	0	OUT3	BAL OUT (-) from "Balanced Output Attenuator Network and Impedance Control
1	1	0	FGTST100	Low level function generator measurements
0	0	1	DVM BAT	Measures memory back up battery voltage "Microprocessor Section
1	0	1	OPTDVM2	Identifies Options 001 /002.
0	1	1		Output from DVM MUX2. Voltages >+4V.
1	1	1		Output from DVM MUX2. Voltages <+4V.

Table 5-8. DVM Mux. 2

DVM3	DVM4	DVM5	Name	Function
0	0	0	FGTST	Output from Function Generator Mux U28 on Function Generator Board.
1	0	0	TEST IN	TP 1
0	1	0	+PK	Positive peak detector output from Output Board
1	1	0	THD	THD filter output from Output Board.
0	0	1	Ground	Circuit Common
1	0	1	-PK	Negative peak detector output from Output Board
0	1	1	VLOOP	Phase Lock Loop filter output from Phase Lock Loop Board
1	1	1	OPTDVM1	Not used in the Model 95

Table 5-9. Function Generator Mux.

A0	A1	A2	Name	Function
0	0	0	Ground	Analog Ground
1	0	0	VSUM	VCG Summing Amplifier Output from Function Generator Board.
0	1	0	+FCV	Positive Symmetry Control output from Function Generator Board.
1	1	0	-FCV	Negative Symmetry Control output from Function Generator Board.
0	0	1	+COMP	Positive Output from the High Frequency Compensation DAC on the Function Generator Board.
1	0	1	-COMP	Negative Output from the High Frequency Compensation DAC on the Function Generator Board.
0	1	1	TRIBAL	Triangle Buffer output from the Function Generator Board.
1	1	1	TRICOM	Triangle Buffer's Analog Ground from the Function Generator Board.

The Output Board's Peak Detector (schematic 1104-00-3335 sheet 6 of 6) selects and routes one of four voltages to the positive and negative Peak Detectors. The Peak Detectors consist of a positive half (U9A and U9D) and a negative half (U9B and U9C). Both detectors function the same, except for the polarity of the outputs, therefore only the positive peak detector will be described. Applying a positive voltage to U9A causes the amplifier's output to swing positive charging capacitor (C69) through diode (CR28). The amplifier (U9D) buffers the capacitor's voltage and provides feedback to the input amplifier (U9A). As the input voltage is reduced, the diode (CR28) becomes reversed biased and the capacitor (C69) holds a charge that represents the most positive (peak) voltage. The diode (CR35) provides local feedback to the input amplifier (U9A) while holding the peak. The transistor (Q20) discharges the capacitor (C69) when the PKRST line goes low which resets the peak detector. The relay (K7) bypasses the peak detector when the Internal Calibration Network measure dc voltages from the Output Board. Three switches (U8A - U8C) select the inputs to the peak detector. Table 5-10 describes the inputs and the control lines that selects them.

The THD Filter is a Twin Tee Notch filter that receives its input , SIN1, from the Sine Buffer on the Phase Lock Loop Board. The Filter (schematic 1104-00-3335 sheet 6 of 6) consists of the actual filter (U10B) and and rms Detector (U10A). The notch filter has a center frequency of about 10 kHz. The rms Detector provides a dc voltage proportional to the harmonics of the 10 kHz sine wave input.

The Frequency Measurement Section consists of three inputs to the Microprocessor Section; refer to paragraph 5.7.2.

Table 5-10. Peak Detector

Control Line	Input Name	Function
$\overline{\text{SELPRE}}$	AMSIG	Amplitude control signal from AM buffer from Phase Lock Loop Board.
$\overline{\text{SELBAL2}}$	BOUT2	Negative Balance Driver output from Output Board.
$\overline{\text{SELBAL1}}$	BOUT1	Positive Balance Driver output from Output Board.
$\overline{\text{SELPA}}$	PA OUT	Power Amplifier output from Output Board.

SECTION 6
MAINTENANCE

6.1 INTRODUCTION

This section presents information, which when used with the Verification Procedure (Section 3), the Circuit Description (Section 5), and the Schematic and Assembly Drawings (Section 7), returns the Model 95 to operating condition. This section covers:

Factory Service,
Problem Isolation
Disassembly and Reassemble - including board removal.

6.2 ROUTINE MAINTENANCE

Section 2 of this manual covers routine maintenance of the Model 95.

6.3 FACTORY SERVICE

Wavetek maintains a factory repair department for those customers not possessing the personnel or test equipment to troubleshoot the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the problem symptoms should be attached to minimize turnaround time.

Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
TWX: (910) 335-2007
FAX: (619) 595-9558

Before returning the instrument, call Wavetek's Customer Service department and obtain a Return Authorization Number; Wavetek uses this number to identify your instrument while it is in for repair.

The instrument should be packed according to the instructions in paragraph 2.3 of the *Model 95 Operator's Manual.*

6.4 BEFORE BEGINNING

Before beginning the troubleshooting process, verify that the instrument setup is correct. See section 3 of the *Model 95 Operator's Manual.*

Visually inspect the instrument for physical damage, paragraph 6.6.1.
Check the primary source:

1. Check the primary source.
2. Check the power cord.
3. Verify the primary supply voltage and the units voltage selection match; see paragraph 2.4.1 of the *Model 95 Operator's Manual.*
4. Check the unit's fuse; see paragraph 2.2 of this manual.

6.5 TROUBLESHOOTING PHILOSOPHY

The intent of this section is not to isolate failures to the component level but to give service technicians a set of "tools" that will guide them to the most likely circuit or circuits. From that point, the service technician must turn to the appropriate set of schematics and assembly drawings in the rear of this manual, and together with the circuit description (section 5) isolate the faulty component.

6.6 BEFORE TROUBLESHOOTING

6.6.1 Inspection

Before before beginning the troubleshooting procedure, use the following inspection procedures to locate obvious malfunctions with the Model 95.

1. Inspect all external surfaces of Model 95 for physical damage, breakage, loose or dirty contacts, and missing components.
2. Remove top cover, shield, and bottom cover to access components; paragraph 6.9.

WARNING

The Model 95 contains high voltages. After power is removed, discharge capacitors to ground before working inside the instrument to prevent electrical shock.

CAUTION

Do not disconnect or remove any board assemblies in the Model 95 unless the instrument is unplugged. Some board assemblies contain devices that can be damaged if the board is removed with the power on. Several components, including MOS devices, can be damaged by electrostatic discharge. Use conductive foam and grounding straps when servicing is required around sensitive components. Use care when unplugging ICs from high-grip sockets.

3. Inspect printed circuit board surfaces for discoloration, cracks, breaks, and warping.
4. Inspect printed circuit board conductors for breaks, cracks, cuts, erosion, or looseness.
5. Inspect all assemblies for burnt or loose components.
6. Inspect all chassis-mounted components for looseness, breakage, loose contacts or conductors.
7. Inspect the Model 95 for disconnected, broken, cut, loose, or frayed cables or wires.

6.6.2 Test Point Access

Test point access on the vertically mounted boards requires that, during signal tracing, a board be connected to the mother board through special extender cards.

Since only one board can be extended at a time and still allow access to components and test points, the person performing the troubleshooting should review the fault and the fault isolation steps logically to determine a plan that will require the least amount of board removal and reinstallation.

CAUTION

Do not install or remove vertical board assemblies from the mother board with the operating power ON. Damage to components on the assemblies will occur if the assemblies are removed or inserted with operating power on.

CAUTION

Before removing Arb board, disconnect cables which are attached to board through holes in the rear shield.

Test points called out in the following procedures are shown on the assembly drawings and the schematic diagrams for each vertical board and the mother board. Three types of test points are shown. Numbered test points which are actual reference designator components on the board, and numbered test points which are locations on components that have been added as an aid in fault isolation. The final test points are actually pins on ICs and connectors.

Some circuits on the mother board and the phase lock loop board are shielded by rectangular metal cans soldered to the board traces. Test points located under these shields must be accessed from the solder side of the boards. Do not remove the shields except if repair is required in the shielded area.

6.6.3 Board Location

Figure 6-1 shows the location of the board assemblies in the Model 95.

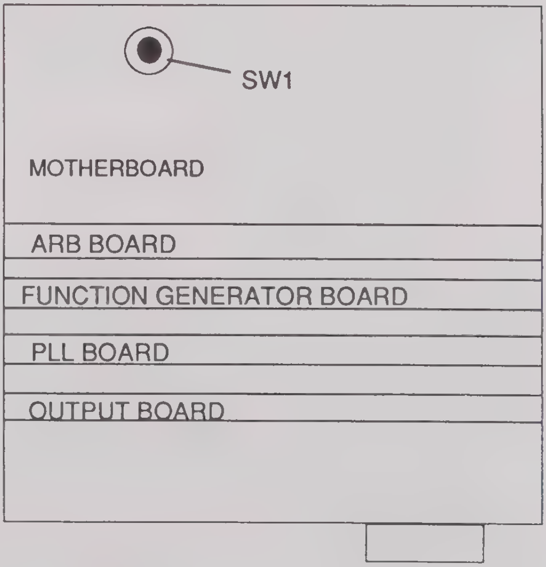


Figure 6-1. Board Locations

6.7 FAULT ISOLATION

This paragraph provides a series of procedures that when followed will point to recommended circuit blocks. Skip those procedures that do not apply to your symptom. Each circuit block reference will contain additional references to the proper Circuit Description paragraphs and Schematic and Assembly drawings. Use the circuit descriptions in conjunction with the schematics to gain a deeper understanding of the circuit block. Table 6-1 lists the recommended equipment necessary to troubleshoot the Model 95.

Table 6-1. Recommended Equipment

Equipment	Requirements
Scope	Dual trace, 20 MHz Bandwidth
Digital Voltmeter	Three Digit Accuracy (minimum).
Frequency Counter	>Four Digits of resolution, <±10 ppm accuracy. (Synthesizer and Optional Frequency Reference.
Board Extender Kit	Wavetek part number 1100-00-3411

6.7.1 Front Panel Not Active - Neither the front panel's display, annunciators, or keyboard operate.

1. Check the primary source; paragraph 6.4.
2. Visually inspect the unit; paragraph 6.6.

Secondary Supplies

1. Remove the top cover (see paragraph 6.9.1 - Top Cover/Shield Removal)
2. Check the unit's secondary supplies using the digital voltmeter. Table 6-2 lists the power supplies, their voltages and tolerances, as well as drawing references. Test Points are located on the Motherboard. All voltages are referenced to analog ground (TP6). Also check the power supplies distribution system.

Power Supplies check OK.

1. Check the Microprocessor Section: Schematic 1104-00-3395 Sheet 3 of 10, Assembly drawing 1101-00-3395 sheet 1 of 3. For a description of the Microprocessor Section's circuits, refer to paragraph 5.7.2.
2. Check the microprocessor section: paragraph 6.8.16.

HINTS

Check the supply voltages to the circuits within the Microprocessor Section. Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

3. If the key pad and display still do not operate, check the front panel input decoder, U4. Refer to schematic 0103-00-3001 sheet 3 of 3, assembly drawing 1101-00-3322 sheet 1 of 2, circuit description paragraph 5.7.4.5.

6.7.2 Front Panel Not Active - Keyboard Does Not Work

1. Refer to schematic 1104-00-3322, assembly drawing 1101-00-3322 sheet 1 of 2, and circuit description paragraph 5.7.4.5 - Keyboard.
2. Check the supply voltages to the circuits within the Keyboard.
   Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

6.7.3 Front Panel Not Active - Display Does Not Work

1. Refer to schematic 1104-00-3322, assembly drawing 1101-00-3322 sheet 1 of 2, and circuit description paragraph 5.7.4.5 - Display.
2. Check the supply voltages to the circuits within the Display.
   Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

Table 6-2 Power Supply Test Points

Test Point	Supply Voltage	Tolerance	Schematic Drawing	Assembly Drawing
JMP 4	+12VDC	±0.2 Vdc	1104-00-3395 Sheet 8 of 10	1101-00-3396 Sheet 1 of 3
JMP 5	-12VDC	±0.2 Vdc	1104-00-3395 Sheet 8 of 10	1101-00-3396 Sheet 1 of 3
JMP 6	+5V	±0.2 Vdc	1104-00-3395 Sheet 8 of 10	1101-00-3396 Sheet 1 of 3
TP14	+24 VDC	±0.2 Vdc	1104-00-3395 Sheet 9 of 10	1101-00-3396 Sheet 1 of 3
TP15	-24VDC	±0.2 Vdc	1104-00-3395 Sheet 9 of 10	1101-00-3396 Sheet 1 of 3

6.7.4 Front Panel Not Active - Annunciators Do Not Work

1. Refer to schematic 1104-00-3322, assembly drawing 1101-00-3322 sheet 1 of 2, and circuit description paragraph 5.7.4.5 - Annunciator Circuit.
2. Check the supply voltages to the circuits within the Display.
   Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

6.7.5 Self Test and Self Test Error Messages

When power is first applied, the Model 95 performs Self Test. Self test checks the unit's internal battery, Motherboard memory, and storage memory. Failure of any of the tests will cause the Model 95 to display an error message. Table 6-3 defines the error messages. If Self Test is successful, the Model 95 will display "Wavetek Model 95".

6.7.6 AutoCal and AutoCal Error Messages

The Model 95 contains a powerful fault isolation tool: AutoCal. AutoCal measures numerous "test points" in the Model 95. It compares these measurements against either a frequency standard or voltage standard. AutoCal attempts to make correction for any deviations. But if AutoCal can not bring the measurement within limits, the Model 95 produces an error message. The Model 95 runs AutoCal until it hits its first error. Then it stops until the error is fixed by either performing the Calibration procedure, section 5, or isolating and fixing the problem. Continue running AutoCal until all problems have been identified and fixed.

To AutoCal the Model 95, perform the following steps. AutoCal requires no external test equipment. In fact, test equipment should not be connected to the Model 95's input connectors, otherwise the AutoCal could alter the calibration of the instrument. Also, disconnect all outputs from the instrument otherwise the sudden changes in the instrument's output waveforms could damage external equipment.

1. Turn on the Model 95 and allow it to warm up for 20 minutes. Pressing the CALIBRATE key during the 20 minute warm up time displays the count-down time, after the 20 minutes the Model 95 begins AutoCal. Pressing any other key during the count down aborts AutoCal and returns the instrument to normal operation.

REMEMBER
Remove all input and output connections to the Model 95 before pressing AutoCal.

2. After a 20 minute warm up, press the SHIFT and CALIBRATE key and allow the unit time to complete the AutoCal cycle. While running AutoCal, the Model 95 displays "CALIBRATING". When completed successfully, the Model 95 displays "AUTOCALIBRATED". Then the unit returns to its last operational setup. If the AutoCal fails the Model 95 displays an error message which identifies the parameter - ERR (*Keyword*); for example ERR VSINCAL. If this occurs occasionally, try to AutoCal the unit again. Note the error keywords and report the errors when the unit is returned for scheduled maintenance.

Following is a listing of the AutoCal error messages. Included is a brief description of the AutoCal step. In addition, each step contains Pass/Fail instructions.

Table 6-3. Self Test Error Messages

Display	Probable Cause	Corrective Action
Err xxxxxxxxx	Improper self-check/unit	Press POWER key OFF and then ON. If identical failure error is displayed, refer to paragraph 6.7.1 - Power Supplies Check OK. If a different error is displayed, press the Calibrate key again. If "WAVETEK MODEL 95" is displayed, the unit is operational.
Low batt x.xxx v	Internal battery voltage low.	Unit is available for immediate operation. Refer to paragraph 2.3 for battery replacement.
Cal Required	Internal battery dead.	Unit has lost its calibration data but can be used after performing and passing AutoCal. Instrument may not meet all specifications.

VCG0	This check adjusts out frequency shift error in the function generator. The test sets the generator to 200 Hz on the 200 kHz range and using the internal calibration network adjusts out 1000:1 frequency errors (<0.7 Hz deviation). **Passes:** Verifies the function generator operates correctly. No message will be displayed and AutoCal moves to the next step. **Fail:** If the unit displays the VCGO message which means the Function Generator may not be working correctly. Use the procedure in paragraph 6.8.1 to isolate the faulty circuit.
VFREQ0	This check zeros the VCG summing amplifier with the VFREQ input connected. It also zeros the Function Generator board's Auto Cal circuit. Test requires the VSUM voltage be <20 mV of analog ground. **Passes:** Verifies the VCG Summing Amplifier and Auto Calibration circuit operates correctly. No message will be displayed and AutoCal moves to the next step. **Fail:** If the unit displays the VFREQ0 message which means the VCG Summing Amplifier or Auto Cal circuit may not be working correctly. Use the procedure in paragraph 6.8.1 to check the VCG Summing Amplifier. Use paragraph 6.8.9 to check the function generator's AutoCal circuit.
VFREQ0 SCL	This check zeros the VCG Summing amplifier with the VFREQ input disconnected. It also zeros the Function Generator board's Auto Cal circuit. Test requires the VSUM voltage be <10 mV of analog ground. **Passes:** Verifies the VCG summing Amplifier and Auto Calibration circuit operates correctly. No message will be displayed and AutoCal moves to the next step. **Fail:** If the unit displays the VFREQ0 message which means the VCG summing amplifier or AutoCal circuit may not be working correctly. Use the procedure in paragraph 6.8.1 to check the VCG summing amplifier.
S+VCGOFF	This check zeros (<20 mV) the positive symmetry control relative to the analog ground. **Passes:** Verifies the positive symmetry control works. No message will be displayed and AutoCal moves to the next step. **Fails:** Check the Symmetry Control, paragraph 6.8.3.
S–VCGOFF	This check zeros (<20 mV) the negative symmetry control relative to the analog ground. **Passes:** Verifies the negative symmetry control works. No message will be displayed and AutoCal moves to the next step. **Fails:** Check the Symmetry Control, paragraph 6.8.3.
VTRIBAL	This check zeros (<59 mV) the triangle buffer, TRIBAL, relative to analog ground, TRICOM. **Passes:** Verifies the triangle buffer works. No message will be displayed and AutoCal moves to the next step.. **Fails:** Check the Triangle Buffer and Comparator, paragraph 6.8.2.
SYMM50PCT	This check sets the symmetry control to 50%, symmetry off, and adjusts for 50% ±0.03% symmetry at 201 Hz on the 200 kHz range. **Passes:** Verifies the symmetry control and current sources work. No message will be displayed and AutoCal moves to the next step. **Fails:** Check the symmetry control (paragraph 6.8.3) and current sources (paragraph 6.8.4).
+VCGOFF	This check turns on the symmetry, sets the symmetry to 50%, and adjust the symmetry to 50%. **Passes:** Verifies the symmetry control and current sources work. No message will be displayed and AutoCal moves to the next step. **Fails:** Check the symmetry control, paragraph 6.8.3.

SWPLENGTH	This check sets VSLEN (sweep length) DAC reference input and adjusts the sweep DAC to a specified frequency. **Passes:** Verifies the sweep generator works. No message will be displayed and AutoCal moves to the next step. **Fails:** Check the Sweep Generator, paragraph 6.8.10.
SCALE	This check sets VFREQ input to the VCG summing amplifier to a level that when the Scale switch is open causes the function generator to produces a 20 kHz signal. The internal calibration network adjusts VFREQ to 20 kHz ± 1Hz **Passes:** Verifies the frequency accuracy at 1000:1 on the 20 MHz range. No message will be displayed and AutoCal moves to the next step. **Fails:** Check the function generator, paragraph 6.8.1. Also check the *DAC* Sample and Hold Network, paragraph 6.8.17.
TOFR7	This check sets the function generator to the 200 kHz range. The internal calibration network measures and adjusts VFREQ to 200 kHz ± 10 Hz. **Passes:** Verifies the frequency accuracy at the top of the 200 kHz range. No message will be displayed and AutoCal moves to the next step. **Fails:** Check Frequency Range Switch Circuit, paragraph 6.8.7. Also check the function generator, paragraph 6.8.1.
TOFR6	This check sets the function generator to the 20 kHz range. The internal calibration network measures and adjusts VFREQ to 20 kHz ± 1Hz. **Passes:** Verifies the frequency accuracy at the top of the 20 kHz range. No message will be displayed and AutoCal moves to the next step. **Fails:** Check Frequency Range Switch Circuit, paragraph 6.8.7. Also check the function generator, paragraph 6.8.1.
TOFR5	This check sets the function generator to the 2kHz range. The internal calibration network measures and adjusts VFREQ to 200 kHz ±0.15 Hz. **Passes:** Verifies the frequency accuracy at the top of the 2kHz range. No message will be displayed and AutoCal moves to the next step. **Fails:** Check Frequency Range Switch Circuit, paragraph 6.8.7. Also check the function generator, paragraph 6.8.1.
TOFR4	This check sets the function generator to the 200 Hz range. The internal calibration network measures and adjusts VFREQ to 200 Hz ±0.01 Hz. **Passes:** Verifies the frequency accuracy at the top of the 200 Hz range, and verifies the operation of the capacitance multiplier. No message will be displayed and AutoCal moves to the next step. **Fails:** Check the capacitance multiplier, paragraph 6.8.8. Also check the function generator, paragraph 6.8.1.
TOFR3	This check sets the function generator to the 20 Hz range. The internal calibration network measures and adjusts VFREQ to 20 Hz ±0.02 Hz. **Passes:** Verifies the frequency accuracy at the top of the 20 Hz range, and verifies the operation of the capacitance multiplier. No message will be displayed and AutoCal moves to the next step. **Fails:** Check the capacitance multiplier, paragraph 6.8.8. Also check the function generator, paragraph 6.8.1.
COMP9+	This check sets the function generator to 20 MHz range. Then sets VFREQ to 2MHz. Next the VFREQ value is set for 20 MHz, and the high frequency DAC adjusted for 20 MHz. The cycle repeats for up to 20 iterations. **Passes:** Verifies the 20 MHz range 10:1 frequency linearity. No message will be displayed and AutoCal moves to the next step. **Fails:** Check the high frequency com-

pensation circuit, paragraph 6.8.6. Also check the function generator, paragraph 6.8.1.

COMP8+ This check sets the function generator to 2MHz range. Then it sets VFREQ to 200 kHz. Next the VFREQ value is set for 2MHz, and the high frequency DAC adjusted for 2MHz. The cycle repeats for up to 20 iterations.
Passes: Verifies the 2MHz range 10:1 frequency linearity. No message will be displayed and AutoCal moves to the next step.
Fails: Check the high frequency compensation circuit, paragraph 6.8.6. Also check the function generator, paragraph 6.8.1.

FINDNOTCH This check sets the function generator to a 10 kHz sine wave. Then using the notch filter and internal calibration network adjusts the frequency (VFREQ) to 10 kHz.
Passes: Verifies the sine convertor and buffer, variable supply, and notch filter operates correctly. No message will be displayed and AutoCal moves to the next step.
Fails: Check the Sine Buffer, Sine Converter, and Variable Supply. See paragraph 6.8.11.

OFSTZERO This check sets the function to dc and the offset voltage to 0Vdc. Then measuring the power amplifiers output with the internal calibration network adjusts the offset (VOFST) to <9 mV.
Passes: Verifies the operation of the power amplifier. No message will be displayed and AutoCal moves to the next step.
Fails: Check the power amplifier; see paragraph 6.8.14. Also, check the DAC Sample and Hold Network, paragraph 6.8.17.

OFSTGAIN This check sets the function to dc and the offset voltage to 5Vdc. Then measuring the power amplifiers output with the internal calibration network adjusts the offset gain (VOFST) to +5Vdc ±9mV.
Passes: Verifies the operation of the power amplifier. No message will be displayed and AutoCal moves to the next step.
Fails: Check the power amplifier; see paragraph 6.8.14. Also check the DAC Sample and Hold Network, paragraph 6.8.17.

BALOFFST This check sets the function to dc and the offset voltage to 0Vdc. The internal calibration network measures the two balanced outputs and adjusts the offset voltage (VOFST) so the difference between the two outputs is <3 mVdc.
Passes: Verifies the operation of the balanced drivers. No message will be displayed and AutoCal moves to the next step.
Fails: Check the balanced drivers, paragraph 6.8.14.

SINEAMPL This check sets the function to sine wave and using the peak detector, measures the peak to peak amplitude of the sine wave, and adjusts amplifier output via VAMCAL to 20 ±0.03 Vpp.
Passes: Verifies the operation of the function selector, preamplifier and multiplier, and AM buffer. No message will be displayed and AutoCal moves to the next step.
Fails: Check the function selector (paragraph 6.8.14), preamplifier/multiplier (paragraph 6.8.14), and AM buffer (paragraph 6.8.14).

TRIAMPL This check sets the function to triangle wave and using the peak detector, measures the peak to peak amplitude of the triangle wave, and adjusts amplifier output via VAMCAL to 20 ±0.03 Vpp.
Passes: Verifies the operation of the function selector, preamplifier and multiplier, and AM buffer. No message will be displayed and AutoCal moves to the next step.
Fails: Check the function selector (paragraph 6.8.14), preamplifier/multiplier (paragraph 6.8.14), and AM buffer (paragraph 6.8.14).

SQURAMPL This check sets the function to square wave and using the peak detector, measures the peak to peak amplitude of the square wave, and adjusts amplifier output via VAMCAL to 20 ±0.03 Vpp.

Passes: Verifies the operation of the function selector, preamplifier and multiplier, and AM buffer. No message will be displayed and AutoCal moves to the next step.

Fails: Check the function selector (paragraph 6.8.14), preamplifier/multiplier (paragraph 6.8.14), and AM buffer (paragraph 6.8.14).

BALAMPL This check adjusts the balanced output amplitude to 20 ±0.03 Vpp by measuring the balanced driver output with the peak detector and varying VAMCAL.

Passes: Verifies the operation of the balanced drivers. No message will be displayed and AutoCal moves to the next step.

Fails: Check the balanced drivers, paragraph 6.8.14. Also, check the -20 dB Attenuator, paragraph 6.8.14.

VSINCAL This check sets the function generator to a 10 kHz sine wave. Then using the notch filter and internal calibration network adjusts the sine wave harmonic distortion.

Passes: Verifies the sine convertor and buffer, variable supply, and notch filter operates correctly. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Sine Buffer, Sine Converter, and Variable Supply. See paragraph 6.8.11.

ARBAMPL This check sets the function to Arb square wave and, using the peak detector, measures the peak to peak amplitude of the Arb square wave, and adjusts amplifier output via VAMCAL to 20 ±0.03 Vpp.

Passes: Verifies the operation of the Arbitrary waveform generator, function selector, preamplifier and multiplier, and AM buffer. The Model 95 has completed the AutoCal cycle.

Fails: Check the Arbitrary waveform generator (paragraph 6.8.13), function selector (paragraph 6.8.14), preamplifier/multiplier (paragraph 6.8.14), and AM buffer (paragraph 6.8.14).

6.8 BLOCK ISOLATION

The following procedures provide a method of isolating faulty circuit blocks. Most steps use test points; see paragraph 6.6.2.

6.8.1 Function Generator

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheets 2 through 7) in section 7 of this manual. Also, refer to paragraph 5.2 of this manual. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First check the function generator board's power input. Schematic 1104-00-3342 sheet 1.

TP20	+5 Vdc
TP23	-12 Vdc
TP25	+24 Vdc
TP26	-24 Vdc

2. Check the following test points which will step you forward through the function generator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

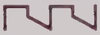
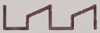
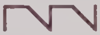
22	VLOOP	Locked: +0.1 Vdc. Unlocked: -0.5 Vdc.	
TP2	VSUM	-2 Vdc	
TP4	-FCV	-4 Vdc.	
TP3	+FCV	+4 Vdc	
U22A-1		+COMP	≈+2.6 Vdc
U22B-7		-COMP	≈-2.6 Vdc
TP6	VI+	+17 Vdc.	
TP7	VI-	-17 Vdc.	
TP9	TRINODE	2.5 Vpp Triangle @ 1kHz.	
TP12	TRIOUT	2.5 Vpp triangle @1kHz.	
TP15	SQWAVE	2.25 Vpp square @ 1kHz.	

6.8.2 Triangle Buffer/Comparator

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheets 6 and 7) in section 7 of this manual. Also, refer to paragraph 5.2.2 - Comparator and Triangle Buffer. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the triangle buffer and comparator circuits using paragraph 6.8.1.
2. Check the following test points which will step

you through the triangle buffer and comparator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

28	ISWITCH+	 3.5 Vpp @ 1kHz.
29	ISWITCH–	 3.5 Vpp @ 1kHz.
TP9	TRINODE	2.5 Vpp Triangle @ 1kHz
TP12	TRIOUT	2.5 Vpp Triangle @ 1kHz.
27	TRI/SQR	 2.5 Vpp @ 1kHz.
18	SQ1	1Vpp square offset +8Vdc @ 1kHz.
19	SQ2	4Vpp Square @ 1kHz.
TP15	SQWAVE	2.5 Vpp Square @ 1kHz.
TP13	REFSQR	2.5 Vpp square @ 1kHz.

6.8.3 Symmetry Control

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 3) in section 7 of this manual. Also, refer to paragraph 5.2.4. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1.
2. Check the following test points which will step you through the symmetry control circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP2	VSUM	-2 Vdc.
21	DAC ref	-6 Vdc
TP3	+FCV	+4 Vdc
TP4	-FCV	-4 Vdc

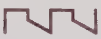
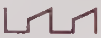
3. Verify the data line "wiggle". U12, pins 9, 10, 11, 12, 13, 14, 15, and 16. U17, pins 9, 10, 11, 12, 13, 14, 15, and 16. The following table identifies the enable DAC.

	DS1	**DS2**	**A/B**
Pin #	**19**	**20**	**17**
U7C Enabled	1	0	1
U7D Enabled	1	0	0
U12B Enabled	0	1	0
U12A Enabled	0	1	1

6.8.4 VCG Current Sources

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 3) in section 7 of this manual. Also, refer to paragraph 5.2.2, VCG Current Sources. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1.
2. Check the following test points which will step you through the symmetry control circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP3	+FCV	+4 Vdc.
TP5	+VCG	+19 Vdc.
TP6	VI+	+17 Vdc.
28	ISWITCH+	 3.5 Vpp @ 1kHz.
TP4	-FCV	-4 Vdc.
TP8	-VCG	-19 Vdc.
TP7	-VI	-17 Vdc.
29	ISWITCH–	 3.5 Vpp @ 1kHz.

6.8.5 Trigger Baseline Compensation

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 4) in section 7 of this manual. Also, refer to paragraph 5.2.5, Trigger Baseline Compensation. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1. Note, if the generator does not run, check this circuit.
2. Check the following test points which will step you through the trigger baseline compensation circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

U19-3	VSOURCE	+17 Vdc
TP5	+VCG	+19 Vdc
TP8	-VCG	-19 Vdc
17	RUN	+4 Vdc for continuous. 0Vdc off.
TP9	TRINODE	2.5 Vpp

6.8.6 High Frequency Compensation

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 4) in section 7 of this manual. Also, refer to paragraph 5.2.5. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1.
2. Check the following test points which will step you through the high frequency circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP3	+FCV	+4 Vdc
U12C-2	Vref	-5 Vdc
U22A-1	+COMP	≈+2.6 Vdc
TP4	-FCV	-4 Vdc
U12A-8	Vref	+5 Vdc
U22B-7	-COMP	≈-2.6 Vdc

3. Verify the data lines "wiggle". U12, pins 9, 10, 11, 12, 13, 14, 15,. The following material identifies

the enabled DAC.

	DS1	DS2	A/B
Pin #	**19**	**20**	**17**
U12C Enabled	1	0	1
U12D Enabled	1	0	0

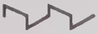
6.8.7 Frequency Range Switches

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 5) in section 7 of this manual. Also, refer to paragraph 5.2.2, Frequency Range Capacitors and Ranges. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the frequency range capacitor circuit using paragraph 6.8.1.
2. Check the test point, TP9 - TRINODE, for a 2.5 Vpp triangle @ 1kHz.
3. Verify the following frequency range control lines are low: $\leq\overline{\text{FR5}}$, $\leq\overline{\text{FR6}}$, $\leq\overline{\text{FR7}}$ $\leq\overline{\text{FR8}}$. Note, in the default settings, the 2kHz to 200 Hz range is selected. For all frequencies above 200 Hz, refer to the control lines and capacitors listed in table 6-4..

6.8.8 Capacitance Multiplier

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 6) in section 7 of this manual. Also, refer to paragraph 5.2.2, Capacitance Multiplier. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First verify the function generator operates correctly using paragraph 6.8.1.
2. Change the unit's frequency to 100 Hz. Check the test point, TP11 - CAP MULT, for  5Vpp @ 100 Hz.

   Also verify the 2KHz range capacitor is selected: 0.52219 µF - C52, C53,C55,C57, C58, C67 ($\leq\overline{\text{FR5}}$, $\leq\overline{\text{FR6}}$, $\leq\overline{\text{FR7}}$ $\leq\overline{\text{FR8}}$)

   For frequencies below 200 Hz, refer to the control lines and capacitors listed in table 6-5.

6.8.9 Function Generator Auto Calibration

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 4) in section 7 of this manual. Also, refer to paragraph 5.7.6 This circuit is active only when AutoCal is being performed. The following describes the function generator auto cal mux controls.

	A0	A1	A2	Name
U28 Pin	**1**	**16**	**15**	
	0	0	0	Ground
	1	0	0	VSUM
	0	1	0	+FCV
	1	1	0	-FCV
	0	0	1	+COMP
	1	0	1	-COMP
	0	1	1	TRIBAL
	1	1	1	TRICOM

6.8.10 Sweep Generator

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 2) in section 7 of this manual. Also, refer to paragraph 5.5.3 Reset the unit by pressing SHIFT and RESET ALL keys.

1. First verify the function generator operates correctly using paragraph 6.8.1.
2. Select the sweep mode.
3. Check the following test points which will step you through the sweep generator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

J6-39	VSLEN	
U7A-8	Vref	-3 x (VSLEN)
U8-6	Sweep Out	Approx. 3 x (VSLEN)

Check the sweep DAC.

	DS1	DS2	A/B
Pin #	**19**	**20**	**17**
U7A Enabled	0	1	1

Verify the DAC data lines (U7 - 9, 10, 11, 12, 13, 14, 15, and 16) step from 00000000 to 11111111.

Table 6-4. Frequency Range Switches

Range	Capacitors	Control
20 - 2 MHz	50 pF - (15 pF + Stray) C67	None
2MHz - 200 kHz	490 pF - C57, C58, C67	$\leq\overline{\text{FR8}}$
200 kHz - 20 kHz	0.00519 µF - C55,C57, C58, C67	$\leq\overline{\text{FR7}}$, $\leq\overline{\text{FR8}}$
20 kHz - 2kHz	0.05219 µF - C53,C55,C57, C58, C67	$\leq\overline{\text{FR6}}$, $\leq\overline{\text{FR7}}$, $\leq\overline{\text{FR8}}$
2kHz - 200 Hz	0.52219 µF - C52, C53,C55,C57, C58, C67	$\leq\overline{\text{FR5}}$, $\leq\overline{\text{FR6}}$, $\leq\overline{\text{FR7}}$ $\leq\overline{\text{FR8}}$

Table 6-5. Capacitance Multiplier

Range	Capacitors	Control
200 Hz - 20 Hz	10 kΩ - R67	$\overline{FR4}$
20Hz - 2Hz	110 kΩ - R67, R68	$\overline{FR4}$, $\overline{FR3}$
2Hz - 200 mHz	1.11 MΩ - R67, R68, R69	$\overline{FR4}$, $\overline{FR3}$, $\overline{FR2}$
200 mHz - 20 mHz	11.11 MΩ - R67, R68, R69, R71	All high
20 mHz - 2mHz	See Note	

Note

The Model 95 does not switch to the 20 mHz range. It actually keeps the same range capacitors as the 200 mHz range, but it decreases the input to the VCG Summing Amplifier by 1/10th effectively dropping down a decade range by switching in, $\overline{\text{SCALE}}$, an additional input resistor (R8) in series with the VFREQ input.

4. Check the Sweep Out (Ramp) generator test points.

U7A-21	Vref	-6 Vdc
SWEEP OUT Connector		0 to +5V linear ramp.

Check the Sweep Out DAC.

	DS1	DS2	A/B
Pin #	**19**	**20**	**17**
U7A Enabled	0	1	0

Verify the DAC data lines (U7 - 9, 10, 11, 12, 13, 14, 15, and 16) step from 00000000 to 11111111.

6.8.11 Sine Convertor, Buffer, and Variable Supply

Refer to the Phase Lock Loop assembly drawing (1101-00-3341) and schematic (1104-00-3341 sheets 5 and 6) in section 7 of this manual. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First verify the function generator operates correctly using paragraph 6.8.1.
2. Check the following test points which will step you through the sine wave circuits. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

25	TRISIG	2.5 Vpp triangle @ 1kHz.
27	SINSIG	2.5 Vpp triangle @ 1kHz.
TP13	SINCO	0.6 Vpp sine @ 1kHz.
TP10	SIN	2 Vpp sine @ 1kHz.
TP14	+12VADJ	Approximately +12 Vdc.
TP15	-12VADJ	Approximately -12 Vdc.

6.8.12 Mode Control and Burst Counter

Refer to the Arb board assembly drawing (1101-00-3327) and schematic (1104-00-3327 sheet 2) in section 7 of this manual. Reset the unit by pressing SHIFT and RESET ALL keys.

1. Check the test point, TP3 - RUN, +4 Vdc.
2. Select the Triggered Mode. Check the test point, TP3 - RUN, 0Vdc. Press the Man Trig key on the front panel. TP3 toggles to +4 Vdc and returns to 0Vdc.
3. Refer to paragraph 5.6 for a detailed description of the mode control and burst counter circuits.

6.8.13 Arbitrary Waveform Generator

Refer to the Arb board assembly drawing (1101-00-3327) and schematic (1104-00-3327 sheets 3, 4, and 5) in section 7 of this manual. Also refer to the circuit description, paragraph 5.3 of this manual. Reset the unit by pressing SHIFT and RESET ALL keys.

1. Using the block edit mode *(*paragraph 3.5.19.7 of the *Model 95 Operators Manual)*, place a Arb square wave in the active memory at full amplitude. Set the waveform frequency to 1kHz.
2. Check the test points in table 6-6 which will step you through the Arb waveform generator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

3. Check the following test points which will step you through the Arb waveform generator's RAM battery control (schematic 1104-00-3327 sheet 7). If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

16	+5PV	≈+5 Vdc
TP14	VBAT1	+3.5 Vdc

6.8.14 Output Section

This procedure steps through each block of the output block. Refer to the Output board assembly drawing (1101-00-3335), Motherboard assembly drawing (1101-00-3395), Output board schematic (1104-00-3335) , and Motherboard schematic (1104-00-3395 sheet 7) in section 7 of this manual. Also, refer to the output section circuit description, paragraph 5.4.

Check the following test points which will step you through the output section. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

1. Square Shaper (schematic 1104-00-3335 sheet 2). Reset the unit by pressing SHIFT and RESET ALL keys.

Q2 base		SQRON≈0Vdc

Select Square function.

Q2 base		SQRON>+2.5Vdc
JMP1	SQWAVE	2.25 Vpp square @ 1kHz.
TP1	2V P-P SQUARE	1Vpp square @ 1kHz.

2. Function Selector (schematic 1104-00-3335 sheet 3). Reset the unit by pressing SHIFT and RESET ALL keys.

19	PREAMPIN	1Vpp square @ 1kHz.

Select Sine function

19	PREAMPIN	1Vpp sine @ 1kHz.

Select Triangle function

19	PREAMPIN	1Vpp triangle @ 1kHz.

On the Phase Lock Loop Board, (schematic 1104-00-3341 sheet 4),

26	TRIOUT	1.5 Vpp triangle @ 1kHz.

Select Arb Square

See paragraph 6.8.13.

3. Preamplifier and Multiplier (schematic 1104-00-3335 sheet 3). Reset the unit by pressing SHIFT and RESET ALL keys.

19	PREAMPIN	1Vpp sine @ 1kHz.
TP11	+6V	+6 Vdc
TP12	-6V	-6 Vdc
TP2	PREOUT	1.5 Vpp sine @ 1kHz offset +4 Vdc.

4. AM Summing Amplifier (schematic 1104-00-3341 sheet 6). Reset the unit by pressing SHIFT and RESET ALL keys.

16	VAMCAL	Approximately 1.55 Vdc.
TP12	AMSIG	-1.5 Vdc.

5. Power Amplifier (schematic 1104-00-3335 sheet 4). Reset the unit by pressing SHIFT and RESET ALL keys.

TP2	PREOUT	1.5 Vpp sine @ 1kHz offset +4 Vdc.
17	+22V	+22 Vdc
16	-22V	-22 Vdc
TP4	PA_OUT	8Vpp sine @ 1kHz.

6. -20 dB Attenuator (schematic 1104-00-3335 sheet 5). Reset the unit by pressing SHIFT and RESET ALL keys.

TP4	PA_OUT	8Vpp sine @ 1kHz.
20	UBOUT	5Vpp sine into 50Ω (10 Vpp unterminated).

7. Unbalanced Output Attenuator Network and Impedance Control (schematic 1104-00-3395 sheet 7). Reset the unit by pressing SHIFT and RESET ALL keys. Turn the Output On.

P11-1	UBOUT	5Vpp sine into 50Ω (10 Vpp unterminated).
Unbalanced Output connector		5Vpp sine into 50Ω (10 Vpp unterminated).

8. Balanced Drivers (schematic 1104-00-3335 sheet 5). Reset the unit by pressing SHIFT and RESET ALL keys. Select the 600Ω Balanced Output . Turn the output On.

18	Bal In	5Vpp sine @ 1kHz.
TP6	BOUT2	5Vpp sine @ 1kHz.
TP7	BOUT1	5Vpp sine @ 1kHz.

Table 6-6. Arb Test Points

Test Point	Name	Conditions
Arb Board		
TP1	ACK1	4Vpp square @ sample frequency. Sample frequency = # of points between the start and stop addresses multiplied by the waveform frequency.
TP5	-5V Supply	-5 Vdc.
20	-1.2VREF	-1.2 Vdc.
21	VREF	+5 Vdc.
TP6	UNFILTER OBSIG	1Vpp Arb square wave @ 1kHz.
TP7	50K FILT	1Vpp Arb square wave @ 1kHz with filtering.
TP8	5M FILT	1Vpp Arb square wave @ 1kHz with filtering.
Output board		
TP2	PREOUT	1.5 Vpp Arb square offset +4 Vdc @ 1kHz.

9. Balanced Output Attenuator Network and Impedance Control (schematic 1104-00-3395 sheet 7). Reset the unit by pressing SHIFT and RESET ALL keys. Select the 600Ω Balanced Output. Turn the output On.

On the Output board, check:

TP6	BOUT2	5Vpp sine @ 1kHz.
TP7	BOUT1	5Vpp sine @ 1kHz.

On the Motherboard, check:

J21	BAL OUT (-)	5Vpp sine terminated.
J20	BAL OUT (+)	5Vpp sine terminated.

6.8.15 Frequency Synthesizer and Phase Lock Loop

This procedure steps you through the frequency synthesizer and phase lock loop. Also, refer to paragraph 5.5.4. Refer to the following drawings:

Motherboard assembly drawing 1101-00-3395.
Motherboard schematic 1104-00-3395 sheet 4.
Phase Lock Loop assembly drawing 1101-00-3341
Phase Lock Loop schematic 1104-00-3341 sheets 2 and 3.

Reset the unit by pressing SHIFT and RESET ALL keys.

1. Check the following test points on the frequency synthesizer (schematic 1104-00-3395 sheet 4). If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

18	OSCIN	3.5 Vpp square @ 500 kHz.
TP5	VC LOOP	+3 Vdc Locked, and +5 Vdc Unlocked.
TP17	SYOUT	┬┬┬ 4Vp TTL 50 ns pulses @ 1kHz.

2. Check the following test points on the phase lock loop (schematic 1104-00-3341 sheets 2, 3, and 4). If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP3	SYNTH	┬┬┬ ≈4Vp TTL 50 ns pulses @ 1kHz.
TP1	Z-CROSS	≈5Vpp Square @ 1kHz.
19	SQWAVE	≈3 Vpp Square @ 1kHz
20	1Y	┬┬┬ ≈4Vp pulses
21	2Y	≈3 Vpp square
22		3.5 Vp pulses
23		3.5 Vp pulses
TP7	VLEADR	┴┴┴ ≈4Vp pulses @ 500 Hz.
TP8	VLAGR	┬┬┬ ≈4Vp pulses @ 500 Hz.
TP9	PLLER (VLOOP)	Locked: +0.1Vdc Unlocked: -12 Vdc.

3 If Option 001 - Frequency Reference is installed, check the following test points on the phase lock loop (schematic 1104-00-3327 sheet 6).

TP11	TCXO Output	≈4Vpp square @ 10 MHz ±1ppm.
TP12	OSCIN	≈3.5 Vpp square @ 500 kHz.
REF OUT		TTL square @ 10 MHz.

Connect a 10 MHz TTL signal to the Ref In connector.

TP10	EXTREF	TTL square @ 10 MHz.

6.8.16 Microprocessor Section

1. Check the Microprocessor Section: Schematic 1104-00-3395 Sheet 3 of 10, Assembly drawing 1101-00-3395 sheet 1 of 3. For a description of the Microprocessor Section' circuits, refer to paragraph 5.7.2.
2. Observe the Microprocessor's Life Lite. During normal operation the Microprocessor's Life Lite blinks at a rate of about 2 or 3 blinks per second. If the Life Lite blinks, the Microprocessor Section is functioning correctly.
   Non-Blinking Life Lite - Microprocessor Section inoperative. The LED may be continuously on or off. If continuously on, the power supplies are probably operational and the fault is in the microprocessor circuits. If continuously off, the possibility of power supply failure should be checked prior to microprocessor circuit troubleshooting.
3. Check the supply voltages to the circuits within the Microprocessor Section.
4. Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

6.8.17 DAC Sample and Hold Network

Refer to the Motherboard assembly drawing (1101-00-3395) and schematic (1104-00-3395 sheet 5) in section 7 of this manual. Also refer to the circuit description, paragraph 5.7.5 of this manual. Reset the unit by pressing SHIFT and RESET ALL keys.

Check the following test points. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP7	SHDAC	Verify a stepped waveform.
R33/R34	VOFST	≈0Vdc
U21B-7	VAMCAL	Verify a dc voltage.
U22B-7	VSLEN	Verify a dc voltage.
U23B-7	VFREQ	Verify a dc voltage.

U22A-1	VCGZERO	Verify a dc voltage.
U24B-7	VPHASE	Verify a dc voltage.
U21A-1	VSINCAL	Verify a dc voltage.
U24A-1	VTRIBAL	Verify a dc voltage.

6.8.18 GPIB Section

Refer to the Motherboard assembly drawing (1101-00-3395) and schematic (1104-00-3395 sheet 10) in section 7 of this manual. Also refer to the circuit description, paragraph 5.7.3 of this manual.

To troubleshoot the GPIB section,

1. Check the digital control lines to the GPIB board. Verify the overhead signals work correctly (E clock, Read/Write, chip select).
2. Check the address and data lines between the GPIA (U8) and the microprocessor section.
3. Check the lines connecting the GPIA and transceiver (U9 and U10).
4. Check the lines between the transceiver and the GPIB controller.

6.8.19 Board Interfaces

Each of the Model 95's boards contains interface circuits that "translates" address/data information from the microprocessor section for use on the board. Troubleshooting these interfaces checking the boards enable lines and verifying the activity on the address and data lines.

Function Generator Board Interface

Schematic: 1104-00-3342 sheet 1.
Assembly: 1101-00-3342
Circuit Description: paragraph 5.7.4.1.

Phase Lock Loop Board Interface

Schematic: 1104-00-3341 sheet 1.
Assembly: 1101-00-3341
Circuit Description: paragraph 5.7.4.2.

Arb Board Interface

Schematic: 1104-00-3327 sheet 1.
Assembly: 1101-00-3327
Circuit Description: paragraph 5.7.4.3.

Output Board Interface

Schematic: 1104-00-3335 sheet 1.
Assembly: 1101-00-3335
Circuit Description: paragraph 5.7.4.4.

Front Panel Interface

Schematic: 1104-00-3322 sheet 2.
Assembly: 1101-00-3322
Circuit Description: paragraph 5.7.4.5.

6.9 DISASSEMBLY AND REASSEMBLY

6.9.1 Disassembly

Top Cover/Shield Removal

To remove the top cover and shield,

1. Set the POWER switch to OFF (extended).
2. Remove the power cable from the rear panel power connector.
3. Remove the five screws that secure the top cover; four in the top and one at the rear. Two of the four top cover screws are located under the Calibration Label.
4. Slide the top cover toward the rear and remove. Then lift off the shield.

Bottom Cover Removal

To remove the bottom cover,

1. Set the POWER switch to OFF (extended).
2. Remove the power cable from the rear panel power connector.
3. Turn the Model 95 upside down.
4. Remove the three screws that secure the bottom cover; one in the bottom cover and two in the rear. The one screw on the bottom cover is located under the Calibration Label.
5. Slide the bottom cover towards the rear and remove.

6.9.2 Board Removal/Replacement

To remove the Output, PLL, Function Generator, or Arb board,

1. Perform the steps in paragraph 6.9.1 - Top Cover/Shield Removal.

2. Disconnect the cable from the Output Board. Disconnect the four cables from the Arb Board.

3. Lift out the board using the extractors.

To replace the Output, PLL, Function Generator, or Arb board

1. Place the board in its guide and press it down to lock it in the connector

2. Connect the cable to the Output Board. Connect the four cables to the Arb Board.

2 Perform the steps in paragraph 6.9.3 - Top Cover/ Shield Reassembly.

6.9.3 Reassembly

Bottom Cover Replacement

To replace the bottom cover,

1. Turn the Model 95 upside down.
2. Slide the bottom cover into the slots on the bottom.
3. Secure the bottom cover with three screws (two in the rear and one on the bottom cover).

Top Cover Replacement

Top replace the top cover,

1. Turn the Model right side up.
2. Install the shield, aligning the screw holes.
3. Slide the top cover into the slots on the top.
4. Secure the top cover using five screws (one at the rear and four in the top). The four top cover

SECTION 7
PARTS LISTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, schematics, and parts lists are arranged in order shown below.

7.1.1 Assembly Drawing

All of the mechanical assembly drawings are show in this section. These drawings contain enough detail and clarity to assist the repair technician in the disassembly and reassembly of the Model 95 . The parts lists for each assembly drawing immediately follows that drawing.

7.1.2. Schematics

All of the schematics for the Model 95 are shown in this section. Schematic drawings containing a proprietary message may not be copied for resale or use in any other publication nor for any use other than the repair and maintenance of the instrument associated with this manual.

7.1.3 Parts Lists

The parts lists for each individual board or assembly are shown immediately following that board or assembly. The parts lists contain Wavetek and manufacturers parts information. All manufacturers are listed by a Wavetek code designation.

7.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permits. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

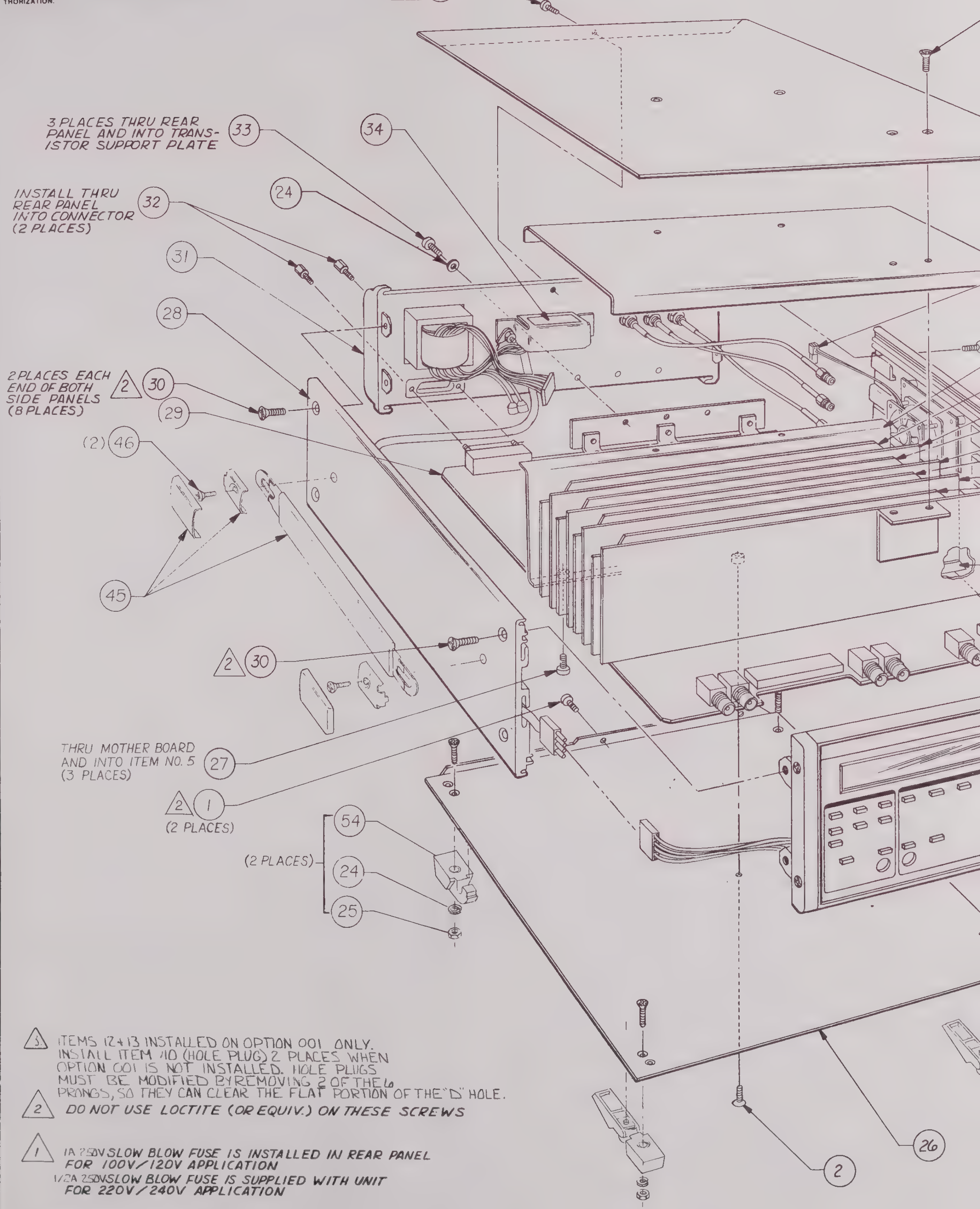
7.3 ORDERING PARTS

When ordering spare parts, please specify the part number, circuit reference, board, serial number of the unit, and, if applicable, the function performed.

The number etched into a PC board is the board part number. The assembly (PC board and components on the board) part number is stamped on the board.

DRAWING	DRAWING NUMBER
Top Assembly Drawing	1001-00-0599
Instrument Schematic	1004-00-0599
Instrument Parts List	1000-00-0609
Installation Drawing	0002-00-0599
Motherboard Schematic	1104-00-3395
Motherboard Assembly	1101-00-3395
Motherboard Parts List	1100-00-3390
	1200-00-3390
Front Panel Assembly	1101-00-3344
Front Panel Assembly Parts List	1100-00-3344
Display / Keyboard Assembly Schematic	1104-00-3322
Display / Keyboard Assembly	1101-00-3322
Display / Keyboard Assembly Parts List	1100-00-3322
Output Board Schematic	1104-00-3335
Output Board Assembly	1101-02-3335
Output Board Parts List	1100-00-3335

DRAWING	DRAWING NUMBER
Phase Lock Board Schematic	1104-00-3437
Phase Lock Board Assembly	1101-00-3437
Phase Lock Board Parts List	1100-00-3437
Function Generator Board Schematic	1104-00-3342
Function Generator Board Assembly	1101-00-3342
Function Generator Board Parts List	1100-00-3342
Arb Board Schematic	1104-00-3327
Arb Board Assembly	1101-00-3327
Arb Board Parts List	1100-00-3401
Rear Panel Assembly	1101-00-3325
Rear Panel Assembly Parts List	1100-00-3325
Tilt Bail Assembly	1201-00-3392
Tilt Bail Parts List	1200-00-3392


115085
8
7
6
5
D
C
B
A
2 1
34
3 PLACES THRU REAR PANEL AND INTO TRANSISTOR SUPPORT PLATE 33
INSTALL THRU REAR PANEL INTO CONNECTOR (2 PLACES) 32
24
31
28
2 PLACES EACH END OF BOTH SIDE PANELS (8 PLACES) 2 30
29
(2) 46
45
2 30
THRU MOTHER BOARD AND INTO ITEM NO. 5 (3 PLACES) 27
2 1
(2 PLACES)
(2 PLACES)
54
24
25
26
2

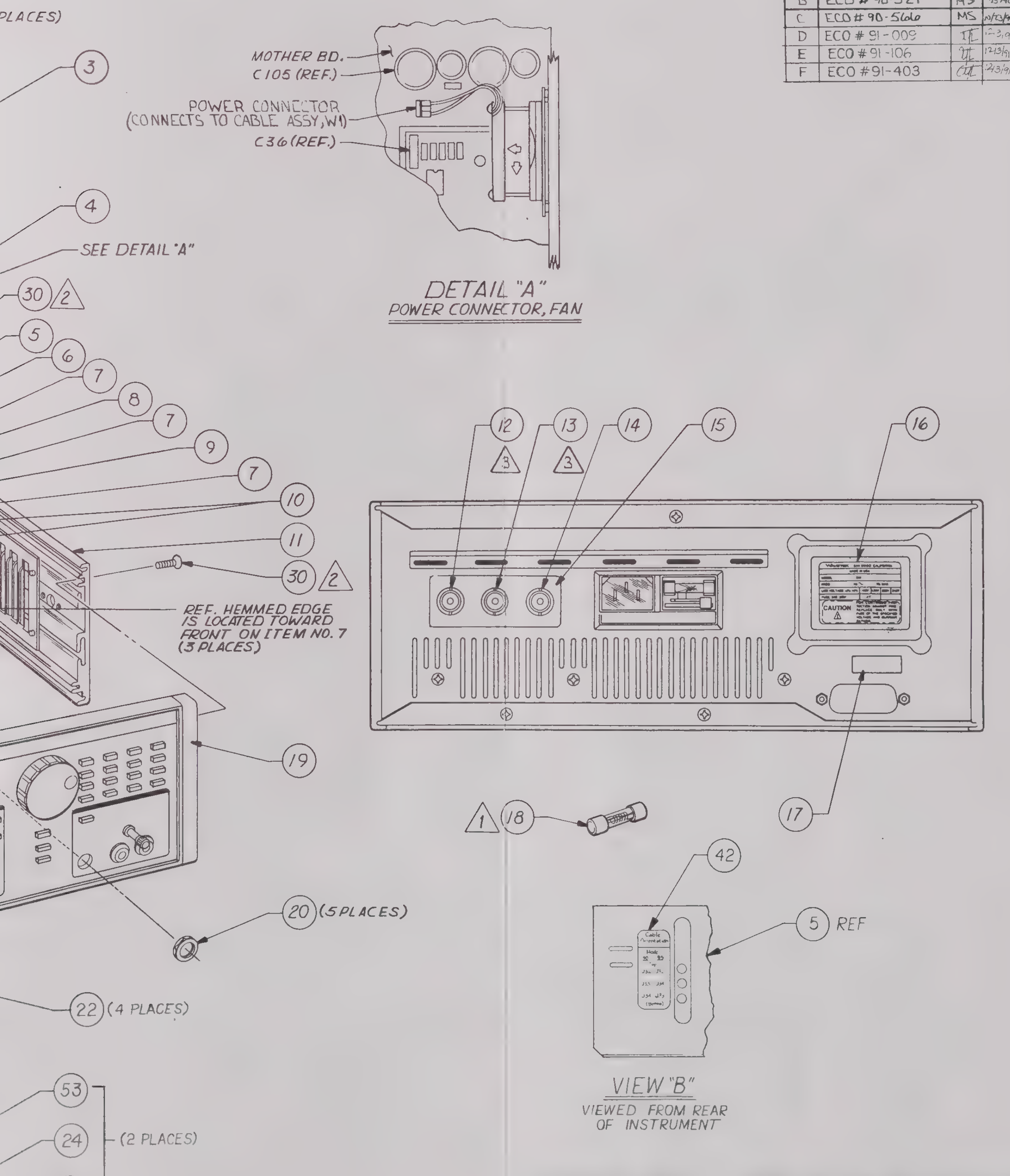
3 ITEMS 12+13 INSTALLED ON OPTION 001 ONLY. INSTALL ITEM 10 (HOLE PLUG) 2 PLACES WHEN OPTION 001 IS NOT INSTALLED. HOLE PLUGS MUST BE MODIFIED BY REMOVING 2 OF THE 6 PRONGS, SO THEY CAN CLEAR THE FLAT PORTION OF THE "D" HOLE.

2 DO NOT USE LOCTITE (OR EQUIV.) ON THESE SCREWS

1 1A 250V SLOW BLOW FUSE IS INSTALLED IN REAR PANEL FOR 100V/120V APPLICATION
1/2A 250V SLOW BLOW FUSE IS SUPPLIED WITH UNIT FOR 220V/240V APPLICATION

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ERO NO. 90-441	AD	6/29/90	
B	ECO # 90-521	MS	10/15/90	NM
C	ECO # 90-566	MS	10/23/90	
D	ECO # 91-009	TL	1-23-91	NM
E	ECO # 91-106	TL	12/13/91	NM
F	ECO # 91-403		12/13/91	NM


PLACES)
3
MOTHER BD.
C105 (REF.)
POWER CONNECTOR (CONNECTS TO CABLE ASSY, W1)
C36 (REF.)
4
SEE DETAIL "A"
30 2
5
6
7
8
7
9
7
10
11
30 2
REF. HEMMED EDGE IS LOCATED TOWARD FRONT ON ITEM NO. 7 (3 PLACES)
19
12 3
13
14 3
15
16
CAUTION
1 18
17
42
Cable
5 REF
20 (5 PLACES)
22 (4 PLACES)
53
24
25
(2 PLACES)

DETAIL "A"
POWER CONNECTOR, FAN

VIEW "B"
VIEWED FROM REAR OF INSTRUMENT

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 5-11-90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —//—	CHECKED	6/20/90	TITLE TOP ASSEMBLY DRAWING
	PROJ ENGR	6/28/90	
FINISH WAVETEK PROCESS —//—	RELEASE APPROV	6/29/90	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS ± / DECIMALS .XX ± / .XXX ± / ANGLES ± /		SIZE D · FSCM NO. 23338 · DWG. NO. 1001-00-0599 · REV F
DO NOT SCALE DRAWING			SCALE NONE · MODEL 95 · SHEET 1 OF 1

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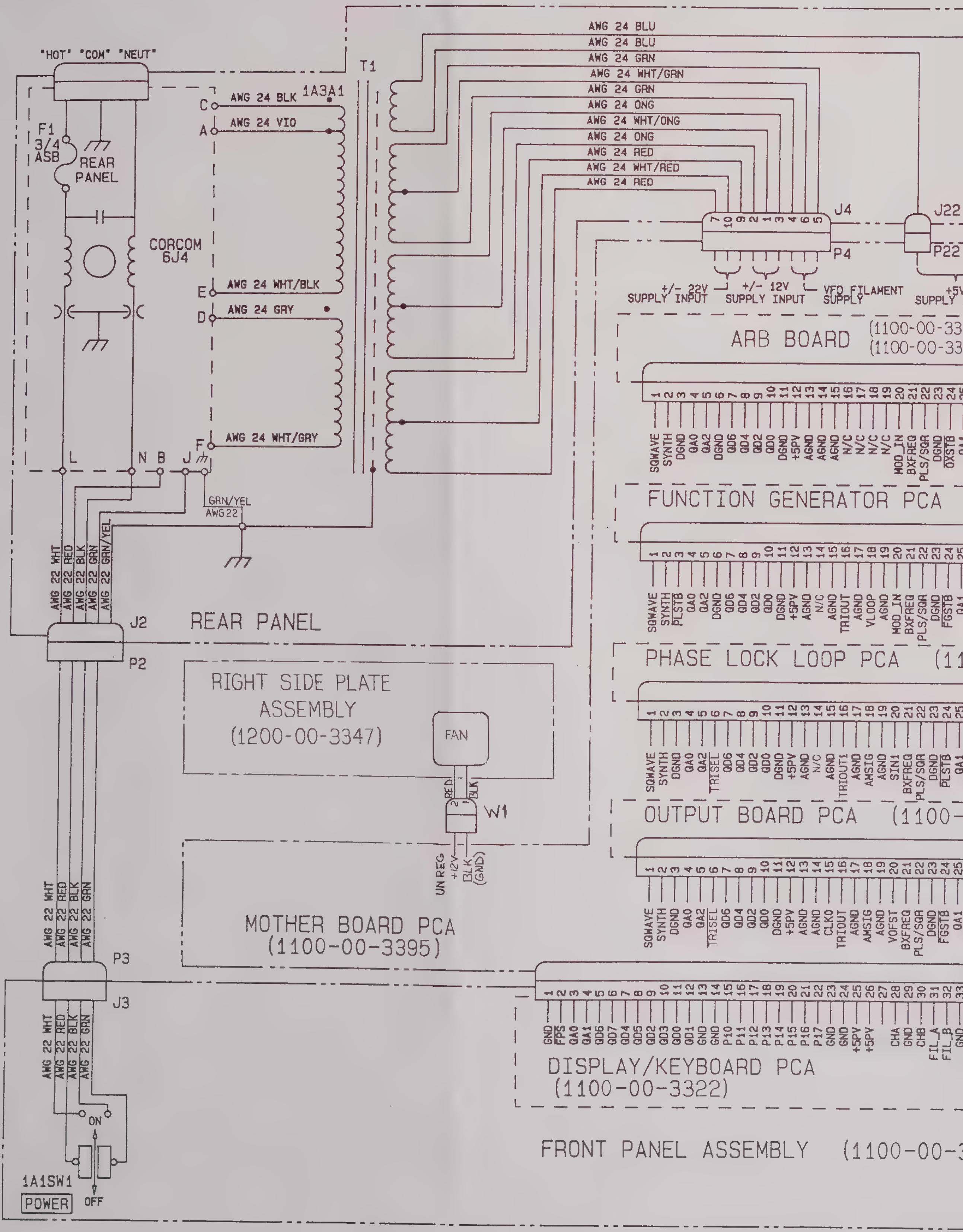
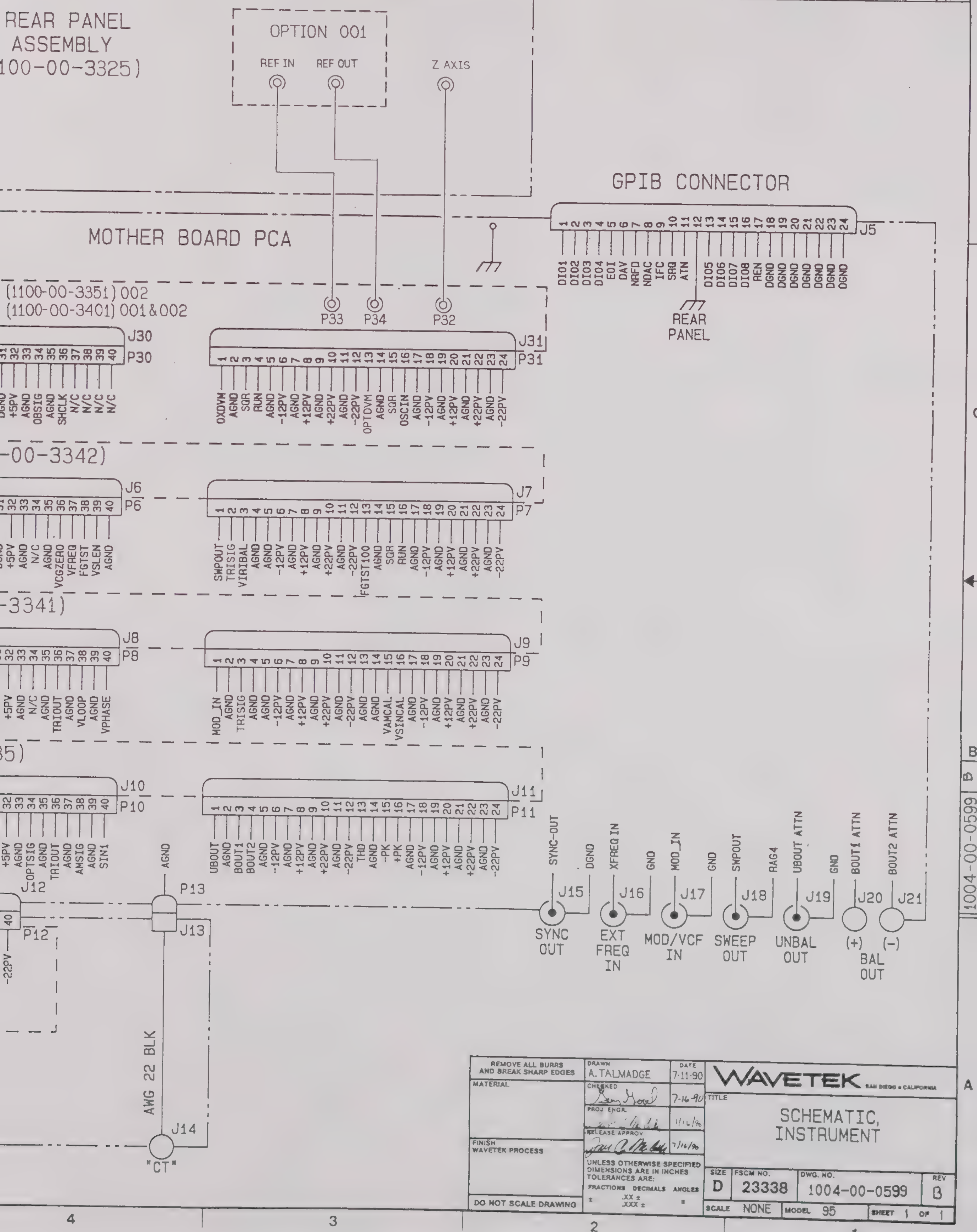

"HOT" "COM" "NEUT"
F1
3/4
ASB
REAR
PANEL
CORCOM
6J4
L
N
B
J
C
A
E
D
F
AWG 24 BLK
1A3A1
AWG 24 VIO
AWG 24 WHT/BLK
AWG 24 GRY
AWG 24 WHT/GRY
T1
GRN/YEL
AWG22
AWG 24 BLU
AWG 24 BLU
AWG 24 GRN
AWG 24 WHT/GRN
AWG 24 GRN
AWG 24 ONG
AWG 24 WHT/ONG
AWG 24 ONG
AWG 24 RED
AWG 24 WHT/RED
AWG 24 RED
7 10 9 2 1 3 4 6 5
J4
P4
J22
P22
+/- 22V SUPPLY INPUT
+/- 12V SUPPLY INPUT
VFD FILAMENT SUPPLY
+5V SUPPLY
ARB BOARD
(1100-00-33
(1100-00-33
1 SQWAVE
2 SYNTH
3 DGND
4 QA0
5 QA2
6 DGND
7 QD6
8 QD4
9 QD2
10 QD0
11 DGND
12 +5PV
13 AGND
14 AGND
15 AGND
16 N/C
17 N/C
18 N/C
19 N/C
20 MOD_IN
21 BXFREQ
22 PLS/SQR
23 DGND
24 OXSTB
FUNCTION GENERATOR PCA
1 SQWAVE
2 SYNTH
3 PLSTB
4 QA0
5 QA2
6 DGND
7 QD6
8 QD4
9 QD2
10 QD0
11 DGND
12 +5PV
13 AGND
14 N/C
15 AGND
16 TRIOUT
17 AGND
18 VLOOP
19 AGND
20 MOD_IN
21 BXFREQ
22 PLS/SQR
23 DGND
24 FGSTB
25 QA1
PHASE LOCK LOOP PCA (11
1 SQWAVE
2 SYNTH
3 DGND
4 QA0
5 QA2
6 TRISEL
7 QD6
8 QD4
9 QD2
10 QD0
11 DGND
12 +5PV
13 AGND
14 N/C
15 AGND
16 TRIOUT1
17 AGND
18 AMSIG
19 AGND
20 SIN1
21 BXFREQ
22 PLS/SQR
23 DGND
24 PLSTB
25 QA1
OUTPUT BOARD PCA (1100-
1 SQWAVE
2 SYNTH
3 DGND
4 QA0
5 QA2
6 TRISEL
7 QD6
8 QD4
9 QD2
10 QD0
11 DGND
12 +5PV
13 AGND
14 AGND
15 CLKO
16 TRIOUT
17 AGND
18 AMSIG
19 AGND
20 VOFST
21 BXFREQ
22 PLS/SQR
23 DGND
24 FGSTB
25 QA1
AWG 22 WHT
AWG 22 RED
AWG 22 BLK
AWG 22 GRN
AWG 22 GRN/YEL
J2
P2
REAR PANEL
RIGHT SIDE PLATE
ASSEMBLY
(1200-00-3347)
FAN
RED
BLK
2
1
W1
UN REG
+12V
BLK
(GND)
MOTHER BOARD PCA
(1100-00-3395)
AWG 22 WHT
AWG 22 RED
AWG 22 BLK
AWG 22 GRN
P3
J3
AWG 22 WHT
AWG 22 RED
AWG 22 BLK
AWG 22 GRN
ON
OFF
1A1SW1
POWER
1 GND
2 FPS
3 QA0
4 QA1
5 QD6
6 QD7
7 QD4
8 QD5
9 QD2
10 QD3
11 QD0
12 QD1
13 GND
14 GND
15 P10
16 P11
17 P12
18 P13
19 P14
20 P15
21 P16
22 P17
23 GND
24 GND
25 +5PV
26 +5PV
27
28 CHA
29 GND
30 CHB
31 FIL_A
32 FIL_B
33 GND
DISPLAY/KEYBOARD PCA
(1100-00-3322)
FRONT PANEL ASSEMBLY (1100-00-

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ERO # 90-477	GT	7/16/90	ΠM
B	ECO # 90-521	MS	10/5/90	ΠM



REAR PANEL ASSEMBLY
100-00-3325)
OPTION 001
REF IN
REF OUT
Z AXIS
GPIB CONNECTOR
J5
DIO1 DIO2 DIO3 DIO4 EOI DAV NRFD NDAC IFC SRQ ATN DIO5 DIO6 DIO7 DIO8 REN DGND DGND DGND DGND DGND DGND DGND
REAR PANEL
MOTHER BOARD PCA
(1100-00-3351) 002
(1100-00-3401) 001 & 002
P33
P34
P32
J30
P30
J31
P31
OXDVM AGND SQR RUN AGND -12PV AGND +12PV AGND +22PV AGND -22PV OPTDVM AGND SQR OSCIN AGND -12PV AGND +12PV AGND +22PV AGND -22PV
DGND +5PV AGND OBSIG AGND SHCLK N/C N/C N/C N/C
-00-3342)
J6
P6
J7
P7
DGND +5PV AGND N/C AGND VCGZERO VFREQ FGTST VSLEN AGND
SWPOUT TRISIG VIRIBAL AGND AGND -12PV AGND +12PV AGND +22PV AGND -22PV FGTST100 SQR RUN AGND -12PV AGND +12PV AGND +22PV AGND -22PV
-3341)
J8
P8
J9
P9
+5PV AGND N/C AGND TRIOUT AGND VLOOP AGND VPHASE
MOD_IN AGND TRISIG AGND AGND -12PV AGND +12PV AGND +22PV AGND -22PV AGND AGND VAMCAL VSINCAL AGND -12PV AGND +12PV AGND +22PV AGND -22PV
35)
J10
P10
J11
P11
+5PV AGND OPTSIG AGND TRIOUT AGND AMSIG AGND SIN1
UBOUT AGND BOUT1 BOUT2 AGND -12PV AGND +12PV AGND +22PV AGND -22PV THD AGND -PK +PK AGND -12PV AGND +12PV AGND +22PV AGND -22PV
J12
P12
-22PV
AGND
P13
J13
AWG 22 BLK
J14
"CT"
SYNC-OUT
DGND
XFREQ IN
GND
MOD_IN
GND
SWPOUT
RAG4
UBOUT ATTN
GND
BOUT1 ATTN
BOUT2 ATTN
J15
J16
J17
J18
J19
J20
J21
SYNC OUT
EXT FREQ IN
MOD/VCF IN
SWEEP OUT
UNBAL OUT
(+)
(-)
BAL OUT
1004-00-0599
B
4
3
2
1
A
C

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

		DATE
DRAWN	A. TALMADGE	7-11-90
CHECKED		7-16-90
PROJ ENGR		7/16/90
RELEASE APPROV		7/16/90

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
INSTRUMENT

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1004-00-0599	B

SCALE NONE MODEL 95 SHEET 1 OF 1

D

REFERENCE DESIGNATORS	PART DESCRIPTION
42	LABEL, CABLE ORIENTATION
32	HARDWARE KIT, GPIB CONN
18	FUSE, 1A, 250V, S-B
25	NUT, FLEXLOC, 6-32, Z
20	NUT, HEX, 1/2-28
24	LOCKWASHER, #8 SPLIT RING, SS
22	SCREW, 6-32X3/4 FH 100 PHLP, Z 6-32 X 3/
1	SCREW PLPS PAN M/S 18-8 S/S 6-32X3/8
33	SCREW PLPS PAN M/S 18-8 S/S 8-32X1/2
30	SCREW, 8-32X7/16, 100D G FH, PHLPS, SS
27	SCREW, PH, 6-32 X 5/16, PHLPS, NYLOK, SS
2	SCREW, 6-32/3/8, FH, PH PS, 100 DEG, SS, NYLOK

WAVETEK
PARTS LIST

TITLE
MODEL 95 W/001/002

C

REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	PWR CORD, SHIELDED

WAVETEK
PARTS LIST

TITLE
MODEL 95 W/001/002

B

A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D, INSTRUMENT	1001-00-0599	WVTK	1001-00-0599	1
NONE	ACCEPTANCE TEST PROCEDURE	1002-00-0599	WVTK	1002-00-0599	1
NONE	S/D, INSTRUMENT	1004-00-0599	WVTK	1004-00-0599	1
NONE	INSTRUMENT MANUAL 95 "NOT RELEASED"	1006-00-0599	WVTK	1006-00-0599	1
NONE	CALIBRATION PROCEDURE, MODEL 90	1008-00-0596	WVTK	1008-00-0596	1
NONE	LABEL/DRWG, INFO, S/N & PWR-95	1009-00-0599	WVTK	1009-00-0599	1
NONE	REAR PANEL ASSY, MODEL 90	1100-00-3325	WVTK	1100-00-3325	1
NONE	PCA, OUTPUT BOARD	1100-00-3335	WVTK	1100-00-3335	1
NONE	PCA, FUNCTION GENERATOR	1100-00-3342	WVTK	1100-00-3342	1
NONE	ASSY, FRONT PANEL	1100-00-3344	WVTK	1100-00-3344	1
NONE	PCA, MOTHER BOARD	1100-00-3390	WVTK	1100-00-3390	1
NONE	PCA, ARB BOARD OPT 1 AND 2, MODEL 95	1100-00-3401	WVTK	1100-00-3401	1
NONE	PCA, PHASE LOCK LOOP	1100-00-3437	WVTK	1100-00-3437	1

WAVETEK PARTS LIST
TITLE
MODEL 95 W/001/002
ASSEMBLY NO. 1000-00-0609
PAGE 1
REV
D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY, SIDE PLATE, RIGHT	1200-00-3347	WVTK	1200-00-3347	1
NONE	ASSY, SIDE PLATE, LEFT	1200-00-3348	WVTK	1200-00-3348	1
NONE	ASY ASSY, COAX J32	1200-00-3381	WVTK	1200-00-3381	1
NONE	ASSY, COAX J33	1200-00-3382	WVTK	1200-00-3382	1
NONE	COAX ASSY, J34	1200-00-3383	WVTK	1200-00-3383	1
NONE	TILT BAIL ASSY	1200-00-3392	WVTK	1200-00-3392	1
23	INSTRUMENT FOOT ASSY	1200-00-3428	WVTK	1200-00-3428	4
NONE	LABEL, CAUTION	859-1400	WVTK	1400-01-1400	1
NONE	LABEL, OPTION, MODEL 23	1400-01-9890	WVTK	1400-01-9890	1
NONE	SHIELD, INNER	1400-02-3323	WVTK	1400-02-3323	3
NONE	SHIELD, TOP	1400-02-3353	WVTK	1400-02-3353	1
NONE	COVER, TOP	1400-02-3532	WVTK	1400-02-3532	1
NONE	COVER, BOTTOM	1400-02-4522	WVTK	1400-02-4522	1
NONE	LABLE, SMB CONNECTOR Z AXIS	1400-02-5076	WVTK	1400-02-5076	1
NONE	SHIELD, REAR	1400-02-5084	WVTK	1400-02-5084	1

WAVETEK PARTS LIST
TITLE
MODEL 95 W/001/002
ASSEMBLY NO. 1000-00-0609
PAGE 2
REV
D

GR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
2-5117	WVTK	1400-02-5117	1
-1	AMP	2100-07-0024	1
	BUSS	2400-05-0029	1
T F.L.	CMRCL	2800-15-6100	4
31-2	AMP	2800-16-0025	5
	CMRCL	2800-42-8000	3
3/4 F.H. 100	CMRCL	2800-44-6112	4
7-28	CMRCL	2800-48-6106	3
H 8-32X1/2	CMRCL	2800-48-8108	3
-8107	CMCRL	2800-54-8107	8
-6105	CMRCL	2800-59-6105	3
-6106	CMRCL	2800-60-6106	5

ASSEMBLY NO. 1000-00-0609
PAGE 3
REV
D

GR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
-0009	WVTK	6001-80-0009	1

ASSEMBLY NO. 1000-00-0609
PAGE 4
REV
D

REMOVE ALL BURRS
AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN
DATE
CHECKED
PROJ ENGR
RELEASE APPROV

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE.
FRACTIONS DECIMALS ANGLES
± .XX ± .XXX ± ∠

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
INSTRUMENT

SIZE D
FSCM NO. 23338
DWG NO 1000-00-0609
REV D
SCALE
MODEL 95
SHEET 1 OF 1

113695

8 7 6 5

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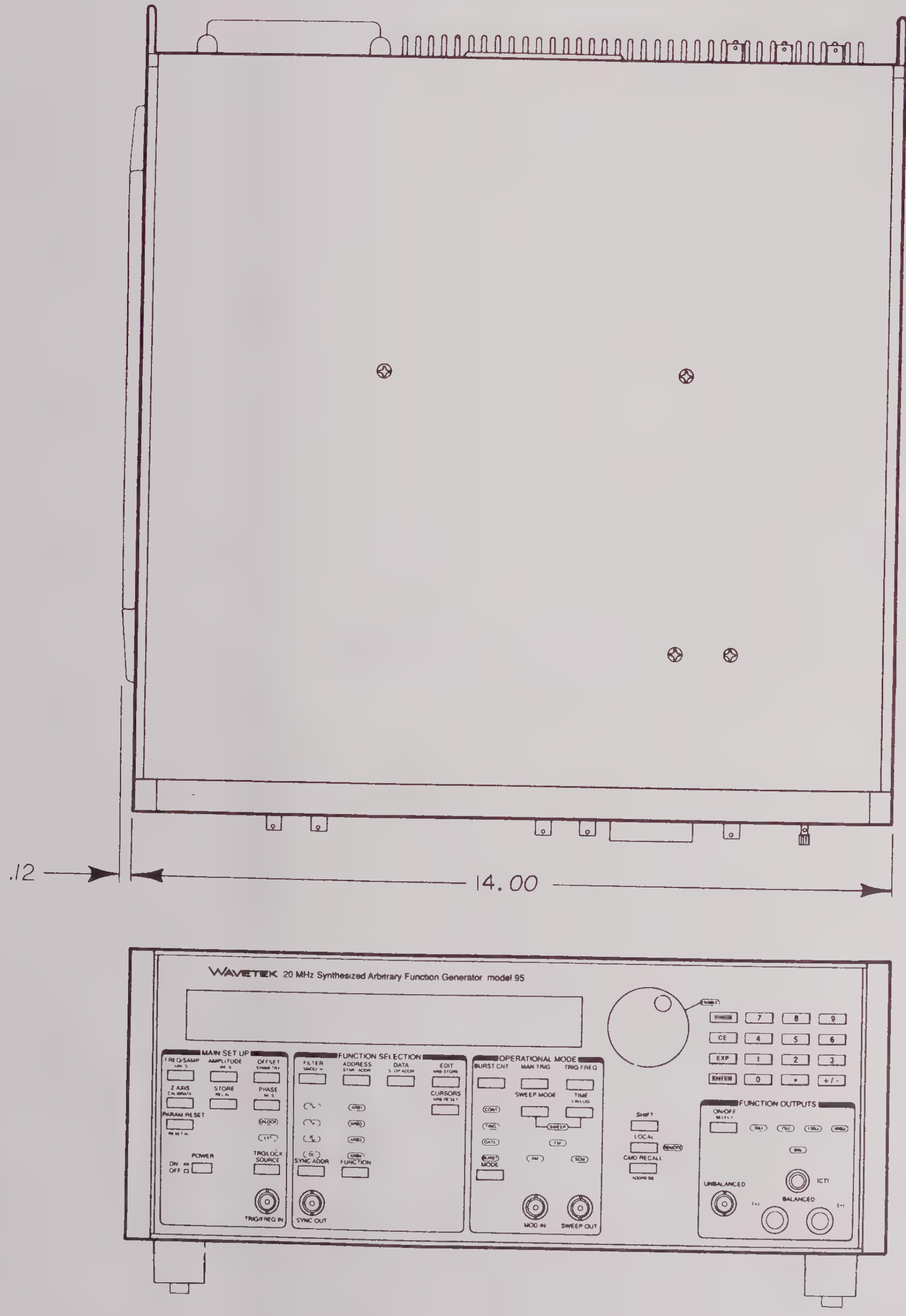
)

C

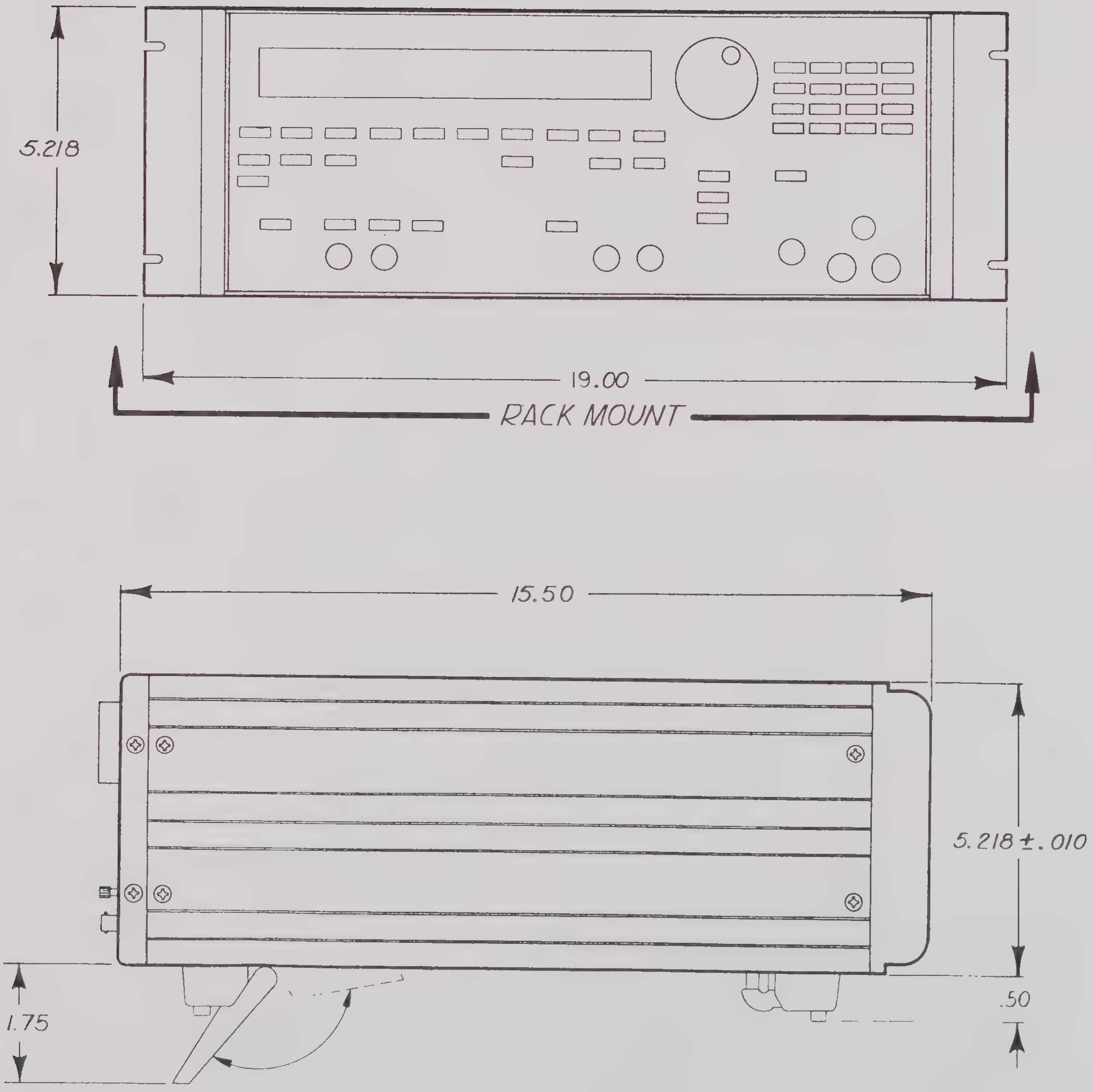
B

A


.12
14.00
WAVETEK 20 MHz Synthesized Arbitrary Function Generator model 95
MAIN SET UP
FREQ/SAMP
AMPLITUDE
OFFSET
Z AXIS
STORE
PHASE
PARAM RESET
POWER
ON
OFF
TRIG/LOCK SOURCE
TRIG/FREQ IN
FUNCTION SELECTION
FILTER
ADDRESS
DATA
EDIT
CURSORS
SYNC ADDR
FUNCTION
SYNC OUT
OPERATIONAL MODE
BURST CNT
MAN TRIG
TRIG FREQ
SWEEP MODE
TIME
MODE
MOD IN
SWEEP OUT
SHIFT
LOCAL
CMD RECALL
CE
EXP
7
8
9
4
5
6
1
2
3
0
•
+/-
FUNCTION OUTPUTS
ON/OFF
UNBALANCED
BALANCED
(+)
(−)

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ERO NO. 90-441	AP	6/29/90	
B	ECO # 91-267	KA	9/16/91	
C	ECO # 91-403		11/21/91	nm



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D.COOPER	DATE 5-11-90	**WAVETEK** SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED	6/29/90	TITLE INSTALLATION DRAWING
	PROJ ENGR	6/29/90	
FINISH WAVETEK PROCESS	RELEASE APPROV	6/29/90	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± 1/ DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 1°		SIZE D · FSCM NO 23338 · DWG. NO. 0002-00-0599 · REV C
DO NOT SCALE DRAWING			SCALE 1/4 · MODEL 95 · SHEET 1 OF 1

C 0002-00-0599

FRONT PANEL BOARD CONNECTOR

J12

Signal	Pin
DGND	1
QA0	2
QD6	3
QD4	4
QD2	5
QD0	6
DGND	7
P10	8
P12	9
P14	10
P16	11
DGND	12
+5PV	13
DGND	14
DGND	15
FIL_A	16
DGND	17
+24PV	18
DGND	19
-24PV	20
$\overline{FPSTB}$	21
QA1	22
QD7	23
QD5	24
QD3	25
QD1	26
DGND	27
P11	28
P13	29
P15	30
P17	31
DGND	32
+5PV	33
RKA	34
RKB	35
FIL_B	36
DGND	37
+24PV	38
DGND	39
-24PV	40

OUTPUT BOARD CONNECTORS

P10

Signal	Pin
SQWAVE	1
SYNTH	2
DGND	3
QA0	4
QA2	5
$\overline{TRISEL}$	6
QD6	7
QD4	8
QD2	9
QD0	10
DGND	11
+5PV	12
AGND	13
	14
CLKO	15
TRIOUT1	16
AGND	17
AMSIG	18
AGND	19
VOFST	20
BXFREQ	21
PLS/SQR	22
DGND	23
$\overline{OBSTB}$	24
QA1	25
DGND	26
QD7	27
QD5	28
QD3	29
QD1	30
DGND	31
+5PV	32
AGND	33
OBSIG	34
AGND	35
*	36
AGND	37
AMSIG	38
AGND	39
SIN1	40

P11

Signal	Pin
UBOUT	1
AGND	2
BOUT1	3
BOUT2	4
AGND	5
-12PV	6
AGND	7
+12PV	8
AGND	9
+24PV	10
AGND	11
-24PV	12
THD	13
AGND	14
-PK	15
+PK	16
AGND	17
-12PV	18
AGND	19
+12PV	20
AGND	21
+24PV	22
AGND	23
-24PV	24

PHASE BOARD

SQWAVE
SYNTH
DGND
QA0
QA2
$\overline{TRISEL}$
QD6
QD4
QD2
QD0
DGND
+5PV
AGND

TRIOUT1
AGND
AMSIG
AGND
SIN1
BXFREQ
PLS/SQR
DGND
$\overline{PLSTB}$
QA1
DGND
QD7
QD5
QD3
QD1
DGND
+5PV
AGND

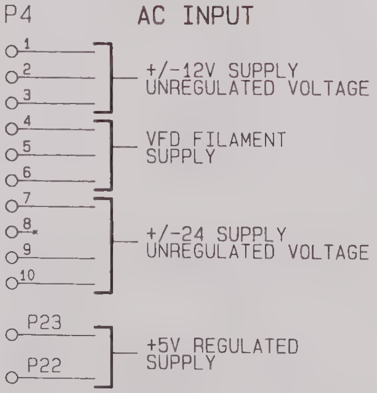
AGND
VLOOP
AGND
VPHASE

MOD_IN
AGND
TRISIG
AGND

-12PV
AGND
+12PV
AGND
+24PV
AGND
-24PV
AGND

VAMCAL
VSINCAL
AGND
-12PV
AGND
+12PV
AGND
+24PV
AGND
-24PV

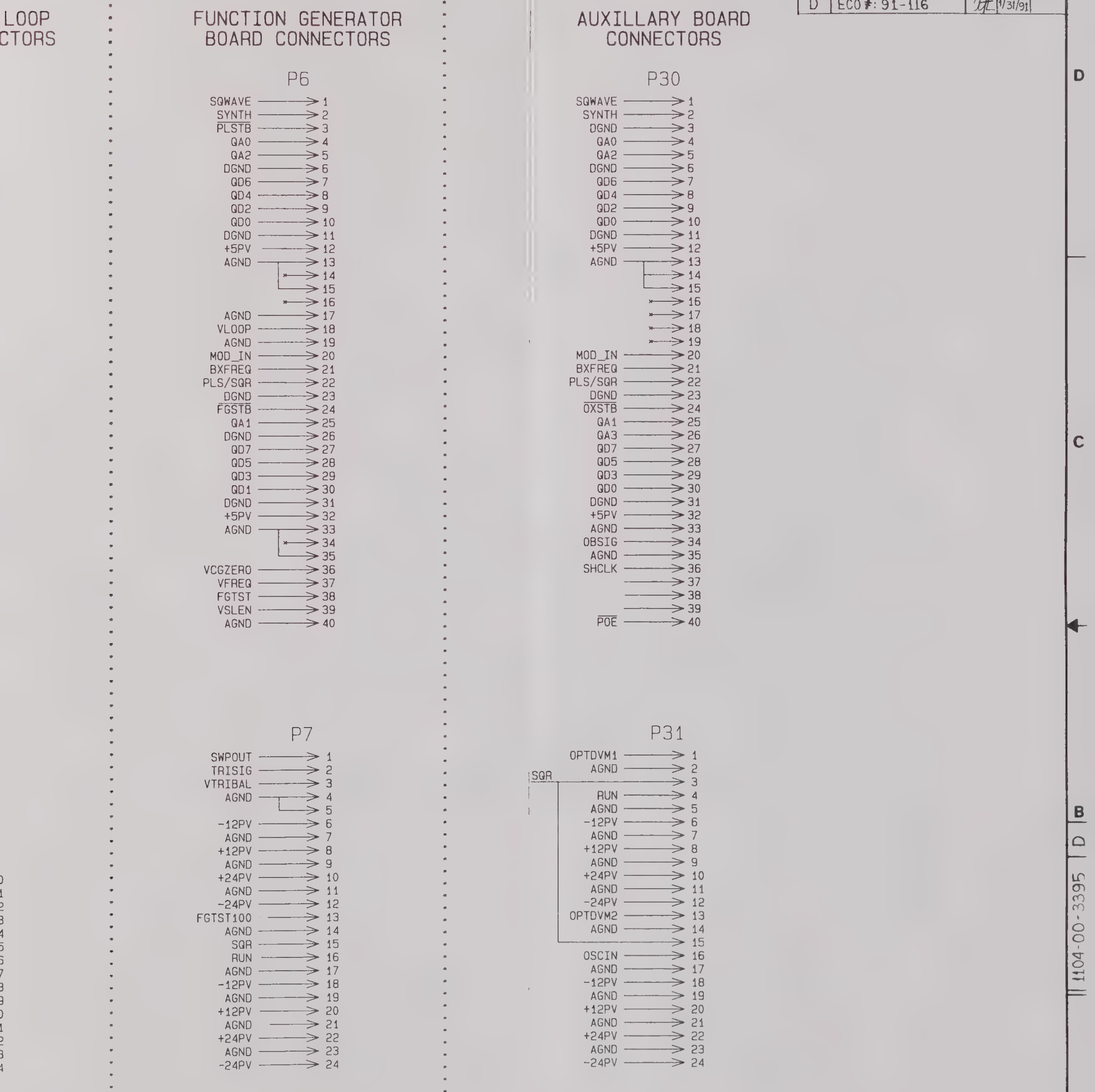
POWER SUPPLY UNREGULATED AC INPUT


P4
1
2
3
+/-12V SUPPLY UNREGULATED VOLTAGE
4
5
6
VFD FILAMENT SUPPLY
7
8*
9
10
+/-24 SUPPLY UNREGULATED VOLTAGE
P23
P22
+5V REGULATED SUPPLY

9. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
8. ⏚D =DGND, ⏚A =AGND.
7. SEE BILL OF MATERIALS FOR PROGRAMMED PART NUMBER.
6. * = PART INSTALLED IN SOCKET.
5. CAPACITORS VALUED IN MICROFRADS (uF).
4. RESISTORS VALUED IN OHMS, 1/8W, 5%.
3. FOR INSTRUMENT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596 FOR MODEL 90 AND 1004-00-0599 FOR MODEL 95.
2. INSTALL JMP1 ON PINS 1 & 2 FOR BIPOLAR EXT FREQ INPUTS. INSTALL ON PINS 2 & 3 FOR TTL EXT FREQ INPUTS.
1. INSTALL JMP7 ON PINS 1 & 2 FOR STANDARD INSTRUMENT. INSTALL ON PINS 2 & 3 FOR OPTION 001.

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ERO #: 90-462	AT	7-2-90	DEF
B	ECO #: 90-506	MS	9-14-90	NM
C	ECO #: 90-521	MS	10/15/90	NM
D	ECO #: 91-116	DL	1/31/91	


LOOP
CTORS
FUNCTION GENERATOR BOARD CONNECTORS
P6
SQWAVE 1
SYNTH 2
PLSTB 3
QA0 4
QA2 5
DGND 6
QD6 7
QD4 8
QD2 9
QD0 10
DGND 11
+5PV 12
AGND 13
14
15
16
AGND 17
VLOOP 18
AGND 19
MOD_IN 20
BXFREQ 21
PLS/SQR 22
DGND 23
FGSTB 24
QA1 25
DGND 26
QD7 27
QD5 28
QD3 29
QD1 30
DGND 31
+5PV 32
AGND 33
34
35
VCGZERO 36
VFREQ 37
FGTST 38
VSLEN 39
AGND 40
P7
SWPOUT 1
TRISIG 2
VTRIBAL 3
AGND 4
5
-12PV 6
AGND 7
+12PV 8
AGND 9
+24PV 10
AGND 11
-24PV 12
FGTST100 13
AGND 14
SQR 15
RUN 16
AGND 17
-12PV 18
AGND 19
+12PV 20
AGND 21
+24PV 22
AGND 23
-24PV 24
AUXILLARY BOARD CONNECTORS
P30
SQWAVE 1
SYNTH 2
DGND 3
QA0 4
QA2 5
DGND 6
QD6 7
QD4 8
QD2 9
QD0 10
DGND 11
+5PV 12
AGND 13
14
15
16
17
18
19
MOD_IN 20
BXFREQ 21
PLS/SQR 22
DGND 23
OXSTB 24
QA1 25
QA3 26
QD7 27
QD5 28
QD3 29
QD0 30
DGND 31
+5PV 32
AGND 33
OBSIG 34
AGND 35
SHCLK 36
37
38
39
POE 40
P31
OPTDVM1 1
AGND 2
SQR 3
RUN 4
AGND 5
-12PV 6
AGND 7
+12PV 8
AGND 9
+24PV 10
AGND 11
-24PV 12
OPTDVM2 13
AGND 14
15
OSCIN 16
AGND 17
-12PV 18
AGND 19
+12PV 20
AGND 21
+24PV 22
AGND 23
-24PV 24
D
C
B
D
1104-00-3395

CAD JOB#: B064E

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

		DATE
DRAWN	RO FIFER	10-90
CHECKED	Gene McAllister	7-2-90
PROJ. ENGR.	D.E. FISH	7-2-90
RELEASE APPROV.	D.E. FISH	7-2-90

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX ±
XXX ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
MOTHERBOARD

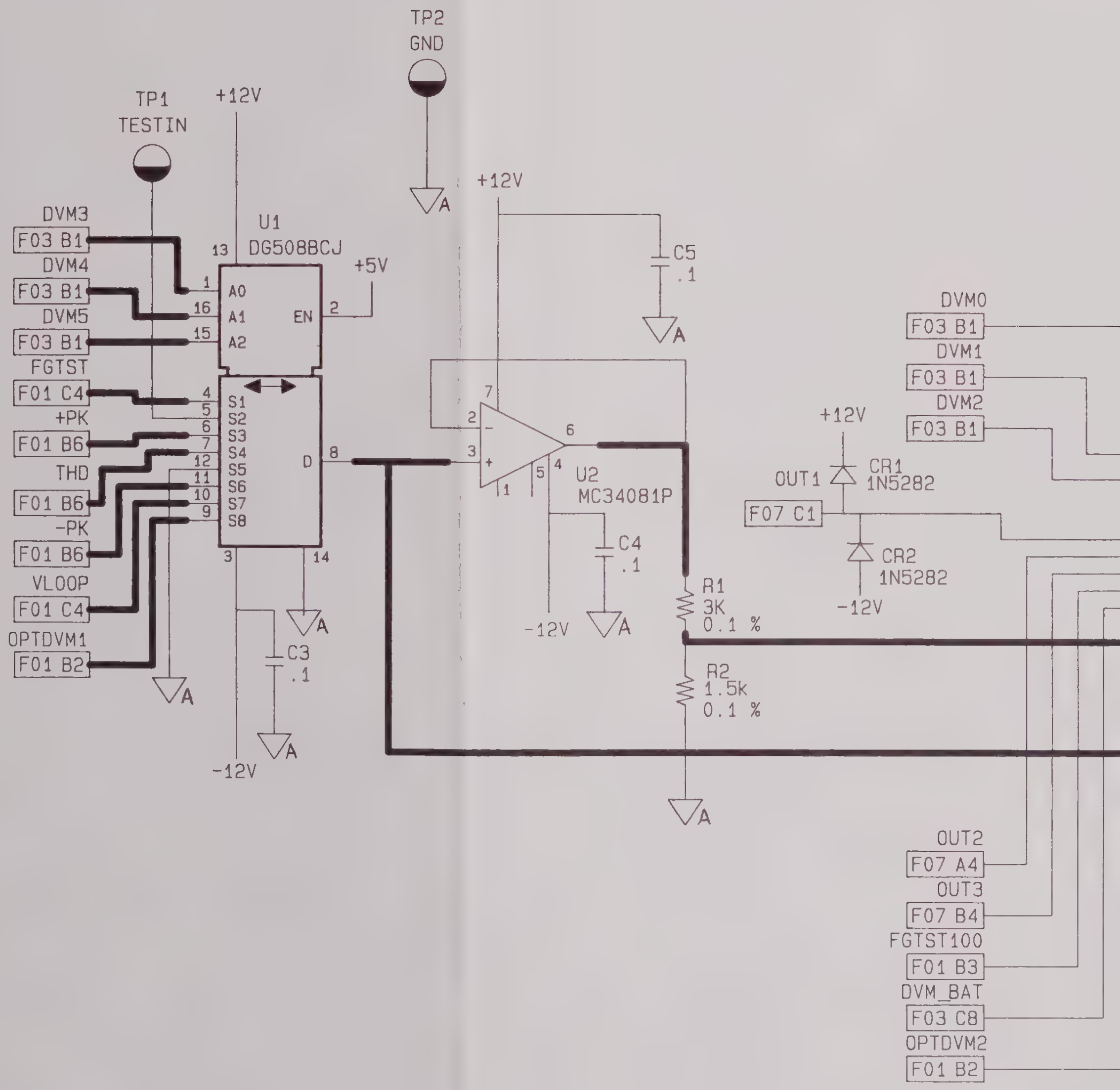
SIZE	FSCM NO	DWG NO.	REV
D	23338	1104-00-3395	D

SCALE NONE MODEL 90 SERIES SHEET 1 OF 10

A

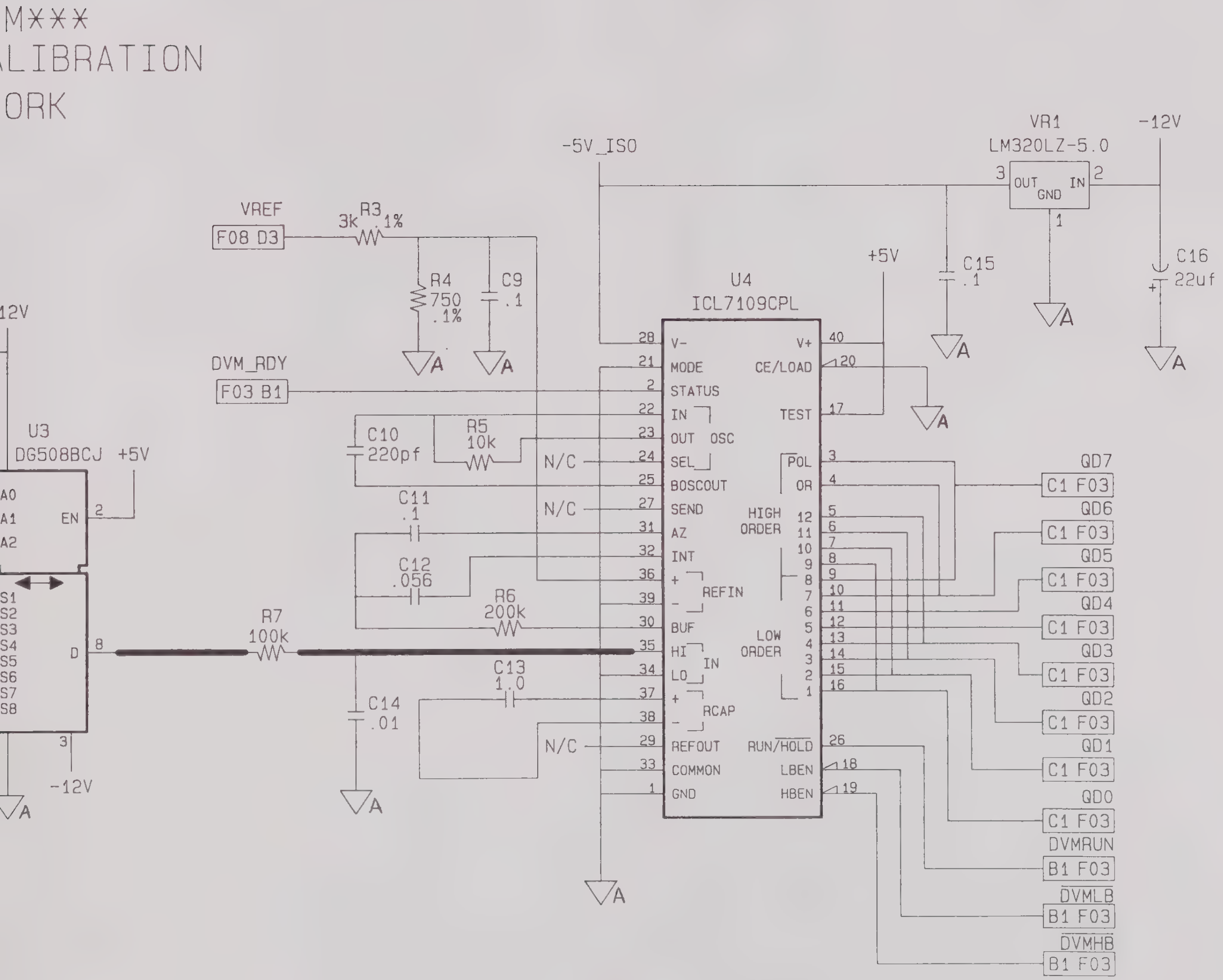
4 3 2 1

INTERNA


TP2
GND
TP1
TESTIN
+12V
U1
DG508BCJ
+5V
EN
A0
A1
A2
S1
S2
S3
S4
S5
S6
S7
S8
D
DVM3
F03 B1
DVM4
F03 B1
DVM5
F03 B1
FGTST
F01 C4
+PK
F01 B6
THD
F01 B6
-PK
F01 B6
VLOOP
F01 C4
OPTDVM1
F01 B2
C3
.1
-12V
C5
.1
U2
MC34081P
C4
.1
-12V
R1
3K
0.1 %
R2
1.5k
0.1 %
A
+12V
OUT1
CR1
1N5282
F07 C1
CR2
1N5282
-12V
DVM0
F03 B1
DVM1
F03 B1
DVM2
F03 B1
OUT2
F07 A4
OUT3
F07 B4
FGTST100
F01 B3
DVM_BAT
F03 C8
OPTDVM2
F01 B2

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


M***
ALIBRATION
ORK
-5V_ISO
VR1
LM320LZ-5.0
-12V
3
OUT
GND
IN
2
1
C15
.1
C16
22uf
+5V
A
VREF
F08 D3
3k
R3
.1%
R4
750
.1%
C9
.1
U4
ICL7109CPL
12V
DVM_RDY
F03 B1
U3
DG508BCJ
+5V
A0
A1
A2
EN
S1
S2
S3
S4
S5
S6
S7
S8
D
8
3
-12V
C10
220pf
R5
10k
N/C
C11
.1
C12
.056
R6
200k
R7
100k
C13
1.0
C14
.01
28 V-
21 MODE
2 STATUS
22 IN
23 OUT
OSC
24 SEL
25 BOSCOUT
27 SEND
31 AZ
32 INT
36 +
39 -
REFIN
30 BUF
35 HI
34 LO
IN
37 +
38 -
RCAP
29 REFOUT
33 COMMON
1 GND
V+ 40
CE/LOAD 20
TEST 17
POL 3
OR 4
HIGH ORDER
12 5
11 6
10 7
9 8
8 9
7 10
6 11
5 12
4 13
3 14
2 15
1 16
LOW ORDER
RUN/HOLD 26
LBEN 18
HBEN 19
QD7
QD6
QD5
QD4
QD3
QD2
QD1
QD0
C1 F03
DVMRUN
DVMLB
DVMHB
B1 F03

CAD JOB # B064E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 6/90
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

SCHEMATIC,
MOTHERBOARD

SIZE	FSCM NO.	DWG NO.	REV
D	23338	1104-00-3395	C

SCALE NONE | MODEL 90 SERIES | SHEET 2 OF 10

1104-00-3395

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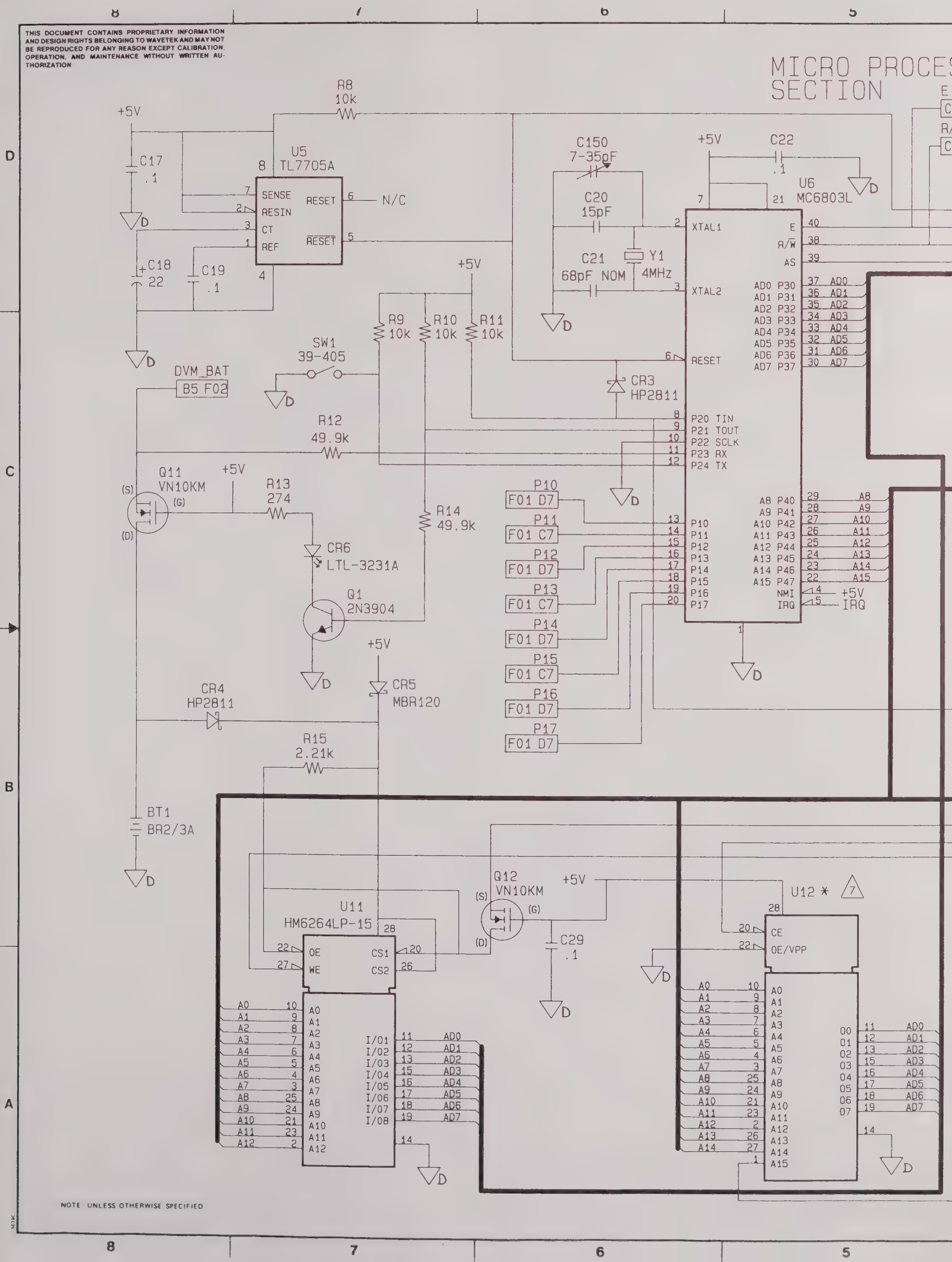
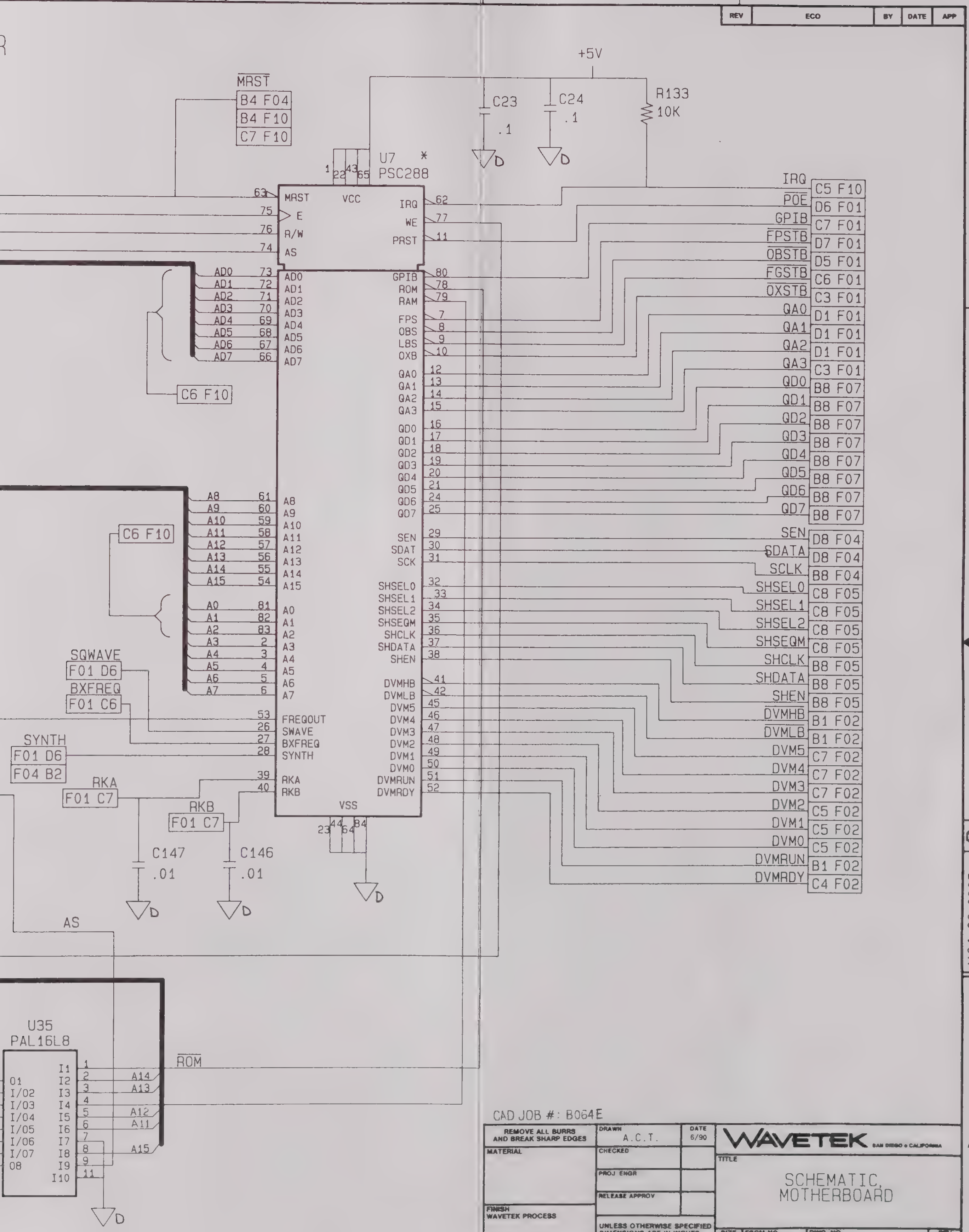
MICRO PROCES
SECTION



8
7
6
5
D
C
B
A
+5V
R8
10k
C17
.1
U5
TL7705A
SENSE
RESIN
CT
REF
RESET
RESET
N/C
C18
22
C19
.1
C150
7-35pF
C20
15pF
C21
68pF NOM
Y1
4MHz
C22
.1
U6
MC6803L
XTAL1
XTAL2
RESET
E
R/W
AS
AD0 P30
AD1 P31
AD2 P32
AD3 P33
AD4 P34
AD5 P35
AD6 P36
AD7 P37
P20 TIN
P21 TOUT
P22 SCLK
P23 RX
P24 TX
P10
P11
P12
P13
P14
P15
P16
P17
A8 P40
A9 P41
A10 P42
A11 P43
A12 P44
A13 P45
A14 P46
A15 P47
NMI
IRQ
+5V
IRQ
R9
10k
R10
10k
R11
10k
SW1
39-405
DVM_BAT
B5 F02
CR3
HP2811
R12
49.9k
Q11
VN10KM
(S)
(G)
(D)
R13
274
R14
49.9k
CR6
LTL-3231A
Q1
2N3904
F01 D7
F01 C7
CR4
HP2811
CR5
MBR120
R15
2.21k
BT1
BR2/3A
Q12
VN10KM
C29
.1
U11
HM6264LP-15
OE
WE
CS1
CS2
I/01
I/02
I/03
I/04
I/05
I/06
I/07
I/08
U12 *
7
CE
OE/VPP
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
00
01
02
03
04
05
06
07
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
D

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


+5V
C23
.1
C24
.1
R133
10K
MRST
B4 F04
B4 F10
C7 F10
U7 *
PSC288
1 22 43 65
63 MRST
75 E
76 R/W
74 AS
VCC
IRQ 62
WE 77
PRST 11
AD0 73
AD1 72
AD2 71
AD3 70
AD4 69
AD5 68
AD6 67
AD7 66
C6 F10
GPIB 80
ROM 78
RAM 79
FPS 7
OBS 8
LBS 9
OXB 10
QA0 12
QA1 13
QA2 14
QA3 15
QD0 16
QD1 17
QD2 18
QD3 19
QD4 20
QD5 21
QD6 24
QD7 25
A8 61
A9 60
A10 59
A11 58
A12 57
A13 56
A14 55
A15 54
A0 81
A1 82
A2 83
A3 2
A4 3
A5 4
A6 5
A7 6
SEN 29
SDAT 30
SCK 31
SHSEL0 32
SHSEL1 33
SHSEL2 34
SHSEQM 35
SHCLK 36
SHDATA 37
SHEN 38
DVMHB 41
DVMLB 42
DVM5 45
DVM4 46
DVM3 47
DVM2 48
DVM1 49
DVM0 50
DVMRUN 51
DVMRDY 52
SQWAVE
F01 D6
BXFREQ
F01 C6
53 FREQOUT
26 SWAVE
27 BXFREQ
28 SYNTH
SYNTH
F01 D6
F04 B2
39 RKA
40 RKB
RKA
F01 C7
RKB
F01 C7
VSS
23 44 64 84
C147
.01
C146
.01
D
AS
IRQ C5 F10
POE D6 F01
GPIB C7 F01
FPSTB D7 F01
OBSTB D5 F01
FGSTB C6 F01
OXSTB C3 F01
QA0 D1 F01
QA1 D1 F01
QA2 D1 F01
QA3 C3 F01
QD0 B8 F07
QD1 B8 F07
QD2 B8 F07
QD3 B8 F07
QD4 B8 F07
QD5 B8 F07
QD6 B8 F07
QD7 B8 F07
SEN D8 F04
SDATA D8 F04
SCLK B8 F04
SHSEL0 C8 F05
SHSEL1 C8 F05
SHSEL2 C8 F05
SHSEQM C8 F05
SHCLK B8 F05
SHDATA B8 F05
SHEN B8 F05
DVMHB B1 F02
DVMLB B1 F02
DVM5 C7 F02
DVM4 C7 F02
DVM3 C7 F02
DVM2 C5 F02
DVM1 C5 F02
DVM0 C5 F02
DVMRUN B1 F02
DVMRDY C4 F02
U35
PAL16L8
I1 1
I2 2
I3 3
I4 4
I5 5
I6 6
I7 7
I8 8
I9 9
I10 11
01
I/02
I/03
I/04
I/05
I/06
I/07
08
A14
A13
A12
A11
A15
ROM
4
3
2
1
D
C
B
A
1104-00-3395
D

CAD JOB #: B064E

REMOVE ALL BURRS AND SHARP EDGES

DRAWN	A.C.T.	DATE 6/90
CHECKED		
PROJ ENGR		
RELEASE APPROV		

MATERIAL

FINISH
WAVETEK PROCESS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
± XX ± ±
XXX ±

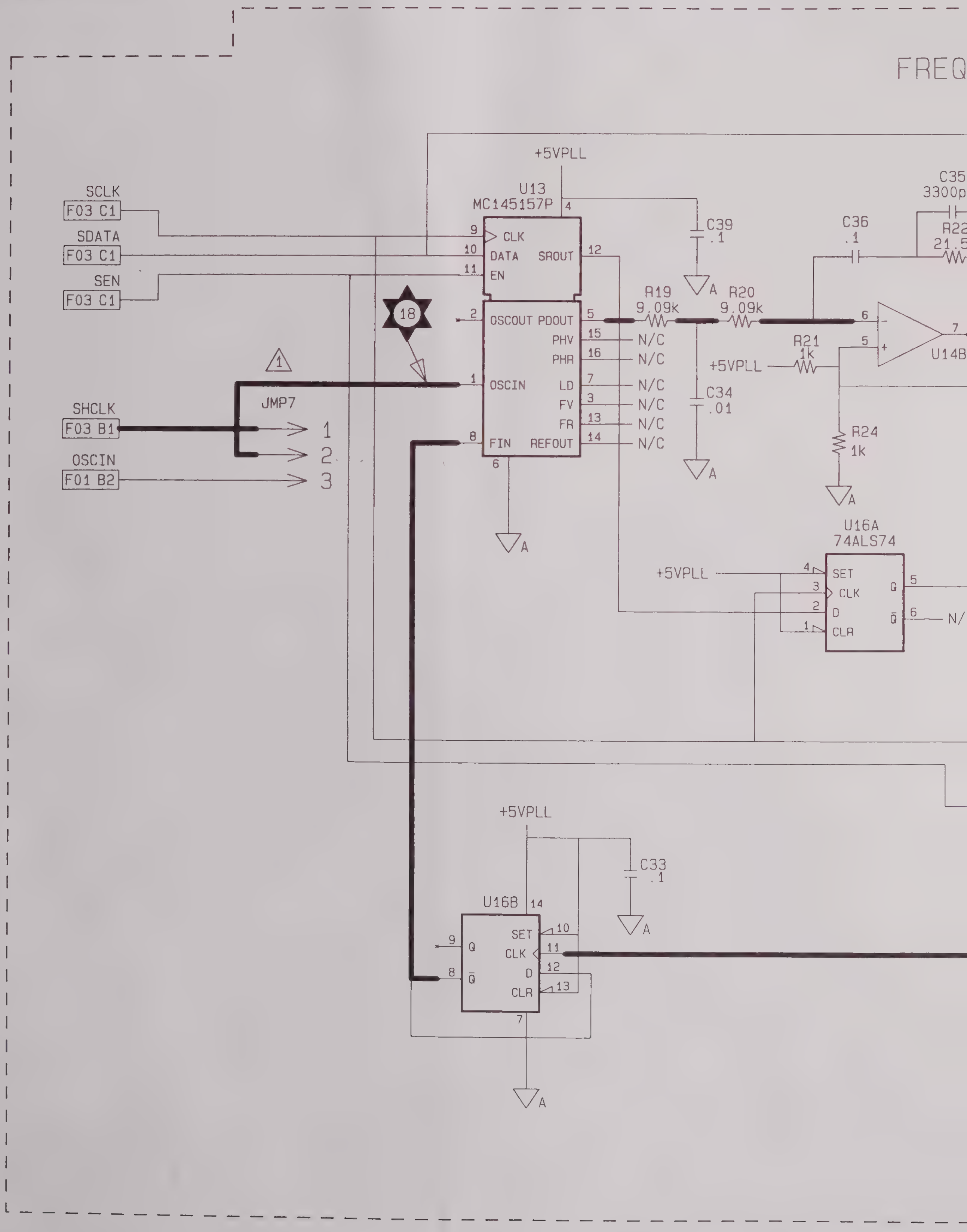
DO NOT SCALE DRAWING

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
MOTHERBOARD

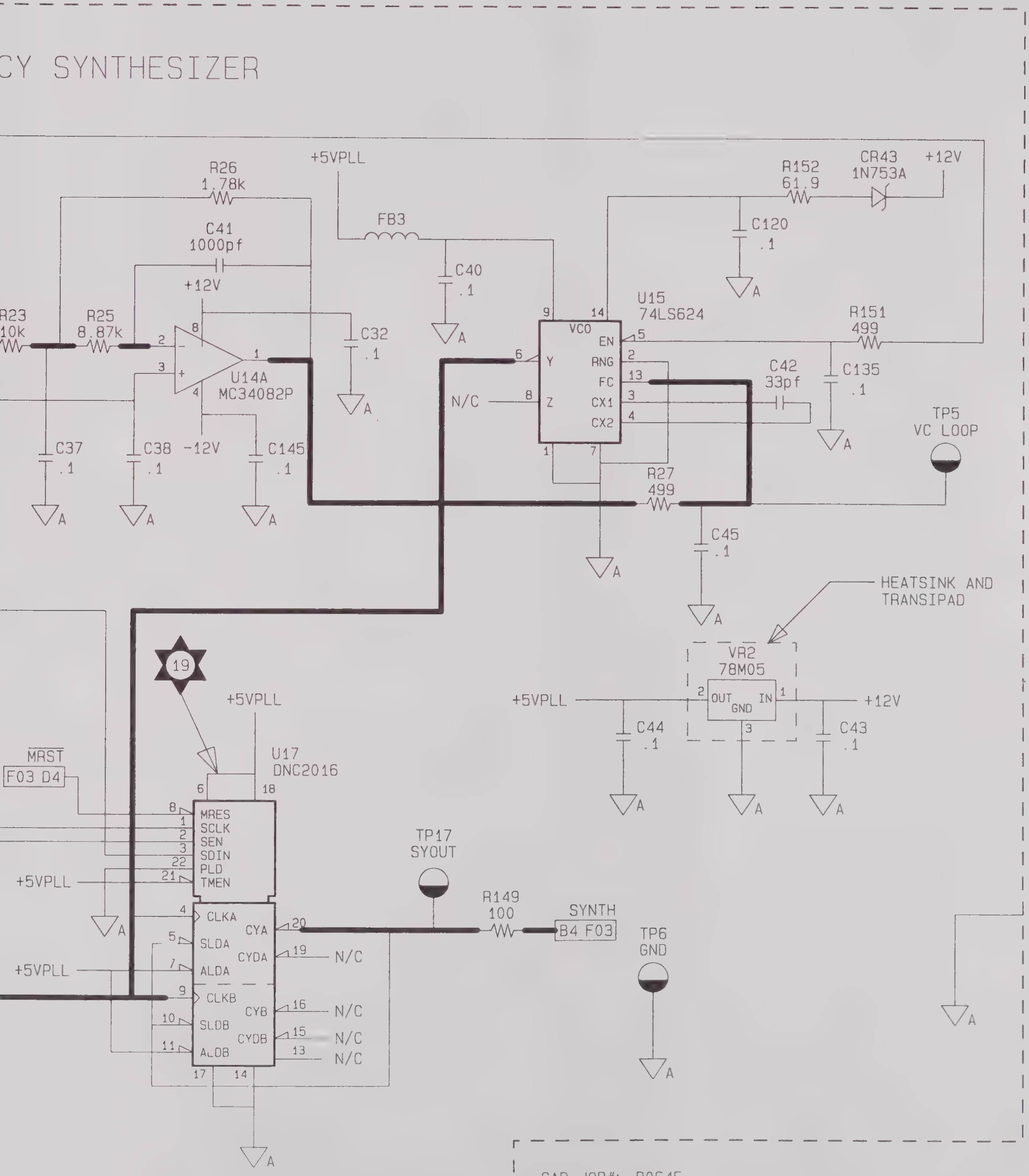
SIZE	FSCM NO	DWG. NO.	REV
D	23338	1104-00-3395	D

SCALE NONE | MODEL 90 SERIES | SHEET 3 OF 10


FREQ
+5VPLL
U13
MC145157P
SCLK
F03 C1
SDATA
F03 C1
SEN
F03 C1
CLK
DATA
EN
SROUT
OSCOUT
PDOUT
PHV
PHR
OSCIN
LD
FV
FR
FIN
REFOUT
N/C
18
1
JMP7
SHCLK
F03 B1
OSCIN
F01 B2
1
2
3
C39
.1
C34
.01
R19
9.09k
R20
9.09k
R21
1k
R24
1k
C35
3300p
C36
.1
R22
21.5
U14B
U16A
74ALS74
SET
CLK
D
CLR
Q
Q̄
N/
U16B
C33
.1
A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP



CY SYNTHESIZER
R26
1.78k
C41
1000pf
+5VPLL
FB3
C40
.1
+12V
R23
10k
R25
8.87k
U14A
MC34082P
C32
.1
C37
.1
C38
.1
-12V
C145
.1
A
U15
74LS624
VCO
EN
RNG
FC
CX1
CX2
Y
Z
N/C
R152
61.9
CR43
1N753A
C120
.1
R151
499
C42
33pf
C135
.1
TP5
VC LOOP
R27
499
C45
.1
HEATSINK AND
TRANSIPAD
VR2
78M05
OUT
IN
GND
C44
.1
C43
.1
19
U17
DNC2016
MRST
F03 D4
MRES
SCLK
SEN
SDIN
PLD
TMEN
CLKA
SLDA
ALDA
CLKB
SLDB
ALDB
CYA
CYDA
CYB
CYDB
TP17
SYOUT
R149
100
SYNTH
B4 F03
TP6
GND

CAD JOB#: B064E

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN RO FIFER DATE 10/90
CHECKED
PROJ ENGR
RELEASE APPROV

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX ·
XXX ·

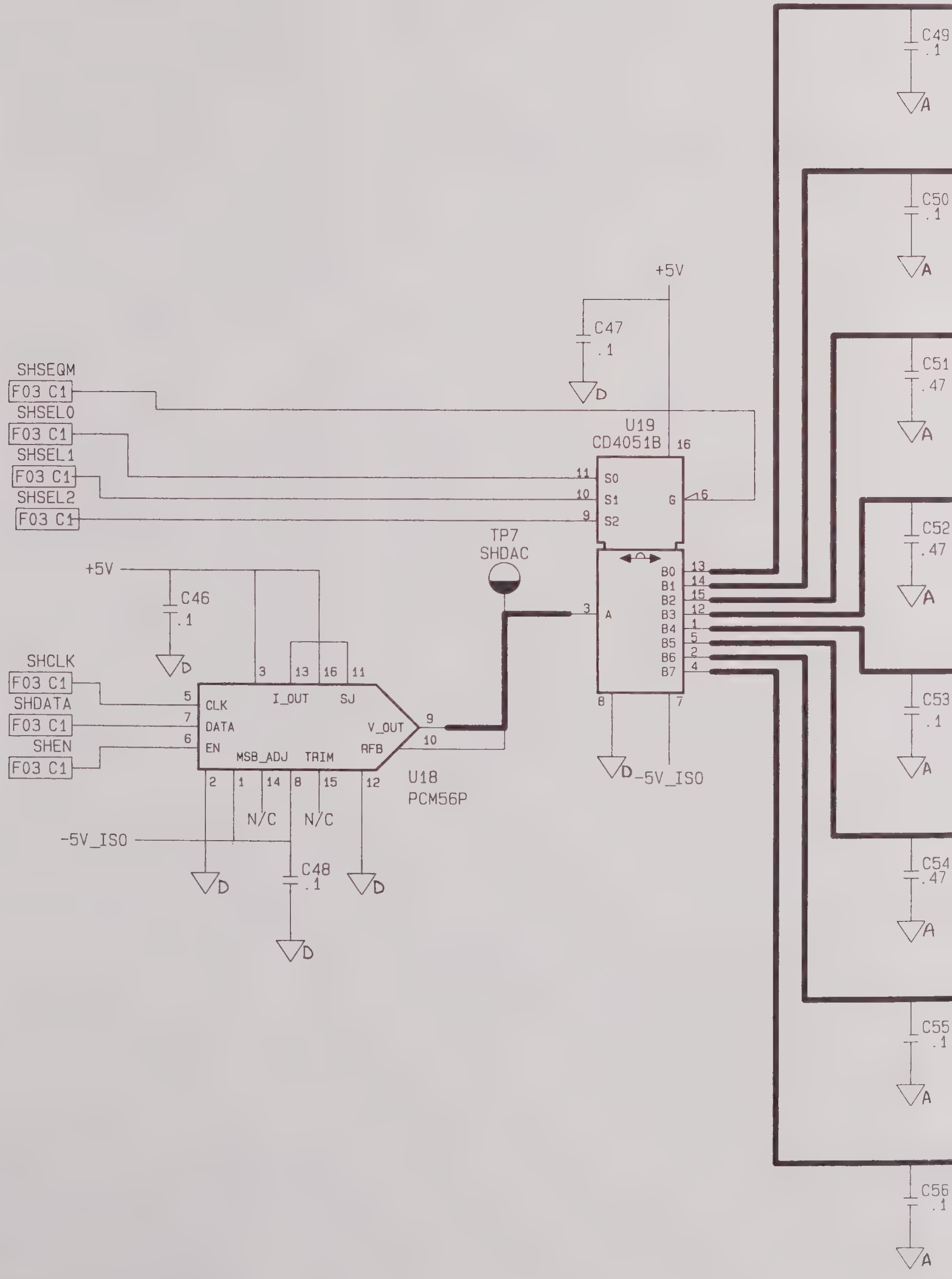
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
MOTHERBOARD

SIZE D FSCM NO 23338 DWG NO 1104-00-3395 REV

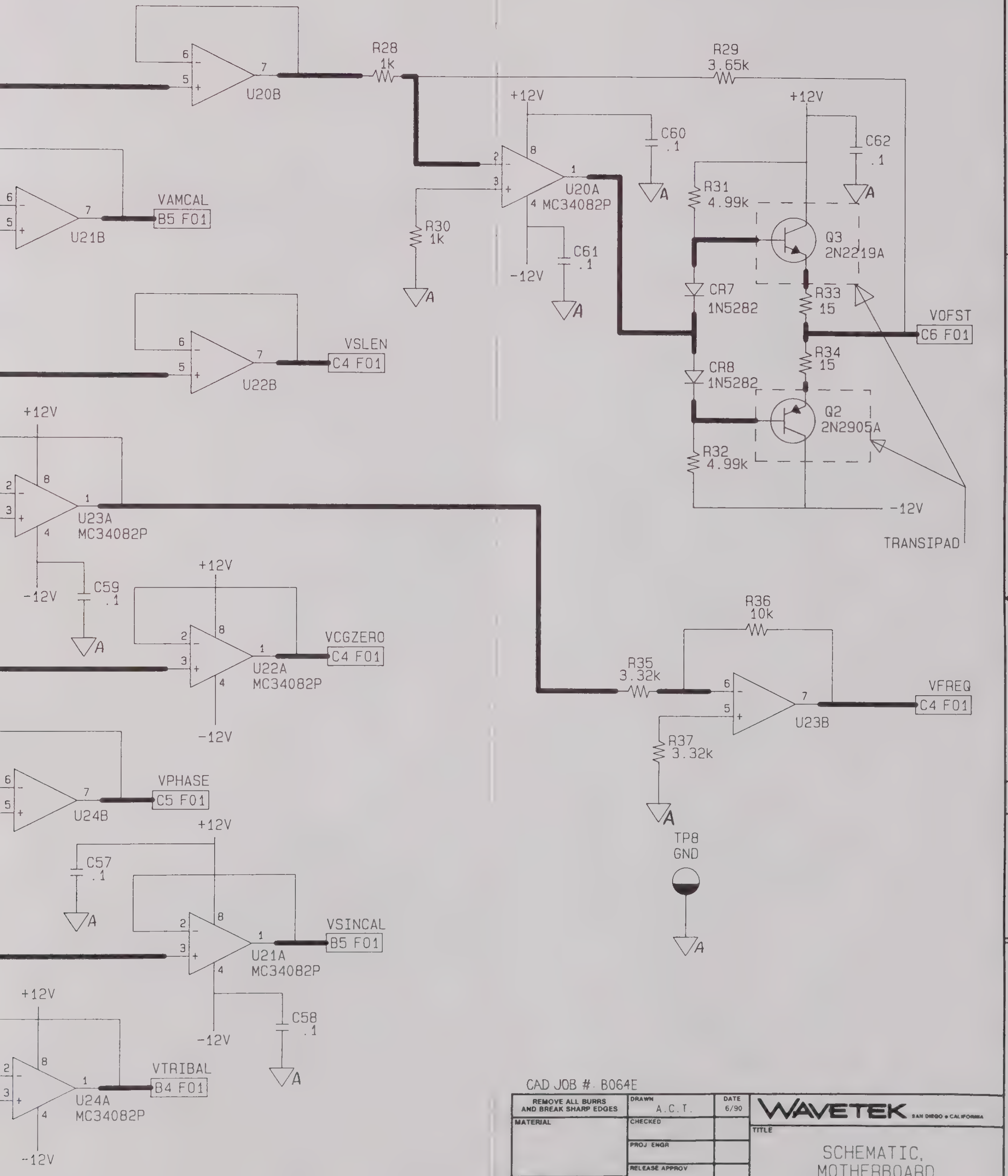
SCALE NONE MODEL 90 SERIES SHEET 4 OF 10

DAC/SAMPLE AND HOLD NETWORK


C49
.1
C50
.1
+5V
C47
.1
C51
.47
SHSEQM
F03 C1
SHSEL0
F03 C1
SHSEL1
F03 C1
SHSEL2
F03 C1
U19
CD4051B
16
11 S0
10 S1
9 S2
G
6
C52
.47
TP7
SHDAC
+5V
C46
.1
3 A
B0 13
B1 14
B2 15
B3 12
B4 1
B5 5
B6 2
B7 4
8
7
-5V_ISO
SHCLK
F03 C1
SHDATA
F03 C1
SHEN
F03 C1
5 CLK
7 DATA
6 EN
I_OUT
SJ
3
13
16
11
V_OUT 9
RFB 10
MSB_ADJ
TRIM
2
1
14
8
15
12
U18
PCM56P
N/C
N/C
-5V_ISO
C48
.1
C53
.1
C54
.47
C55
.1
C56
.1
D
A

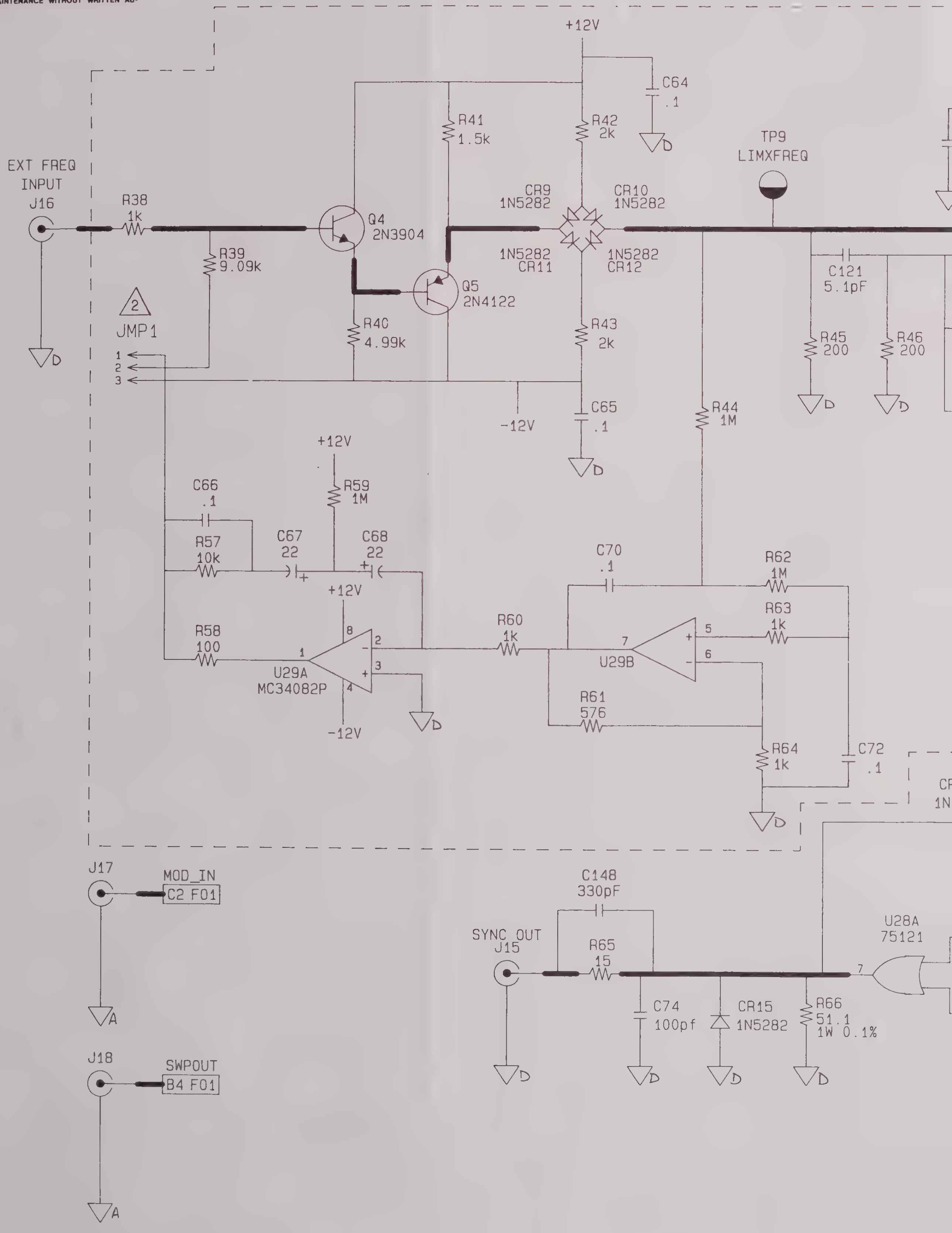
NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


U20B
R28
1k
R29
3.65k
+12V
C60
.1
+12V
C62
.1
U20A
MC34082P
C61
.1
-12V
R30
1k
R31
4.99k
Q3
2N2219A
CR7
1N5282
R33
15
VOFST
C6 F01
R34
15
CR8
1N5282
Q2
2N2905A
R32
4.99k
-12V
TRANSIPAD
VAMCAL
B5 F01
U21B
VSLEN
C4 F01
U22B
+12V
U23A
MC34082P
-12V
C59
.1
+12V
VCGZERO
C4 F01
U22A
MC34082P
-12V
R36
10k
R35
3.32k
VFREQ
C4 F01
U23B
R37
3.32k
VPHASE
C5 F01
U24B
+12V
C57
.1
VSINCAL
B5 F01
U21A
MC34082P
-12V
C58
.1
TP8
GND
+12V
VTRIBAL
B4 F01
U24A
MC34082P
-12V
D
C
B
A
D
1104-00-3395

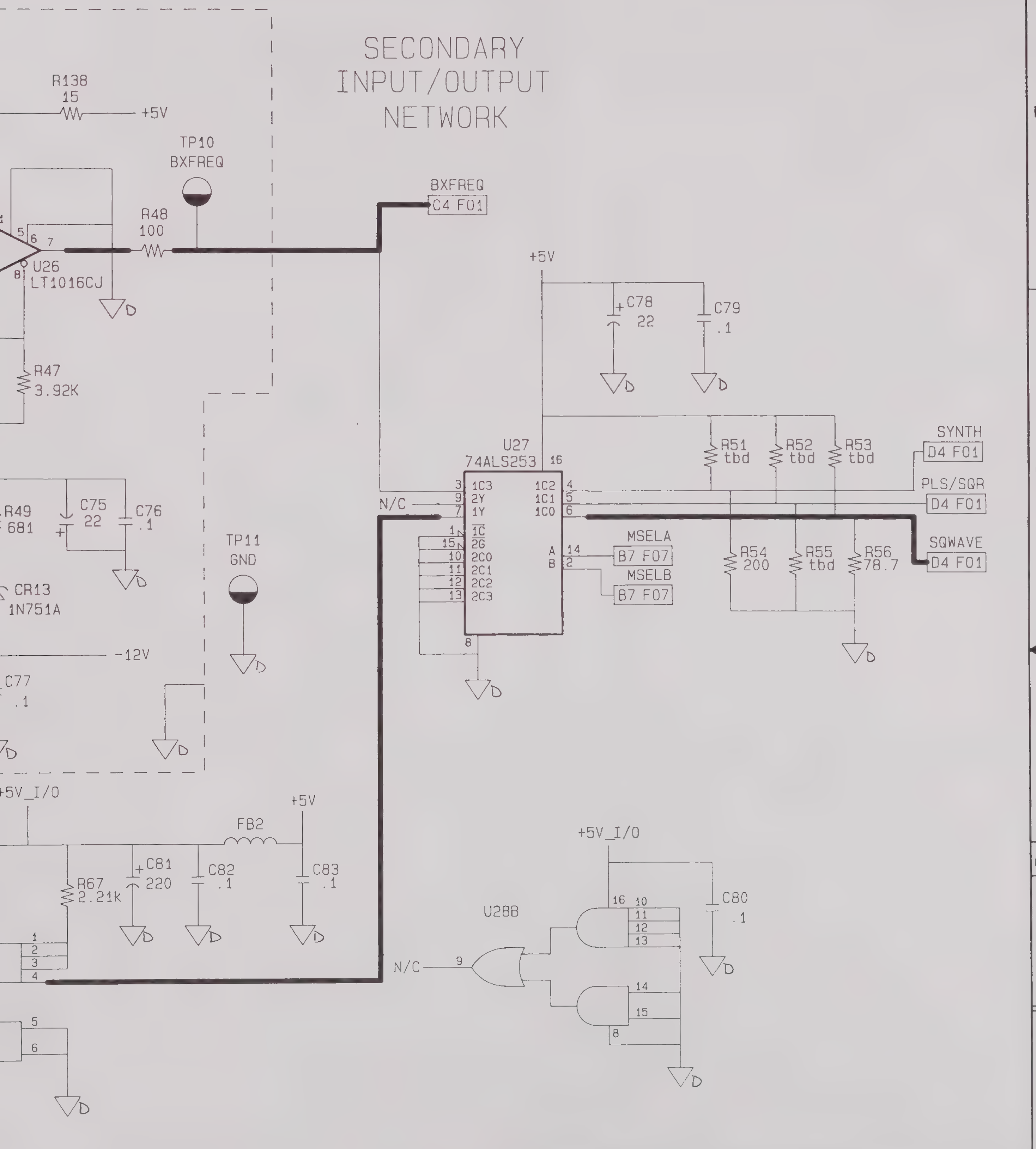
CAD JOB # B064E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 6/90	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	CHECKED		TITLE SCHEMATIC, MOTHERBOARD	
	PROJ ENGR			
	RELEASE APPROV			
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES XX : XXX :		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3395	REV D
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES	SHEET 5 OF 10



+12V
C64
.1
R41
1.5k
R42
2k
TP9
LIMXFREQ
EXT FREQ
INPUT
J16
R38
1k
CR9
1N5282
CR10
1N5282
Q4
2N3904
R39
9.09k
1N5282
CR11
1N5282
CR12
C121
5.1pF
Q5
2N4122
2
JMP1
R40
4.99k
R43
2k
R45
200
R46
200
1
2
3
C65
.1
-12V
R44
1M
+12V
R59
1M
C66
.1
R57
10k
C67
22
C68
22
C70
.1
R62
1M
+12V
R63
1k
R58
100
R60
1k
U29A
MC34082P
U29B
R61
576
-12V
R64
1k
C72
.1
J17
MOD_IN
C2 F01
C148
330pF
U28A
75121
SYNC OUT
J15
R65
15
C74
100pf
CR15
1N5282
R66
51.1
1W 0.1%
J18
SWPOUT
B4 F01
D
A

NOTE UNLESS OTHERWISE SPECIFIED


SECONDARY INPUT/OUTPUT NETWORK
R138
15
+5V
TP10
BXFREQ
R48
100
U26
LT1016CJ
BXFREQ
C4 F01
R47
3.92K
+5V
C78
22
C79
.1
U27
74ALS253
16
1C3
2Y
1Y
1C
2G
2C0
2C1
2C2
2C3
1C2
1C1
1C0
A
B
N/C
MSELA
B7 F07
MSELB
B7 F07
R51
tbd
R52
tbd
R53
tbd
R54
200
R55
tbd
R56
78.7
SYNTH
D4 F01
PLS/SQR
D4 F01
SQWAVE
D4 F01
R49
681
C75
22
C76
.1
TP11
GND
CR13
1N751A
-12V
C77
.1
+5V_I/O
+5V
FB2
R67
2.21k
C81
220
C82
.1
C83
.1
+5V_I/O
U28B
N/C
C80
.1
D

REV	ECO	BY	DATE	APP

CAD JOB #: B064E

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN A.C.T. DATE 6/90
CHECKED
PROJ ENGR.
RELEASE APPROV

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX -
XXX -

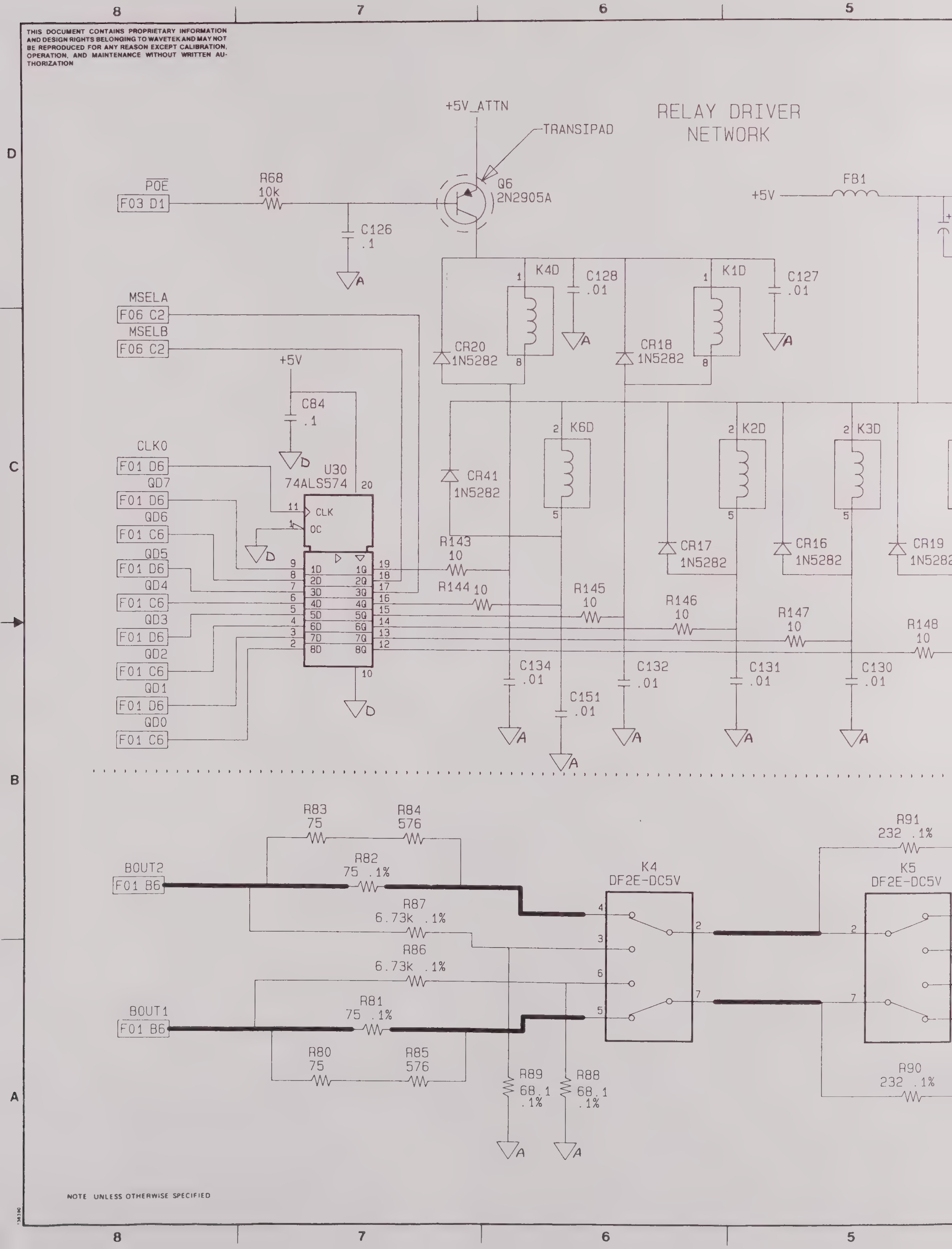
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
MOTHERBOARD

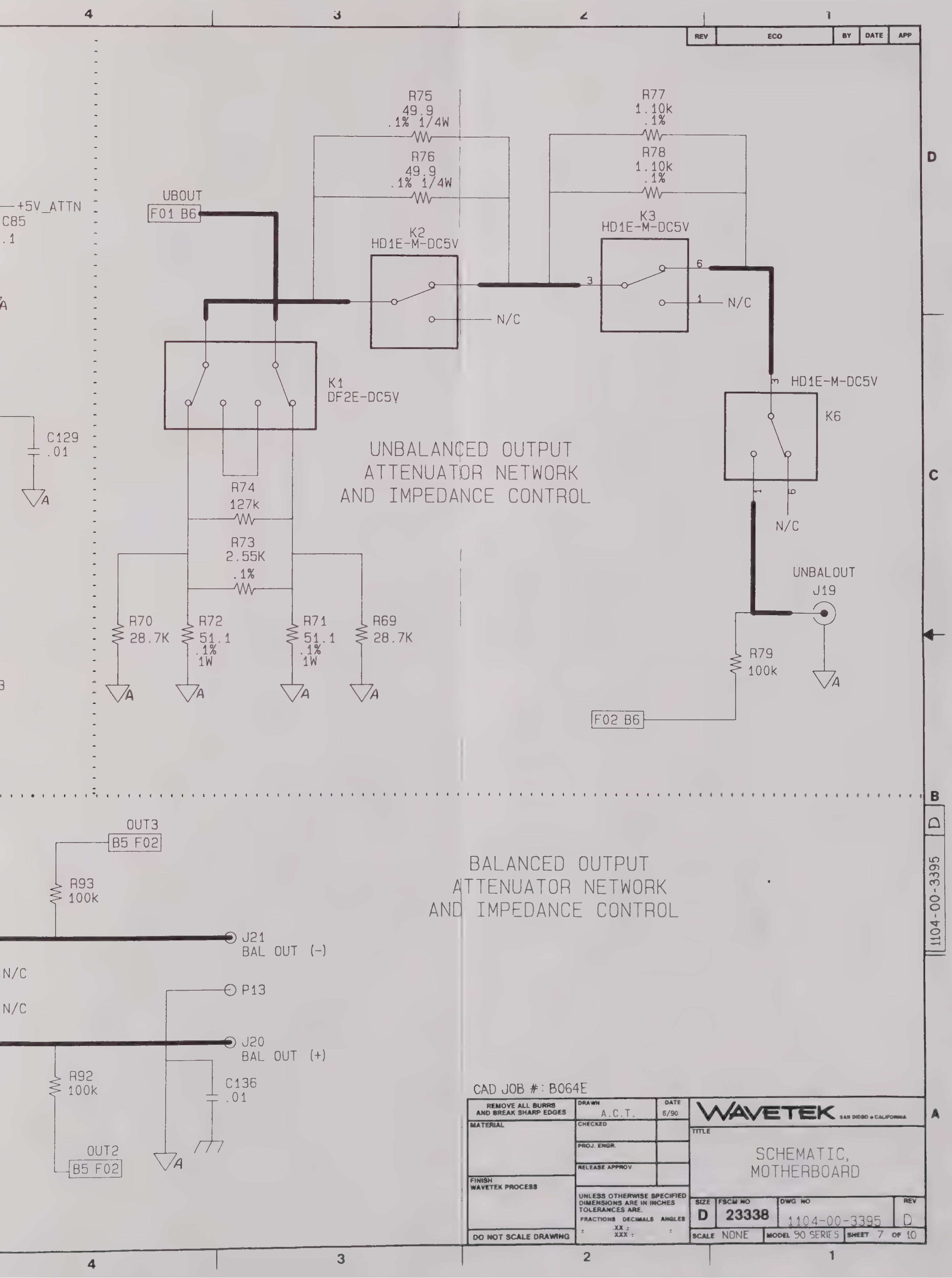
SIZE D
FSCM NO. 23338
DWG. NO. 1104-00-3395
REV D

SCALE NONE
MODEL 90 SERIES
SHEET 6 OF 10

1104-00-3395 D

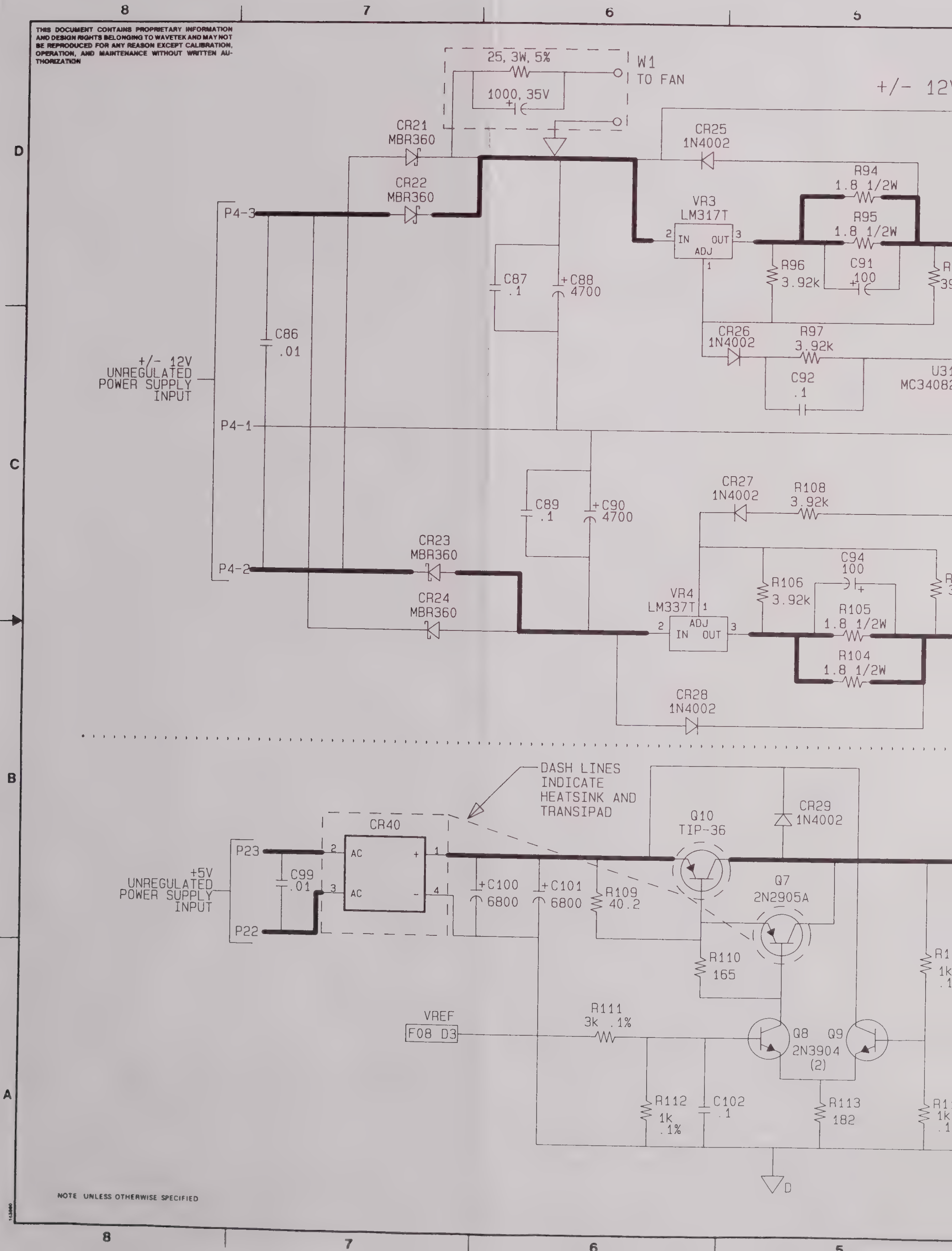

8
7
6
5
D
C
B
A
RELAY DRIVER NETWORK
+5V_ATTN
TRANSIPAD
Q6
2N2905A
POE
F03 D1
R68
10k
C126
.1
FB1
+5V
K4D
C128
.01
K1D
C127
.01
CR20
1N5282
CR18
1N5282
MSELA
F06 C2
MSELB
F06 C2
+5V
C84
.1
K6D
K2D
K3D
CLK0
F01 D6
QD7
F01 D6
QD6
F01 C6
QD5
F01 D6
QD4
F01 C6
QD3
F01 D6
QD2
F01 C6
QD1
F01 D6
QD0
F01 C6
U30
74ALS574
CLK
OC
CR41
1N5282
CR17
1N5282
CR16
1N5282
CR19
1N5282
R143
10
R144 10
R145
10
R146
10
R147
10
R148
10
C134
.01
C151
.01
C132
.01
C131
.01
C130
.01
R83
75
R84
576
R82
75 .1%
R87
6.73k .1%
R86
6.73k .1%
R81
75 .1%
R80
75
R85
576
BOUT2
F01 B6
BOUT1
F01 B6
K4
DF2E-DC5V
K5
DF2E-DC5V
R91
232 .1%
R90
232 .1%
R89
68.1
.1%
R88
68.1
.1%

NOTE UNLESS OTHERWISE SPECIFIED

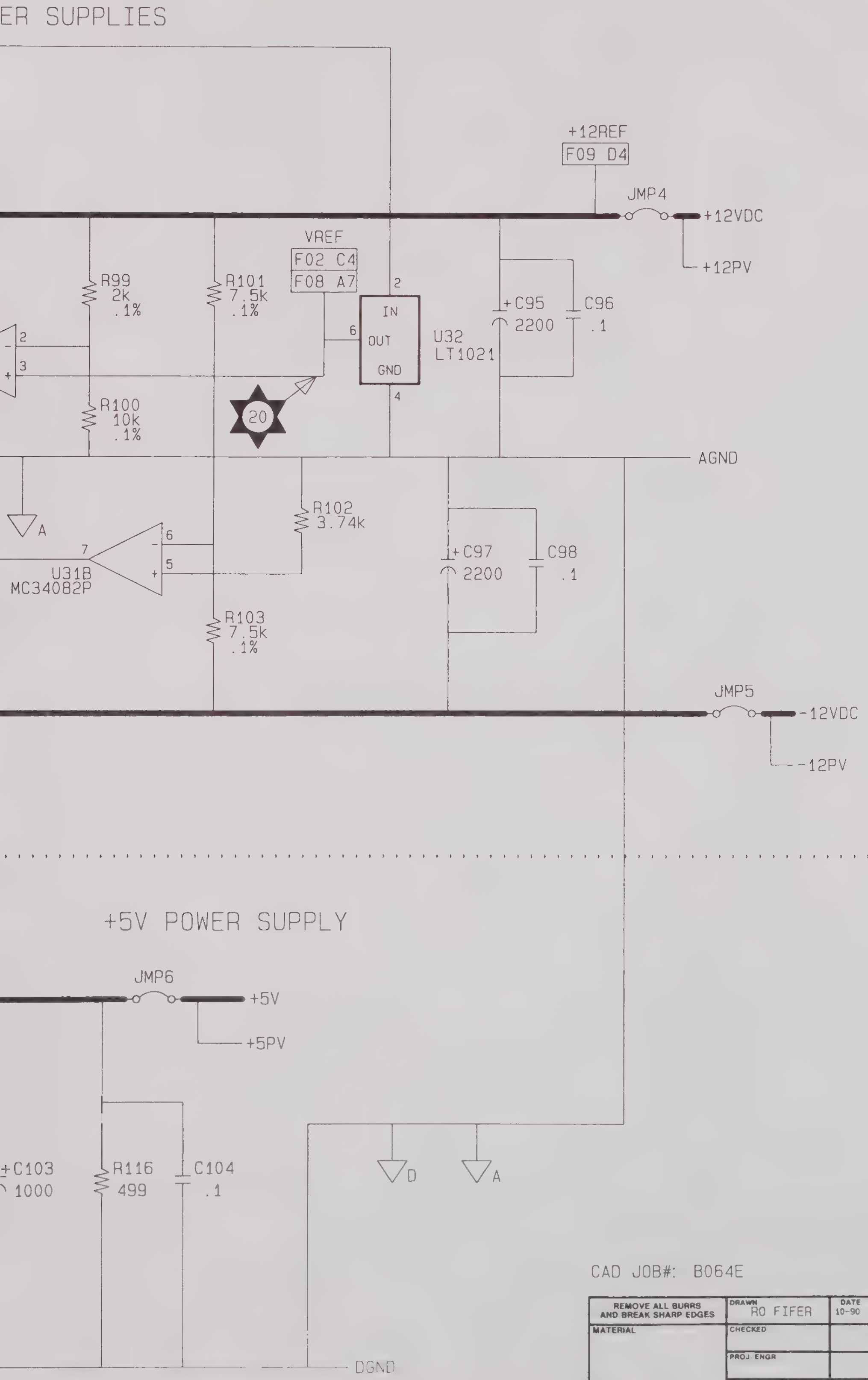

4
3
2
1
REV
ECO
BY
DATE
APP
D
C
B
A
+5V_ATTN
C85
.1
A
C129
.01
A
3
UBOUT
F01 B6
R75
49.9
.1% 1/4W
R76
49.9
.1% 1/4W
K2
HD1E-M-DC5V
N/C
R77
1.10k
.1%
R78
1.10k
.1%
K3
HD1E-M-DC5V
3
6
1
N/C
K1
DF2E-DC5V
R74
127k
R73
2.55K
.1%
R70
28.7K
R72
51.1
.1%
1W
R71
51.1
.1%
1W
R69
28.7K
A
A
A
A
3
HD1E-M-DC5V
K6
1
6
N/C
UNBALOUT
J19
R79
100k
A
F02 B6
UNBALANCED OUTPUT
ATTENUATOR NETWORK
AND IMPEDANCE CONTROL
OUT3
B5 F02
R93
100k
J21
BAL OUT (-)
N/C
N/C
P13
J20
BAL OUT (+)
R92
100k
C136
.01
A
OUT2
B5 F02
BALANCED OUTPUT
ATTENUATOR NETWORK
AND IMPEDANCE CONTROL
D
1104-00-3395

CAD JOB #: B064E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 6/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE SCHEMATIC, MOTHERBOARD
	PROJ. ENGR.		
	RELEASE APPROV		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO 23338 · DWG NO 1104-00-3395 · REV D
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES · SHEET 7 OF 10


8
7
6
5
D
C
B
A
25, 3W, 5%
1000, 35V
W1
TO FAN
+/- 12
CR21
MBR360
CR22
MBR360
CR25
1N4002
P4-3
VR3
LM317T
IN
OUT
ADJ
2
3
1
R94
1.8 1/2W
R95
1.8 1/2W
R96
3.92k
C91
100
C87
.1
C88
4700
C86
.01
CR26
1N4002
R97
3.92k
C92
.1
U31
MC3408
+/- 12V
UNREGULATED
POWER SUPPLY
INPUT
P4-1
CR27
1N4002
R108
3.92k
C89
.1
C90
4700
C94
100
CR23
MBR360
R106
3.92k
P4-2
VR4
LM337T
R105
1.8 1/2W
CR24
MBR360
R104
1.8 1/2W
CR28
1N4002
DASH LINES
INDICATE
HEATSINK AND
TRANSIPAD
CR29
1N4002
Q10
TIP-36
CR40
AC
+
AC
-
P23
C99
.01
+5V
UNREGULATED
POWER SUPPLY
INPUT
P22
C100
6800
C101
6800
R109
40.2
Q7
2N2905A
R110
165
VREF
F08 D3
R111
3k .1%
Q8
Q9
2N3904
(2)
R112
1k
.1%
C102
.1
R113
182
D
NOTE UNLESS OTHERWISE SPECIFIED

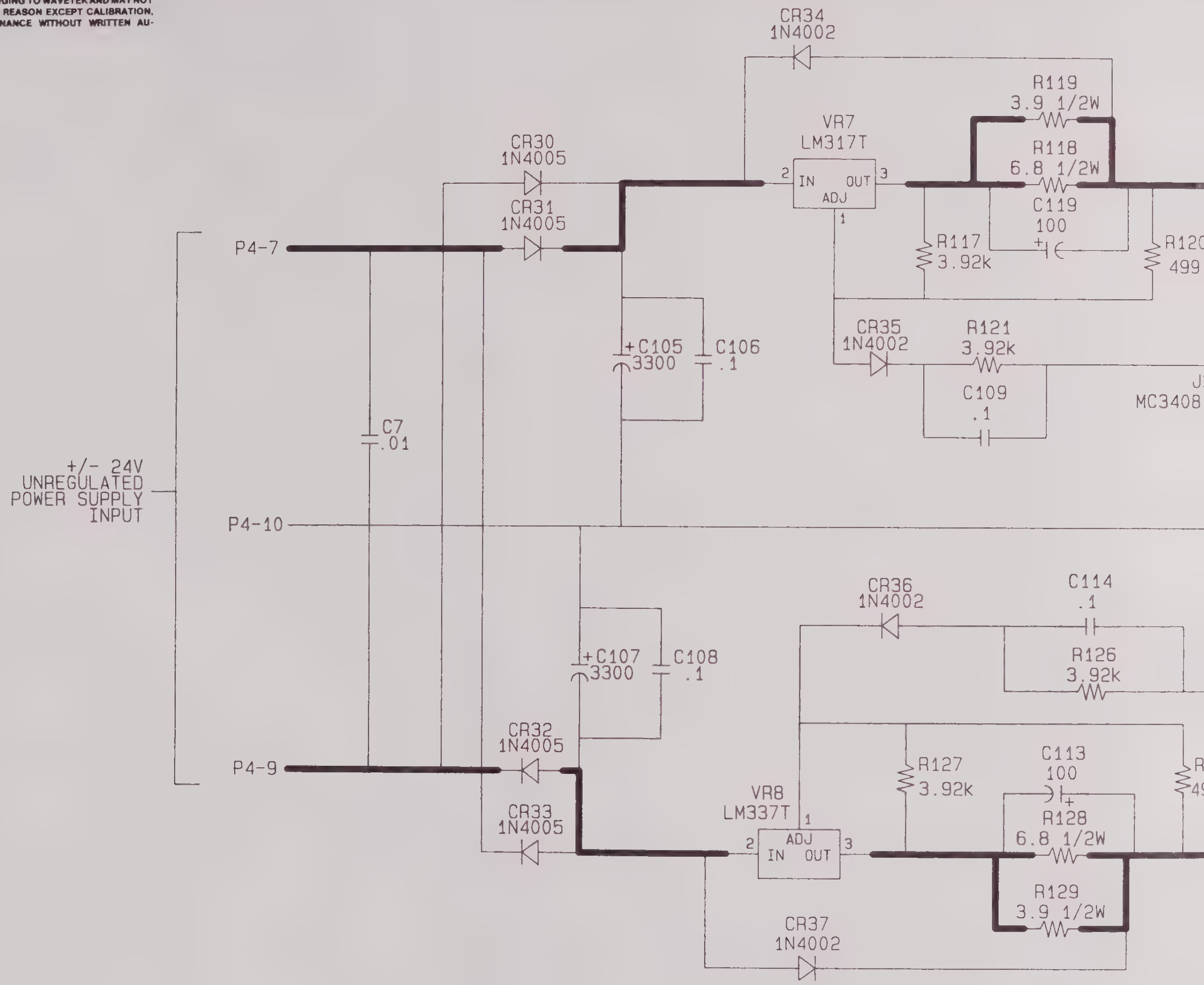
REV	ECO	BY	DATE	APP


ER SUPPLIES
+12REF
F09 D4
JMP4
+12VDC
+12PV
VREF
F02 C4
F08 A7
R99 2k .1%
R101 7.5k .1%
R100 10k .1%
IN
OUT
GND
U32 LT1021
+C95 2200
C96 .1
20
AGND
A
R102 3.74k
U31B MC34082P
+C97 2200
C98 .1
R103 7.5k .1%
JMP5
-12VDC
-12PV
+5V POWER SUPPLY
JMP6
+5V
+5PV
+C103 1000
R116 499
C104 .1
D
A
DGND

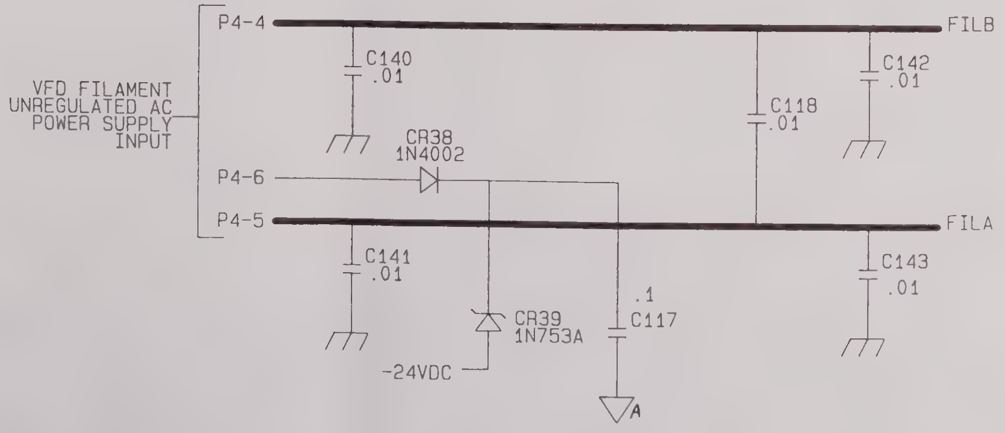
CAD JOB#: B064E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER	DATE 10-90	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	CHECKED		TITLE SCHEMATIC, MOTHERBOARD	
	PROJ ENGR			
	RELEASE APPROV			
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES XX ± XXX ±		SIZE D	FSCM NO 23338
			DWG NO. 1104-00-3395	REV
DO NOT SCALE DRAWING			SCALE NONE	MODEL 90
			SHEET 8 OF 10	

1104-00-3395 D


CR34
1N4002
R119
3.9 1/2W
VR7
LM317T
R118
6.8 1/2W
CR30
1N4005
2 IN OUT 3
ADJ 1
C119
100
CR31
1N4005
P4-7
R117
3.92k
R120
499
CR35
1N4002
R121
3.92k
C105
3300
C106
.1
C109
.1
MC3408
C7
.01
+/- 24V
UNREGULATED
POWER SUPPLY
INPUT
P4-10
CR36
1N4002
C114
.1
R126
3.92k
C107
3300
C108
.1
CR32
1N4005
P4-9
R127
3.92k
C113
100
VR8
LM337T
R128
6.8 1/2W
CR33
1N4005
2 ADJ 1
IN OUT 3
R129
3.9 1/2W
CR37
1N4002

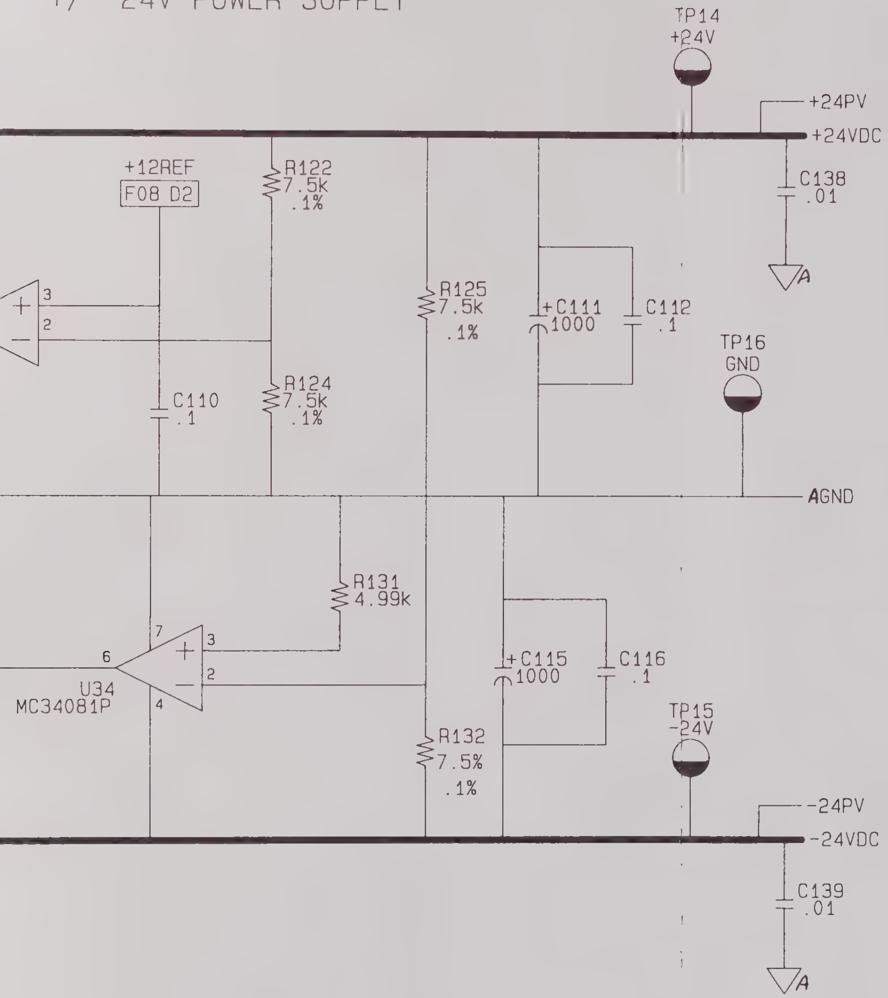
VFD AC FILAMENT SUPPLY


P4-4
FILB
C140
.01
C142
.01
VFD FILAMENT
UNREGULATED AC
POWER SUPPLY
INPUT
C118
.01
CR38
1N4002
P4-6
P4-5
FILA
C141
.01
C143
.01
.1
C117
CR39
1N753A
-24VDC
A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

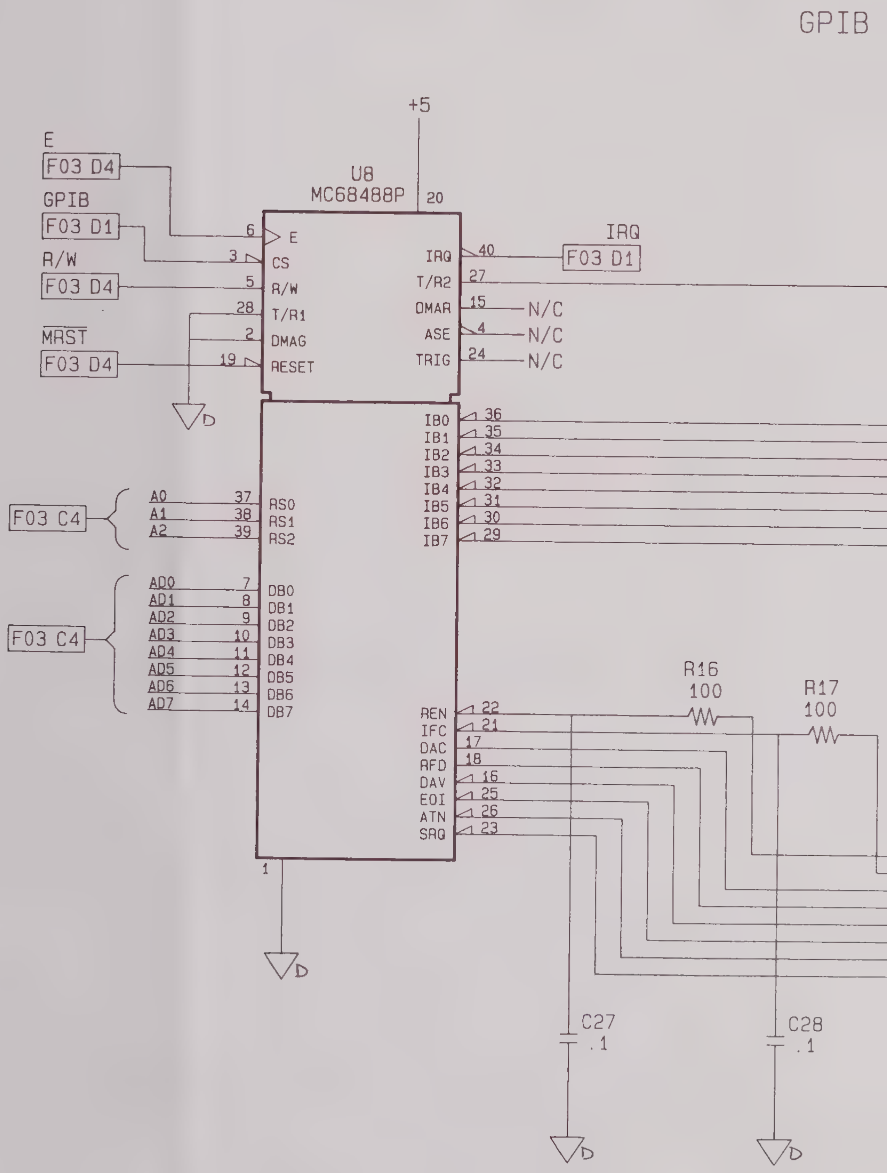
+/- 24V POWER SUPPLY


TP14
+24V
+24PV
+24VDC
C138
.01
A
+12REF
F08 D2
R122
7.5k
.1%
3
2
R125
7.5k
.1%
+C111
1000
C112
.1
TP16
GND
C110
.1
R124
7.5k
.1%
AGND
R131
4.99k
7
3
6
2
U34
MC34081P
4
+C115
1000
C116
.1
TP15
-24V
R132
7.5%
.1%
-24PV
-24VDC
C139
.01
A

1104-00-3395 D

CAD JOB #: B064E

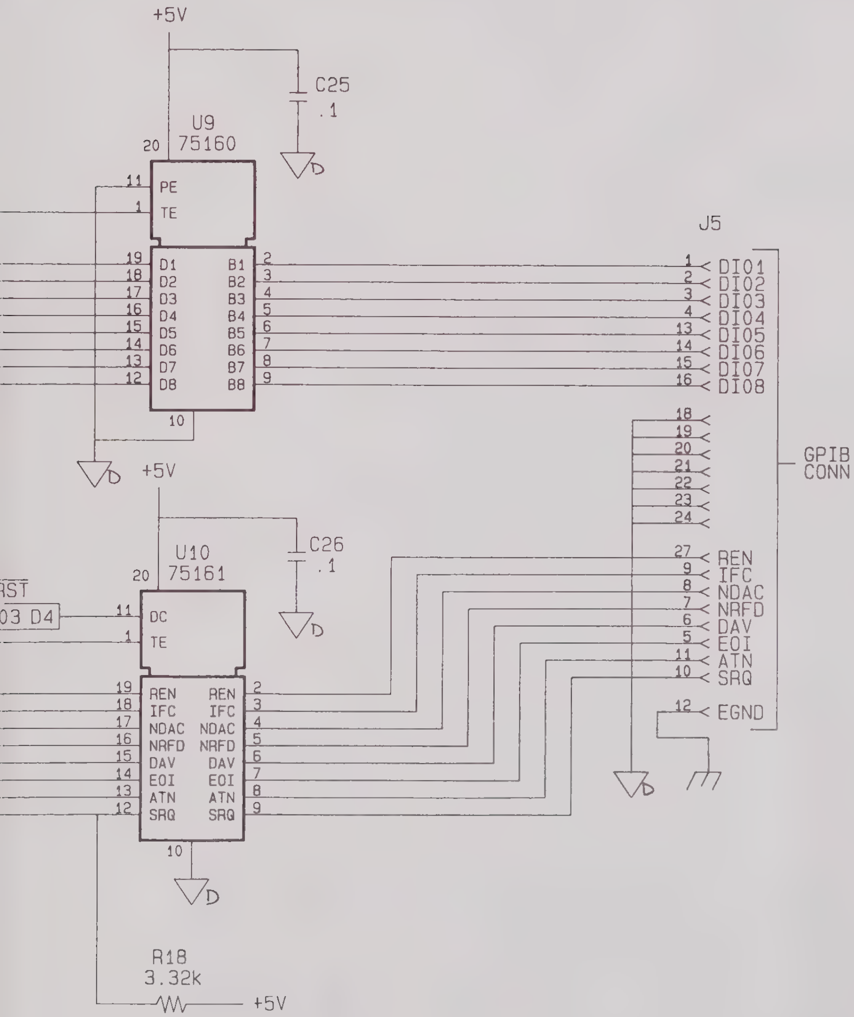
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 6/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE SCHEMATIC, MOTHERBOARD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3395 REV D
DO NOT SCALE DRAWING			SCALE NONE MODEL 90 SERIES SHEET 9 OF 10


GPIB
+5
U8
MC68488P
20
E
F03 D4
GPIB
F03 D1
R/W
F03 D4
MRST
F03 D4
6 E
3 CS
5 R/W
28 T/R1
2 DMAG
19 RESET
IRQ 40
T/R2 27
DMAR 15 N/C
ASE 4 N/C
TRIG 24 N/C
IRQ
F03 D1
F03 C4
A0 37 RS0
A1 38 RS1
A2 39 RS2
F03 C4
AD0 7 DB0
AD1 8 DB1
AD2 9 DB2
AD3 10 DB3
AD4 11 DB4
AD5 12 DB5
AD6 13 DB6
AD7 14 DB7
IB0 36
IB1 35
IB2 34
IB3 33
IB4 32
IB5 31
IB6 30
IB7 29
REN 22
IFC 21
DAC 17
RFD 18
DAV 16
EOI 25
ATN 26
SRQ 23
1
R16
100
R17
100
C27
.1
C28
.1
D

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

TION



+5V
C25
.1
U9
75160
20
11 PE
1 TE
19 D1
18 D2
17 D3
16 D4
15 D5
14 D6
13 D7
12 D8
B1 2
B2 3
B3 4
B4 5
B5 6
B6 7
B7 8
B8 9
10
J5
1 DIO1
2 DIO2
3 DIO3
4 DIO4
13 DIO5
14 DIO6
15 DIO7
16 DIO8
18
19
20
21
22
23
24
GPIB CONN
27 REN
9 IFC
8 NDAC
7 NRFD
6 DAV
5 EOI
11 ATN
10 SRQ
12 EGND
D
+5V
C26
.1
U10
75161
20
RST
03 D4
11 DC
1 TE
19 REN
18 IFC
17 NDAC
16 NRFD
15 DAV
14 EOI
13 ATN
12 SRQ
REN 2
IFC 3
NDAC 4
NRFD 5
DAV 6
EOI 7
ATN 8
SRQ 9
10
R18
3.32k
+5V

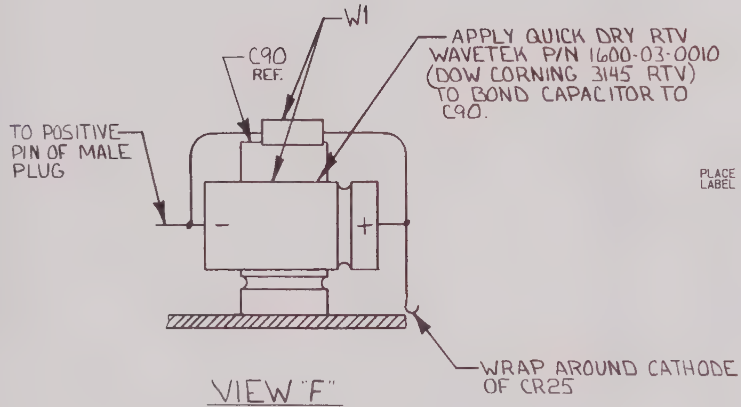
CAD JOB #: B064E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 5/90
MATERIAL	CHECKED	
	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±	
DO NOT SCALE DRAWING		

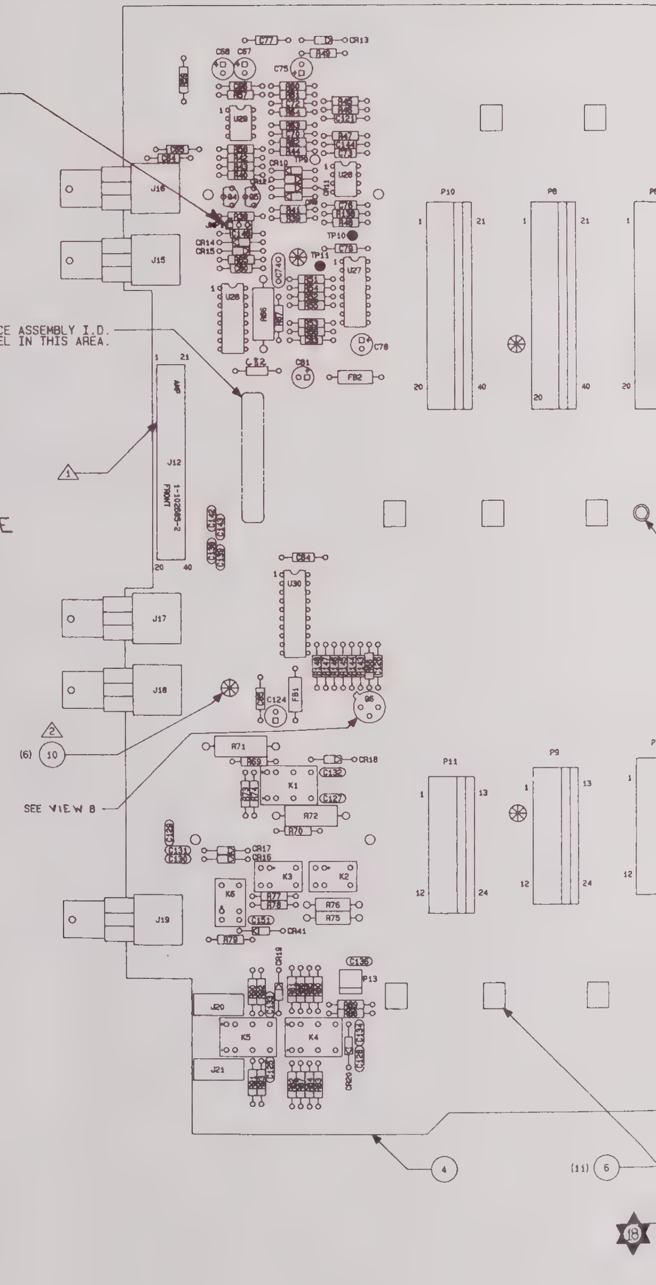
WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, MOTHERBOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3395	D
SCALE NONE	MODEL 90 SERIES	SHEET 10	OF 10


W1
C90
REF.
APPLY QUICK DRY RTV WAVETEK P/N 1600-03-0010 (DOW CORNING 3145 RTV) TO BOND CAPACITOR TO C90.
TO POSITIVE PIN OF MALE PLUG
−
+
WRAP AROUND CATHODE OF CR25

VIEW "F"
NO SCALE


SEE VIEW "G"
13
PLACE ASSEMBLY I.D. LABEL IN THIS AREA.
J16
J15
J12
1-102605-2 FRONT
AMP
J17
J18
J19
J20
J21
P10
P8
P11
P9
P13
U29
U28
U27
U26
U30
TP10
TP11
K1
K2
K3
K4
K5
K6
C77
C68
C67
C75
C78
C82
C81
C84
C124
C132
C127
C136
R49
R71
R72
R76
R75
R77
R78
R79
R69
R70
FB2
FB1
CR13
CR14
CR15
CR16
CR17
CR18
CR41
1
2
(6) 10
SEE VIEW B
4
(11) 6
18
1
20
21
40
12
13
24

13 INSTALL SHORTING JUMPER JMP1 BETWEEN PINS 1+2 (BIPOLAR CONFIGURATION).

12 INSTALL SHORTING JUMPER JMP7 ON PINS 1+2 FOR STD INSTRUMENT + PINS 2+3 FOR OPTION 001.

11 ATTACH FAN CABLE ASSY, W1, AS FOLLOWS. (SEE VIEW "F")
  A. RESISTOR/CAPACITOR END OF W1 TO CATHODE OF CR25.
  B. BLACK WIRE END OF W1 TO GND HOLE AS SHOWN.
  C. SECURE CAPACITOR TO C90 WITH RTV.

10. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.

9. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

8. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596 FOR MODEL 90 AND 1004-00-0599 FOR MODEL 95.

7. SEE 1104-00-3395 FOR SCHEMATIC.

6. COMPONENTS UNDER ITEM NO. 19 TO BE .465 MAX FROM SURFACE OF BOARD.

5. COMPONENTS UNDER ITEM NO. 18 TO BE .325 MAX FROM SURFACE OF BOARD.

4. INSTALL CLEAR RTV BETWEEEN CAPACITORS: C115-C107, C107-C111, C111-C105, C97-C90, C90-C88, C88-C95, C103-C100.

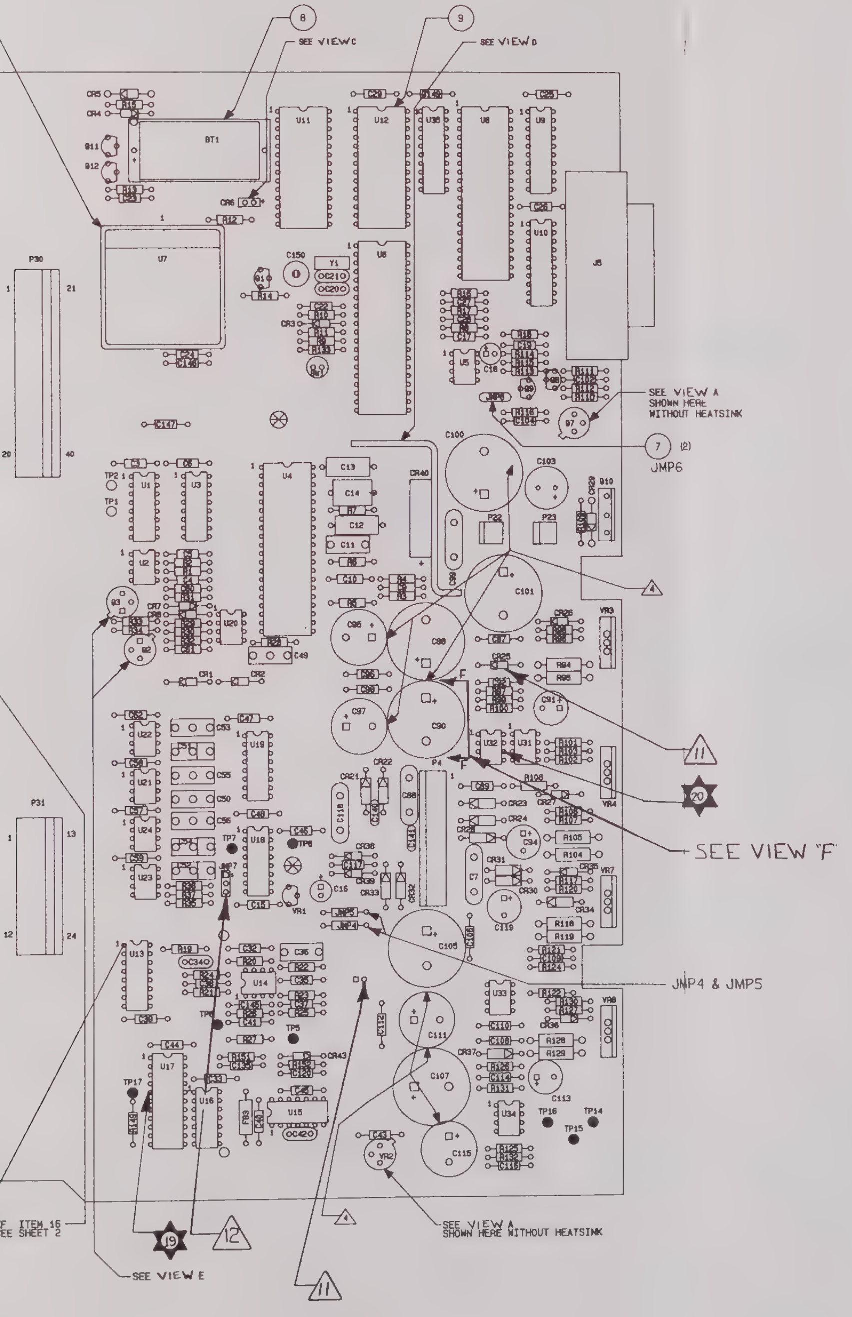
3. INSTALL CANS FLUSH TO COMPONENT SIDE OF P.C. BOARD. SOLDER TABS TO CIRCUIT SIDE.

2. ITEM 10 (SPACERS) TO BE INSTALLED FROM BOTTOM SIDE OF BOARD (CIRCUIT SIDE).

1. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

NOTE UNLESS OTHERWISE SPECIFIED

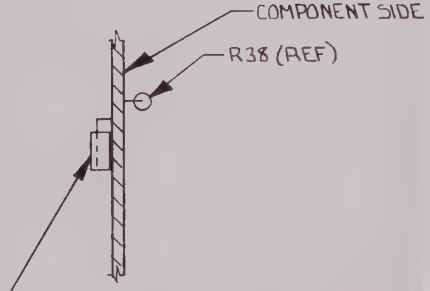
REV	ECO	BY	DATE	APP
A	ERO NO 90-441	DD	6/29/90	
B	ECO # 90-506	MS	9-14-90	YM
C	ECO # 90-521	MS	10/12/90	YM
D	ECO# 90-537	MS	10/23/90	
E	ECO# 91-116		1/31/91	


8
SEE VIEW C
9
SEE VIEW D
BT1
U7
P30
P31
U4
U8
J5
SEE VIEW A
SHOWN HERE
WITHOUT HEATSINK
7 (2)
JMP6
4
11
20
SEE VIEW "F"
JMP4 & JMP5
SEE VIEW A
SHOWN HERE WITHOUT HEATSINK
4
F ITEM 16
SEE SHEET 2
19
12
SEE VIEW E
11

CAD JOB #: B064E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/20/90	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	CHECKED D. FISH	6/29/90	TITLE PCA, MOTHERBOARD	
	PROJ. ENGR.	6/29/90		
	RELEASE APPROV	6/29/90		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE. FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D | FSCM NO. 23338 | DWG. NO. 1101-00-3395	REV E
DO NOT SCALE DRAWING			SCALE FULL | MODEL 90 SERIES	SHEET 1 OF 3

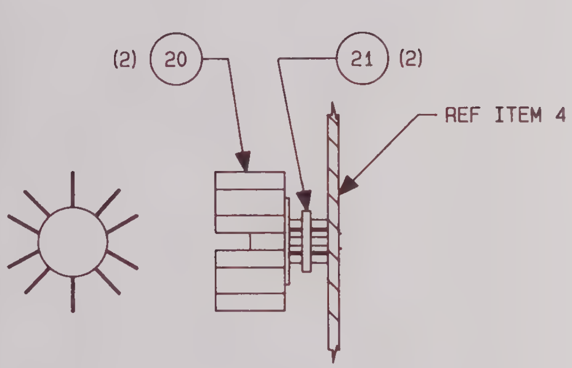
1101-00-3395


COMPONENT SIDE
R38 (REF)

INSTALL XJMP1 ON SOLDER SIDE OF BD. BEND TERMINALS AT RIGHT ANGLE AS SHOWN. BODY OF HEADER MUST BE FLUSH WITH BD.

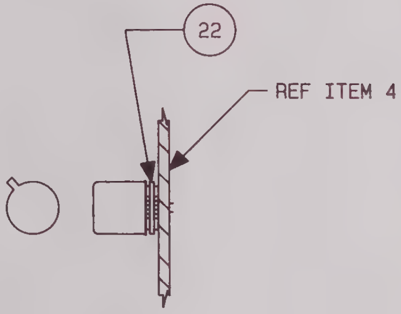
VIEW G

NOT TO SCALE


(2) 20
21 (2)
REF ITEM 4

VIEW A

SCALE = 2/1

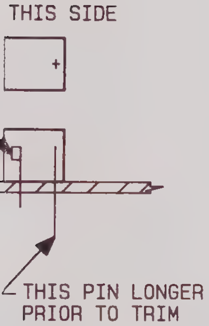

22
REF ITEM 4

VIEW B

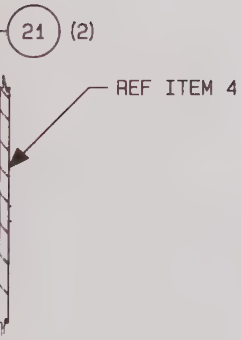
SCALE= 2/1

NOTE UNLESS OTHERWISE SPECIFIED

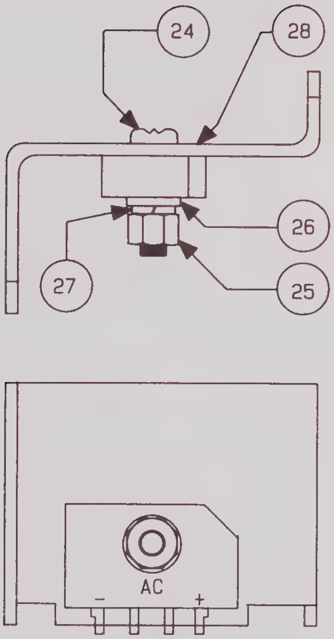
REV	ECO	BY	DATE	APP


THIS SIDE
+
THIS PIN LONGER
PRIOR TO TRIM

IEW C
TO SCALE


21 (2)
REF ITEM 4

E
/1

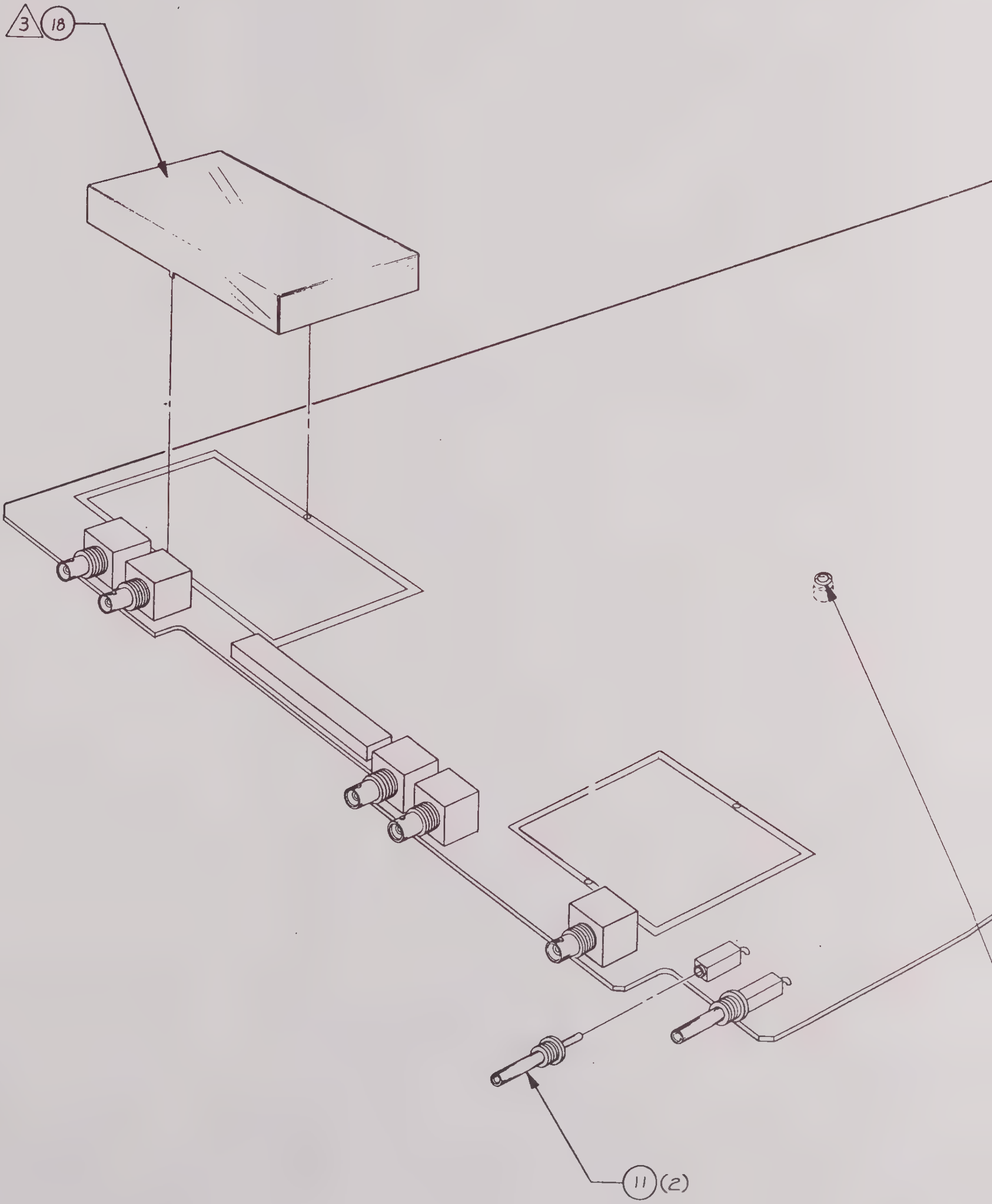

24
28
26
27
25
AC
−
+

VIEW D
SCALE = 2\1

CAD JOB #: B064E

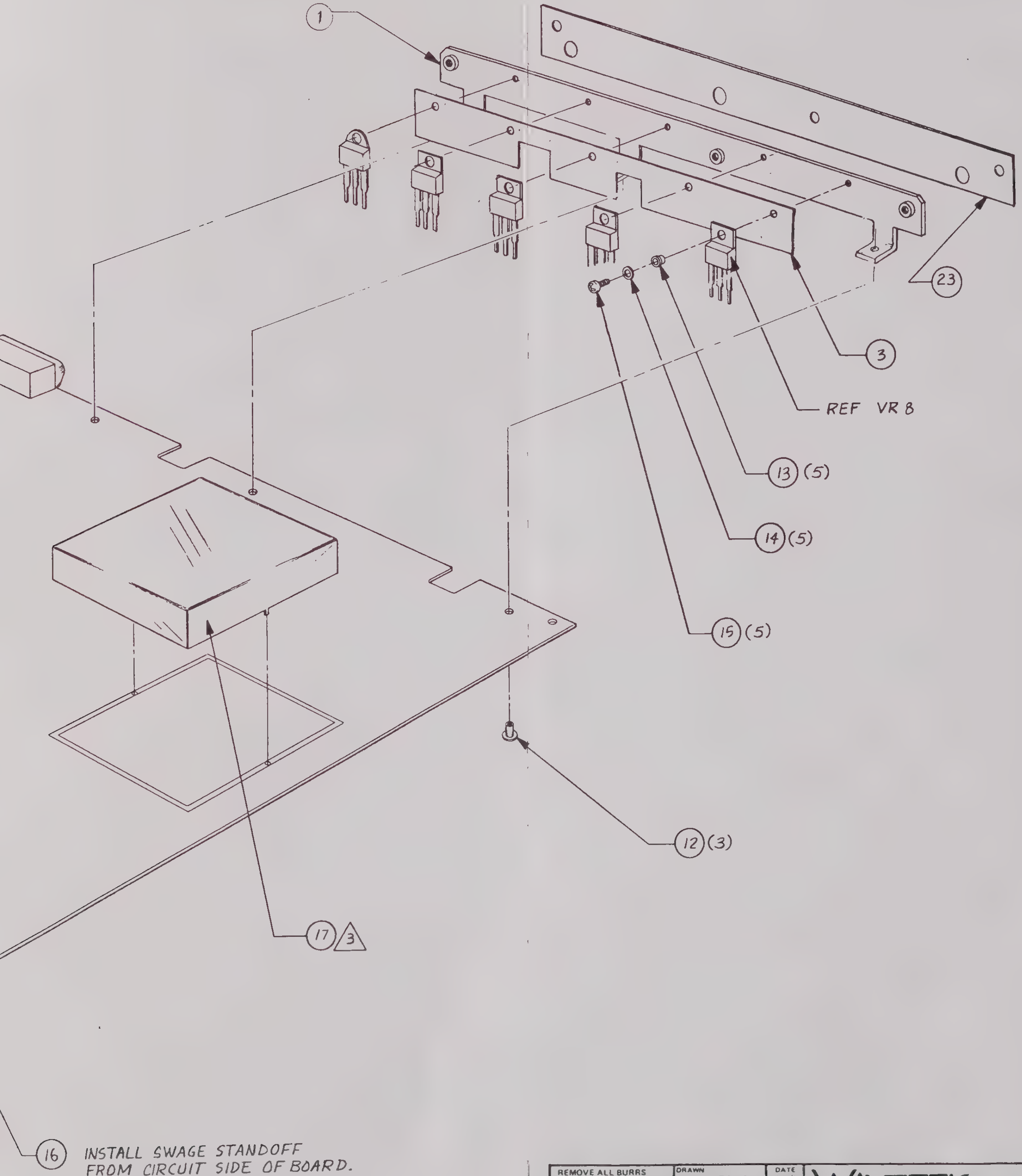
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6-25-90	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	CHECKED		TITLE PCA, MOTHERBOARD	
	PROJ. ENGR.			
	RELEASE APPROV.			
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1101-00-3395	REV E
DO NOT SCALE DRAWING			SCALE 2/1 · MODEL 90 SERIES	SHEET 2 OF 3

D
C
B
E
1101-00-3395
A


3
18
11 (2)
D
C
B
A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
	SEE SHEET #1			



INSTALL SWAGE STANDOFF FROM CIRCUIT SIDE OF BOARD.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S CHERMACK	DATE 6/20/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PCA, MOTHERBOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO. 90 SERIES — DWG NO. 1101-00-3395 — REV E
	SCALE NONE		CODE IDENT 23338 — SHEET 3 OF 3

115685

D

REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	A/D MOTHER BD 90/95
NONE	SCHEMATIC, PCA MOTHE BOARD MODEL 90
NONE	90/95 MOTHERBOARD PREWAVE LOAD
W1	FAN CABLE ASSY
17	CAN, SYNTHESIZER
18	CAN, FREQ IN/SYNC O
3	THERMAL GASKET-REAR PANEL-A
23	THERMAL GASKET-REAR PANEL-B
28	HEATSINK BRIDGE
1	SUPPPORT PLATE, TRANSISTOR
J15 J16 J17 J18 J19	CONN, BNC(PC)
XJMP1	CONN, HEADER, 3 PIN
JMP1 JMP7	JUMPER, FEMALE, 2 POSITION, 0.1 SPACE
20	HEAT SINK

WAVETEK
PARTS LIST

TITLE
PCA, MOTHER BOARD

C

B

A

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
-00-3395	WVTK	1101-00-3395	1
-00-3395	WVTK	1104-00-3395	1
-00-3390	WVTK	1200-00-3390	1
-00-3429	WVTK	1200-00-3429	1
-02-3443	WVTK	1400-02-3443	1
-02-3453	WVTK	1400-02-3453	1
-02-4400	WVTK	1400-02-4400	1
-02-4410	WVTK	1400-02-4410	1
-02-4463	WVTK	1400-02-4463	1
-02-5007	WVTK	1400-02-5007	1
1-1	AMP	2100-01-0019	5
4-01-03	APTRN	2100-02-0196	1
0-00	APTRN	2100-02-0213	2
	WAKE	2800-11-0001	2

ASSEMBLY NO. 1100-00-3390 REV K

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
13	WASHER	5607-150	SESTM	2800-11-0015	5
12	RIVET, 1/8 BODY DIA, 1/8-3/16 GRIP SS	SSD43SSBS	EMHRT	2800-12-0055	3
25	NUT, HEX, 6-32, Z	MS35649-264	COML	2800-14-6100	1
26	WASHER #6 SAE FLAT, .375 O.D.	6 SAE FLAT WASHER	CMRCL	2800-26-6000	1
10	HOLE PLUG, BINDER HEAD, NTRAL NYLON	207-120241-03-0101	FASTX	2800-35-0009	6
27	#6 LOCKWASHER, PLATED	#6SRLW	CMRCL	2800-42-6000	1
14	WASHER, LOCK REG, S/S #4	MS 35338-135	CMRCL	2800-45-4000	5
15	SCREW PLPS PAN M/S 18-8 S/S 4-40X1/4	MS 51957-13	CMRCL	2800-48-4104	5
24	SCREW, PH, PHLPS, 6-32X9/16, SS	2800-61-6109	CMCRL	2800-61-6109	1
Q10	TRANS	TIP-36	TI	4902-00-0360	1
VR3 VR7	VOLT REGULATOR, 3 TERMINAL ADJUSTABLE POS	LM317T	NSC	7000-03-1700	2
VR4 VR8	VOLT REGULATOR	LM337T	NSC	7000-03-3700	2

WAVETEK PARTS LIST

TITLE PCA, MOTHER BOARD

ASSEMBLY NO. 1100-00-3390 REV K

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U12	EPROM, PROG USEA 1 EA 8002-75-1200 FOR MOD 95 V1.3 REF U12	8600-00-0656	WVTK	8600-00-0656	1

WAVETEK PARTS LIST

TITLE PCA, MOTHER BOARD

ASSEMBLY NO. 1100-00-3390 REV K

PAGE 3

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE PARTS LIST MOTHERBOARD
	PROJ. ENGR.		
	RELEASE APPROV		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ±		SIZE D FSCM NO. 23338 DWG. NO. 1100-00-3390 REV K
DO NOT SCALE DRAWING			SCALE MODEL 95 SHEET 1 OF 1

D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PCA MOTHER BOARD MODEL 90	1104-00-3395	WVTK	1104-00-3395	1
VR1	Q: N.V. REG 5V (79L05)	LM320LZ-5.0	NSC	120.0054	1
CR39 CR43	SL ZR 6.2V 5% 400MW (1N753A)	1N753A	ROHM	131.9620	2
C74	CAP CER MON 100PF 50V COG 5% RAD LD SP .2	5028E050RD101J	KYCRA	1500-01-0103	1
C41	CAP, CER, .001MF, 100V	SA101C102MAATR	AVX	1500-01-0206	1
C118 C7 C86 C99	CAP, CER, .01MF, 1KV	GAP-103	CRL	1500-01-0309	4
C146 C147	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	2
C127 C128 C129 C130 C131 C132 C133 C134 C136 C138 C139 C140 C141 C142 C143 C151 C34	CAP CER MON .01MF 50V Z5U +80/-20% RAD LD .2	1C20Z5U103M050B	SPRAG	1500-01-0311	17
C102 C104 C106 C108 C109 C110 C112 C114 C116 C117 C120 C126 C135 C145 C149 C15 C17 C19 C22 C23 C24 C25 C26 C27 C28 C29 C3 C32 C33 C37 C38 C39 C4 C40 C43 C44 C45 C46 C47 C48 C5 C57 C58 C59 C6 C60 C61 C62 C64 C65 C66 C70 C72 C73 C76 C77 C79	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	68

WAVETEK
PARTS LIST
TITLE
90/95 MOTHERBOARD PREWAVE LOAD
ASSEMBLY NO. 1200-00-3390
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REV
E

REFERENCE DESIGNATORS	PART DESCRIPTION
C81	CAP, ELECT, 220MF/10V
C124 C16 C18 C67 C68 C75 C78	CAP, ELECT, 22MF, 25V, R DIAL
C95 C97	CAP, ELECT, 2200MF, 16V RADIAL LEAD, SP .30
C105 C107	CAP, ELECT, 3300MF, 50V RADIAL LEAD, SP .40
C88 C90	CAP, ELECT, 4700MF/25V RADIAL LEAD, SP .50
C100 C101	CAP, ELECT, 6800MF, 16V RADIAL LEAD, SP .50
C14	CAP, POLYC, .01MF, 100V AXIAL
C11 C36 C49 C50 C53 C55 C56	C05 CAP, MET POLY, .1MF, 100V/160V DC, .4 LS
C13	CAP, MYLAR, 1MF, 100V, DIAL
C51 C52 C54	CAP, MET-POLY, 5%.47M 63V RADIAL LEAD SP
C12	CAP, POLYPRO, .056MF, 0V, 2%, AXIAL

WAVETEK
PARTS LIST
TITLE
90/95 MOTHERBOARD PREWAV

C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C80 C82 C83 C84 C85 C87 C89 C9 C92 C96 C98					
C20	CAP CER MON 15PF 50V COG 5% RADIAL LD SP .2	5028E050RD150J	KYCRA	1500-01-5003	1
C10	CAP, CER, 220PF, 100V, AXIAL	CAC02CG221J100A	CORNG	1500-02-2106	1
C42	CAP CER MON 33PF 50V COG 5% RAD LD .2	5028E050RD330J	KYCRA	1500-03-3020	1
C148	CAP, CER, 330PF, 100V, AXIAL	CAC02CG331J100A	CORNG	1500-03-3106	1
C35	CAP, CER, 3300PF, 100V, 20%, AXIAL	CAC02X7R332M100A	CORNG	1500-03-3206	1
C121	CAP, CER, 5.1PF, 200V, AXIAL	SA102A5R1DAA	AVX	1500-05-1906	1
C21	CAP, CERAMIC, 68PF, 100V, 5%, RAD LEAD .2	SR211A680JAA	AVX	1500-06-8016	1
C113 C119 C91 C94	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	4
C111 C115	CAP, ELECT, 1000MF/50V RADIAL LEAD, SP .30	NRE102M50V16X25	NIC	1500-31-0203	2
C103	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	NRE102M16V10X20	NIC	1500-31-0211	1

WAVETEK
PARTS LIST
TITLE
90/95 MOTHERBOARD PREWAVE LOAD
ASSEMBLY NO. 1200-00-3390
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REFERENCE DESIGNATORS	PART DESCRIPTION
C150	CAP, VAR, 7-35PF 250
NONE	PCB, MOTHER BD
P4	CONN, HEADER
J20 J21	PC JACK
NONE	CONN, HEADER, 3 PIN
J12	CONN, HEADER, 40 PIN, RECPT, 2X20, .1 C PCMT
P11 P31 P7 P9	CONN, HEADER, 24 PIN, PCMT, .1 CTR, 2X12, SHRD
P10 P30 P6 P8	CONN, HEADER, 40 PIN, PCB MT, .1 CTR, 2X20, SHRD
J5	CONN, RECP, GPIB, 24PO .125 TAIL, RT ANG, PC MT
9	SOCKET, IC, 28 PIN
5	SOCKET, 84 PIN, PLCC, THRU HOLE
7	SOCKET, CLSD ENTRY,

WAVETEK
PARTS LIST
TITLE
90/95 MOTHERBOARD PREWAV

A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
AU221	PANAS	1500-32-2001	1
VB22RM6X7LL	UNCON	1500-32-2002	7
CV222SC	PANAS	1500-32-2201	2
300/50	NIC	1500-33-3202	2
72M25V18X36	NIC	1500-34-7202	2
2M16V22X41-0.5LS	NIC	1500-36-8201	2
03F	BISHO	1500-41-0304	1
J160D	MALRY	1500-41-0434	7
1.0K100	ITT	1500-41-0524	1
4J63F	MALRY	1500-44-7413	3
63-G	IMB	1500-45-6300	1

ASSEMBLY NO. 1200-00-3390
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MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IKO-02 7/35 PF	TRIKO	1500-53-5000	1
-00-3395	WVTK	1700-00-3395	1
386-0	AMP	2100-02-0079	1
94-1-04	CONCD	2100-02-0190	2
4-01-03	APTRN	2100-02-0196	1
585-2	AMP	2100-02-0256	1
2-2	AMP	2100-02-0257	4
2692-3	AMP	2100-02-0258	4
2R4-24BM32K9	BURND	2100-02-0259	1
28P-108T	BURND	2100-03-0081	1
73-1	AMP	2100-03-0094	1
8752-01-06-00	CAMB	2100-03-0096	2

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	.040 PINS				
P13 P22 P23	TERMINAL TAB (FASTON)	62747-1	AMP	2100-04-0038	3
TP11 TP16 TP2 TP6 TP8	TEST POINT, BLK, PC	TP-104-01-00	COMPD	2100-04-0054	5
TP1 TP10 TP14 TP15 TP17 TP5 TP7 TP9	TEST POINT, RED, PC	TP-104-01-02	COMPD	2100-04-0055	8
11	CONN PIN, INSERT	2100-05-0061	WVTK	2100-05-0061	2
Y1	CRYSTAL, 4MHZ	180-502	MTRON	2300-99-0004	1
6	FUSE HOLDER, CLIP	102071	LITFU	2400-05-0031	11
16	STANDOFF, SW, 6-32X5/32, 1/16 SW, BR, ZN PL	3045-B-632-B MODL=5/32	RAF	2800-06-0062	1
22	TRANSIPAD	10123N	METRS	2800-11-0003	1
21	TRANSIPAD	531-218	BIVAR	2800-11-0004	2
JMP6	JUMPER	461-2871-01-03-10	CAMBN	3000-00-0034	1
NONE	BATTERY HOLDER	BH 2/3A	MPD	3000-00-0137	1
FB1 FB2 FB3	BALUN CORE, FERRITE, 680 OHMS	2943666671	FARIT	3100-00-0017	3
BT1	BATTERY, 3V LITHIUM	BR-2/3A	PANAS	4000-02-0008	1
K1 K4 K5	RELAY, 2 FORMC, 5V, DIP 14	DF2E-DC5V	AROMT	4500-00-0033	3

WAVETEK
PARTS LIST
TITLE 90/95 MOTHERBOARD PREWAVE LOAD
ASSEMBLY NO. 1200-00-3390
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
K2 K3 K6	RELAY, 1 FORMC, 5V, .312H, .296W	HD1E-M-DC5V	AROMT	4500-00-0034	3
R104 R105 R94 R95	RES, C, 1/2W, 5%, 1.8	RC-1/2-1R8J	STKPL	4700-25-0189	4
R119 R129	RES, C, 1/2W, 5%, 3.9	RC-1/2-3R9J	STKPL	4700-25-0399	2
R118 R128	RES, C, 1/2W, 5%, 6.8	RC-1/2-6R8J	STKPL	4700-25-0689	2
R112 R114 R115	RES, MF, 1/8W, .1%, 1K	RN55E-1001B	MEPCO	4701-02-1001	3
R100	RES, MF, 1/8W, .1%, 10K	RN55E-1002B	MEPCO	4701-02-1002	1
R77 R78	RES, MFLM, 1/8W, .1%, 1.1K	5033RE1101B	MEPCO	4701-02-1101	2
R2	RES, MF, 1/8W, .1%, 1.5K	RN55E-1501B	CORNG	4701-02-1501	1
R99	RES, MF, 1/8W, .1%, 2K	RN55E-2001B	MEPCO	4701-02-2001	1
R90 R91	RES, MFLM, 1/8W, .1%, 232	5033RE2320B	MEPCO	4701-02-2320	2
R73	RES, MFLM, 1/8W, .1%, 2.55K	5033RE2551B	MEPCO	4701-02-2551	1
R1 R111 R3	RES, MF, 1/8W, .1%, 3K	RN55E-3001B	MEPCO	4701-02-3001	3
R86 R87	RES, MFLM, 1/8W, .1%, 6.73K	5033RE6731B	MEPCO	4701-02-6731	2
R88 R89	RES, MFLM, 1/8W, .1%, 68.1	CMF-5568R1BT-9	DALE	4701-02-6819	2

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PARTS LIST
TITLE 90/95 MOTHERBOARD PREWAVE LOAD
ASSEMBLY NO. 1200-00-3390
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REMOVE ALL BURRS
AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ ENGR
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
± XX ± ±
XXX ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
MOTHERBOARD PREWAVE

SIZE	FSCM NO	DWG NO	REV
D	23338	1200-00-3390	E

SCALE
MODEL 95
SHEET 1 OF 2

115685

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R4	RES,MF,1/8W,.1%,750	RN55E-7500B	MEPCO	4701-02-7500	1
R101 R103 R122 R124 R125 R132	RES,MF,1/8W,.1%,7.5K	RN55E-7501B	MEPCO	4701-02-7501	6
R81 R82	RES,MFLM,1/8W,.1%,75	5033RE7509B	MEPCO	4701-02-7509	2
R149 R16 R17 R48 R58	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	5
R21 R24 R28 R30 R38 R60 R63 R64	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	8
R10 R11 R133 R23 R36 R5 R57 R68 R8 R9	RES,MF,1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	10
R7 R79 R92 R93	RES,MF,1/8W,1%,100K	RN55D-1003F	TRW	4701-03-1003	4
R44 R59 R62	RES,MF,1/8W,1%,1M	RN55D-1004F	TRW	4701-03-1004	3
R143 R144 R145 R146 R147 R148	RES,MF,1/8W,1%,10	5043ED10R100F	MEPCO	4701-03-1009	6
R74	RES,MFLM,1/8W,1%,127K	5033RD1273F	MEPCO	4701-03-1273	1
R41	RES,MF,1/8W,1%,1.5K	RN55D-1501F	TRW	4701-03-1501	1
R138 R33 R34 R65	RES,MF,1/8W,1%,15	RN55D-15R0F	TRW	4701-03-1509	4
R110	RES,MF,1/8W,1%,165	RN55D-1650F	TRW	4701-03-1650	1
R26	RES,MF,1/8W,1%,1.78K	RN55D-1781F	TRW	4701-03-1781	1

WAVETEK
PARTS LIST
TITLE
90/95 MOTHERBOARD PREWAVE LOAD
ASSEMBLY NO. 1200-00-3390
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R113	RES,MF,1/8W,1%,182	RN55D-1820F	TRW	4701-03-1820	1
R45 R46 R54	RES,MF,1/8W,1%,200	RN55D-2000F	TRW	4701-03-2000	3
R42 R43	RES,MF,1/8W,1%,2K	RN55D-2001F	TRW	4701-03-2001	2
R6	RES,MF,1/8W,1%,200K	RN55D-2003F	MEPCO	4701-03-2003	1
R22	RES,MF,1/8W,1%,21.5K	RN55D-2152F	TRW	4701-03-2152	1
R15 R67	RES,MF,1/8W,1%,2.21K	RN55D-2211F	TRW	4701-03-2211	2
R13	RES,MF,1/8W,1%,274	RN55D-2740F	TRW	4701-03-2740	1
R69 R70	RES,MF,1/8W,1%,28.7K	RN55D-2872F	TRW	4701-03-2872	2
R18 R35 R37	RES,MF,1/8W,1%,3.32K	RN55D-3321F	TRW	4701-03-3321	3
R29	RES,MF,1/8W,1%,3.65K	RN55D-3651F	TRW	4701-03-3651	1
R102	RES,MF,1/8W,1%,3.74K	RN55D-3741F	TRW	4701-03-3741	1
R107 R98	RES,MF,1/8W,1%,392	RN55D-3920F	TRW	4701-03-3920	2
R106 R108 R117 R121 R126 R127 R47 R96 R97	RES,MF,1/8W,1%,3.92K	RN55D-3921F	TRW	4701-03-3921	9
R109	RES,MF,1/8W,1%,40.2	RN55D-40R2F	TRW	4701-03-4029	1
R116 R120 R130 R151 R27	RES,MF,1/8,1%,499	RN55D-4990F	TRW	4701-03-4990	5
R131 R31 R32 R40	RES,MF,1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	4

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PARTS LIST
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90/95 MOTHERBOARD PREWAVE LOAD
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REFERENCE DESIGNATORS	PART DESCRIPTION
R12 R14	RES,MF,1/8W,1%,49.9K
R61 R84 R85	RES,MF,1/8W,1%,576
R152	RES,MF,1/8W,1%,61.9
R49	RES,MF,1/8W,1%,681
R80 R83	RES,MFLM,1/8W,1%,75
R56	RES,MF,1/8W,1%,78.7
R25	RES,MF,1/8W,1%,8.87K
R19 R20 R39	RES,MF,1/8W,1%,9.09K
R75 R76	RES,MFLM,1/4W,.1%,49.9
R66 R71 R72	RES,MFLM,1W,.1%,51.1
JMP4 JMP5	RES, 0 OHM JUMPER
CR13	DIODE, ZENOR, 5.1V, 500MW, GIB, IN751A
CR1 CR10 CR11 CR12 CR14 CR15 CR16 CR17 CR18 CR19 CR2 CR20 CR41 CR7 CR8 CR9	DIODE, HIGH CONDUCTANCE, ULTRA FAST
CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR34 CR35 CR36 CR37 CR38	DIODE,1N4002 GEN PURPOSE RECT. 100V,1A

WAVETEK
PARTS LIST
TITLE
90/95 MOTHERBOARD PREWAVE L

REFERENCE DESIGNATORS	PART DESCRIPTION
CR30 CR31 CR32 CR33	DIODE 1N4005 GENERAL PURPOSE,RECTIFIER,600 V,1A
CR5	DIODE, RECT, SCH BARRIER
CR3 CR4	DIODE 5082-2811 SCHOTTKY,15V,20MA
CR40	BRIDGE ASSY,4 AMP
CR6	LED,GREEN,RECT BAR
Q3	TRANS 2N2219A NPN GENERAL PURPOSE TO-5
Q2 Q6 Q7	TRANS 2N2905A PNP GENERAL PURPOSE TO-5
Q1 Q4 Q8 Q9	TRANS 2N3904 NPN GENERAL PURPOSE TO-92
Q5	TRANS, GENERAL PURPOSE, PNP, TO-92
Q11 Q12	TRANS
SW1	SWITCH,MIN PUSHBUTTON,SPST BLK
U18	DAC,SERIAL INP,16

WAVETEK
PARTS LIST
TITLE
90/95 MOTHERBOARD PREWAVE

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

FGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
4992F	TRW	4701-03-4992	2
5760F	TRW	4701-03-5760	3
61R9F	TRW	4701-03-6199	1
6810F	TRW	4701-03-6810	1
75R0F	MEPCO	4701-03-7509	2
78R7F	TRW	4701-03-7879	1
8871F	TRW	4701-03-8871	1
9091F	TRW	4701-03-9091	3
49R9B	MEPCO	4701-12-4999	2
51R1B	MEPCO	4701-32-5119	3
8G	ROHM	4799-00-0087	2
	FAIR	4801-01-0751	1
	FAIR	4801-01-5282	16
	FAIR	4801-02-0001	14

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FGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	MOT	4806-01-4005	4
0	MOT	4806-02-0120	1
811	HP	4809-02-2811	2
	DIODE	4899-00-0037	1
31A	LITE	4899-00-0057	1
A	NSC	4901-02-2191	1
A	NSC	4901-02-9051	3
	FAIR	4901-03-9040	4
	NSC	4901-04-1220	1
	INTSL	4902-00-0100	2
	GRAHL	5102-00-0015	1
	BURR	7000-00-5600	1

ASSEMBLY NO. 1200-00-3390
REV E
PAGE 10

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	BIT, MONO				
U1 U3	MUX, CMOS, D 4C, 8 CHAN/DUAL 4 CHAN ANAL	DG508ACJ	SLCON	7000-05-0800	2
U26	COMPARATOR, ULTRA FAST, 10NS	LT1016CN8	LINTE	7000-10-1600	1
U32	VOLTAGE REFERENCE, 10V, 8 PIN DIP	LT1021CCN8-10	LINTE	7000-10-2101	1
U4	ADC, 12 BIT	ICL7109CPL	INTSL	7000-71-0900	1
U5	RESET GEN	TL7705ACP	TI	7000-77-0501	1
U2 U33 U34	OP AMP, HI SLEW RTE, WIDEBND, JFET, STD	MC34081P	MOT	7003-40-8100	3
U14 U20 U21 U22 U23 U24 U29 U31	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	8
U28	DRIVER, DUAL LINE	SN75121N	TI	7007-51-2100	1
U19	MUX/DEMUX, ANALOG	CD4051BE	RCA	8000-40-5100	1
U11	SRAM, 8KX8, 120NS, CMOS	CXK5864BP-12L	SONY	8000-62-6400	1
U6	MICROPROCESSOR, 8BIT	MC6803L	MOT	8000-68-0300	1
U16	FLIP-FLOP, DUAL D, POS EDGE TRIG W/CLR/PRES	SN74ALS74N	TI	8000-74-7403	1
VR2	VOLT REGULATOR	LM78M05CH	NSC	8000-78-0501	1

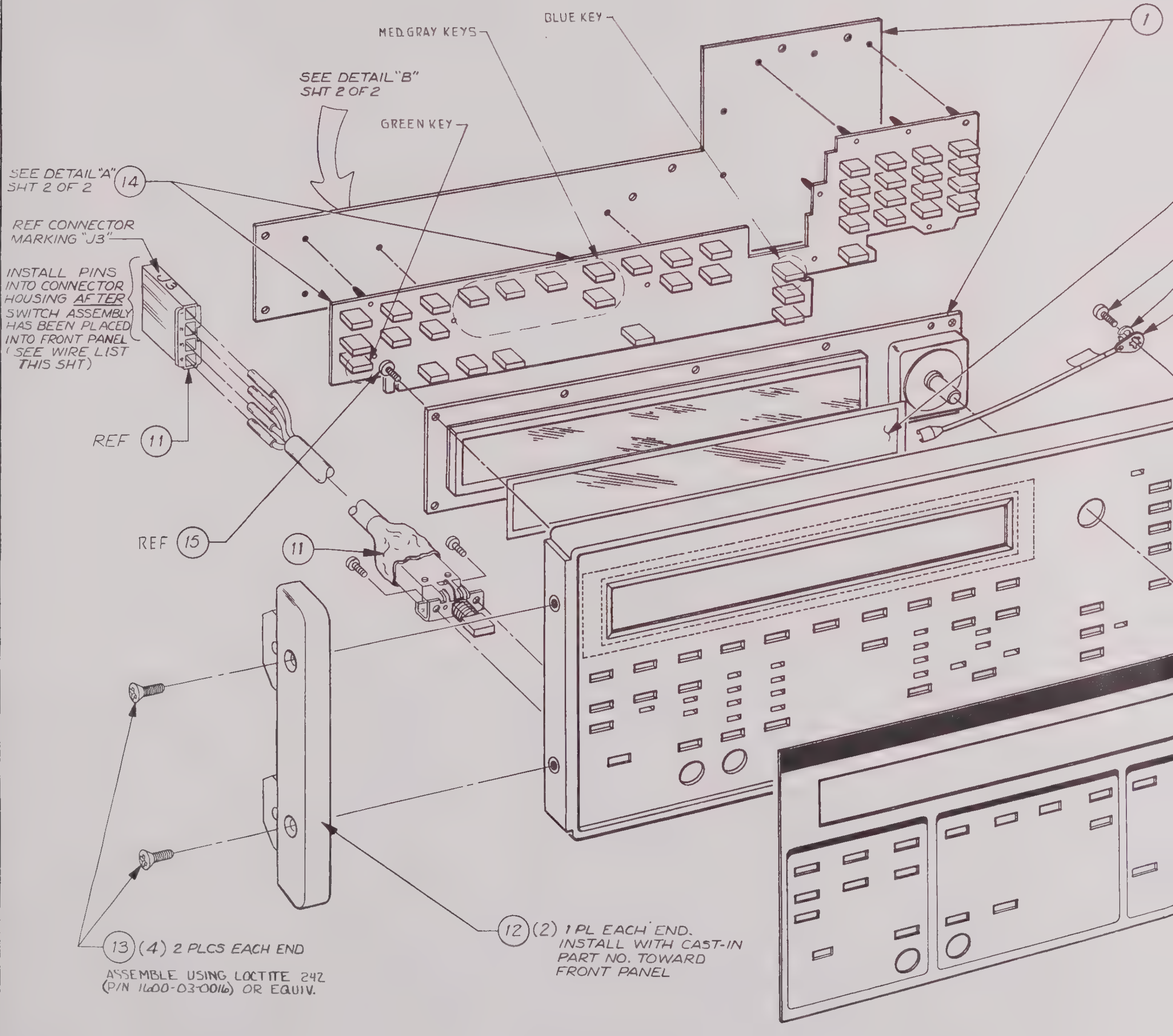
WAVETEK
PARTS LIST
TITLE 90/95 MOTHERBOARD PREWAVE LOAD
ASSEMBLY NO. 1200-00-3390
REV E
PAGE 11

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U8	ADPT, GPIB INTERFACE	MC68488P	MOT	8006-84-8800	1
U27	MUX/SEL, DUAL 1 OF 4 DATA, 3/STATE	SN74ALS253N	TI	8007-42-5300	1
U30	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	1
U15	VCO, TTL	74LS624	TI	8007-46-2410	1
U9	XCVR, OSC BUS, TTL	75160	TI	8007-51-6000	1
U10	TRANSCEIVER, OCT BUS, TTL	SN75161BN	TI	8007-51-6100	1
U13	PLL	MC145157P2	MOT	8014-51-5700	1
U35	PAL, ROM DECODE, USES 1 ea., 8000-16-8000 FOR MOD 90, V1.0, REF U35	8600-00-0596	WVTK	8600-00-0596	1
U7	GATE ARRAY, 84 PIN, PSC288	PSC288	PLESS	8700-00-0003	1
U17		CLA53047BA	PLESS	8700-00-0005	1

WAVETEK
PARTS LIST
TITLE 90/95 MOTHERBOARD PREWAVE LOAD
ASSEMBLY NO. 1200-00-3390
REV E
PAGE 12

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
MOTHERBOARD PREWAVE
SIZE D
FSCM NO 23338
DWG. NO. 1200-00-3390
REV E
SCALE
MODEL 95
SHEET 2 OF 2


D
C
B
A
BLUE KEY
MED. GRAY KEYS
SEE DETAIL "B" SHT 2 OF 2
GREEN KEY
1
SEE DETAIL "A" SHT 2 OF 2
14
REF CONNECTOR MARKING "J3"
J3
INSTALL PINS INTO CONNECTOR HOUSING AFTER SWITCH ASSEMBLY HAS BEEN PLACED INTO FRONT PANEL (SEE WIRE LIST THIS SHT)
REF 11
REF 15
11
13 (4) 2 PLCS EACH END
ASSEMBLE USING LOCTITE 242 (P/N 1600-03-0016) OR EQUIV.
12 (2) 1 PL EACH END. INSTALL WITH CAST-IN PART NO. TOWARD FRONT PANEL

1 MARK ASSEMBLY NO. "1101-00-3344", LATEST REV, MANUFACTURER'S ID, FSCM 23338, PER MIL-STD-130, APPROX WHERE SHOWN.

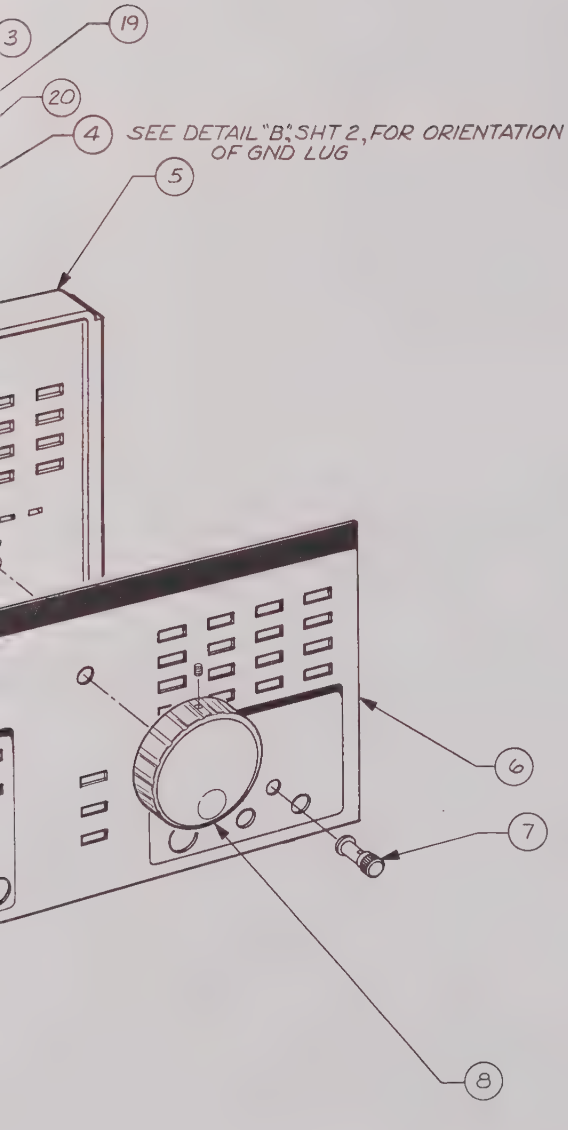
NOTE UNLESS OTHERWISE SPECIFIED

4 3 2 1

REV	ECO	BY	DATE	APP
A	ERO NO. 90-381	AP	[illegible]	[illegible]
B	ECO # 90-536	MS	9-13-90	ΠM

D

C



SEE DETAIL "B", SHT 2, FOR ORIENTATION OF GND LUG

B

1101-00-3344

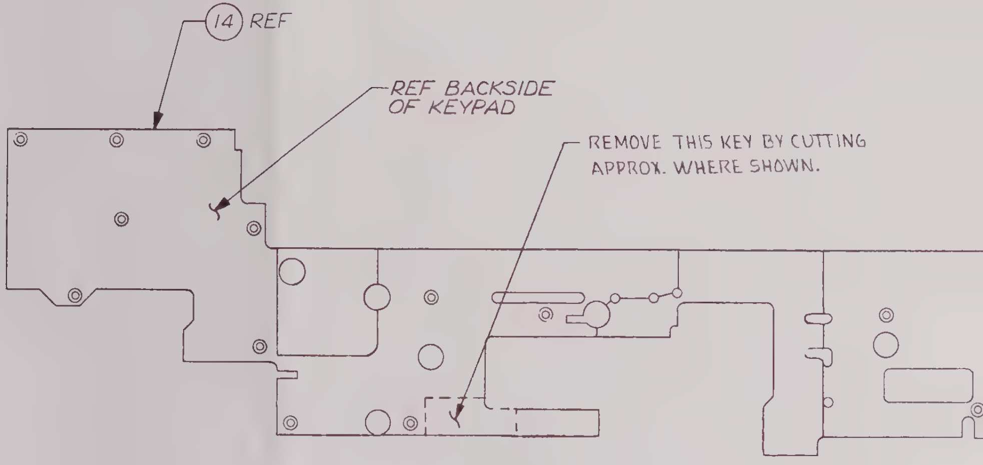
WIRE LIST

"J3" CONN PIN NO.	WIRE COLOR	SWITCH TERMINAL (REF)
3	RED	2A
2	WHT	1A
4	GRN	5B
1	BLK	4B

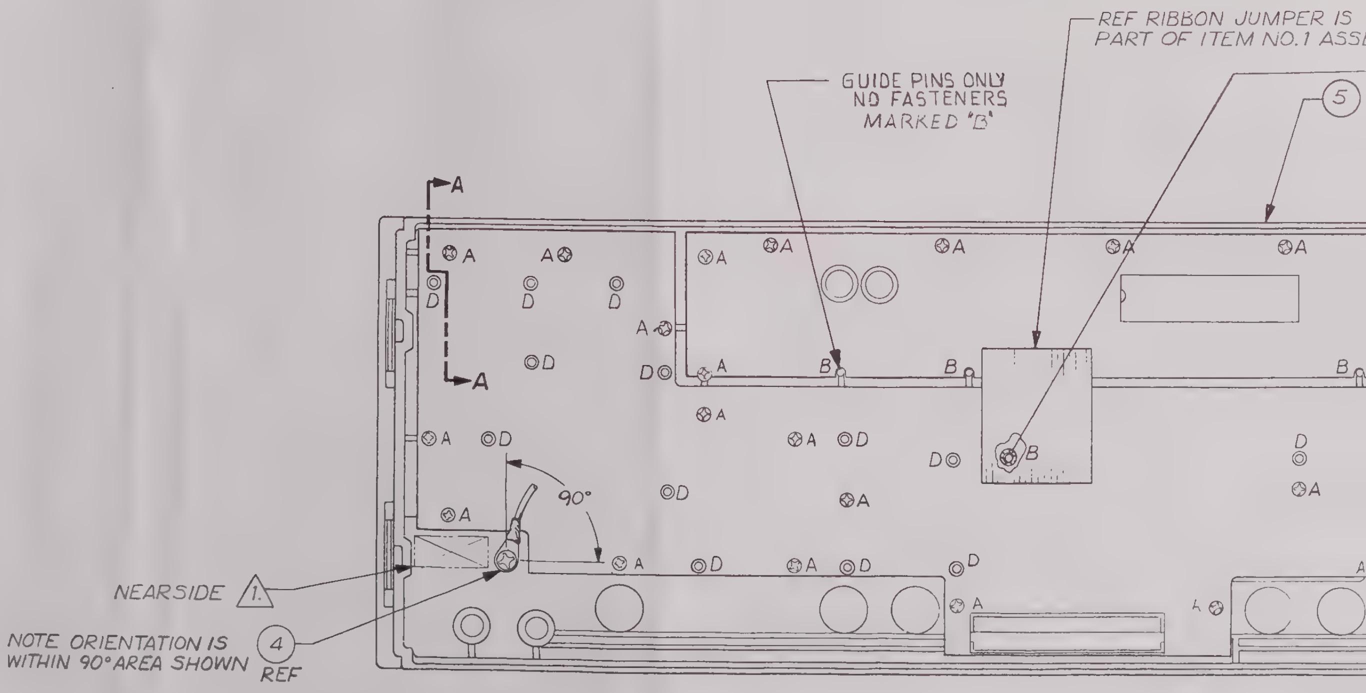
SEE SEPARATE PARTS LIST

A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN SC/AP	DATE 5-18-90	**WAVETEK** SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED D. Buzzell	4/5/90	TITLE ASSEMBLY, FRONT PANEL
	PROJ. ENGR.	6/5/90	
FINISH WAVETEK PROCESS	RELEASE APPROV	-/6/90	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± / DECIMALS .XX ± .XXX ± / ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1101-00-3344 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 95 · SHEET 1 OF 2


14 REF
REF BACKSIDE OF KEYPAD
REMOVE THIS KEY BY CUTTING APPROX. WHERE SHOWN.

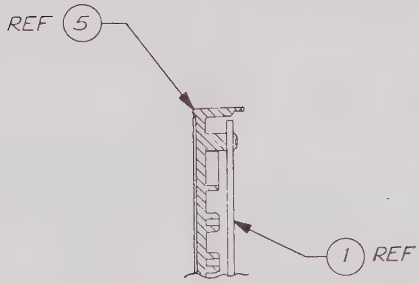
DETAIL "A"
(KEYPAD PREP. NOTE: KEYS OF KEYPAD ARE NOT SHOWN)


REF RIBBON JUMPER IS
PART OF ITEM NO.1 ASS
GUIDE PINS ONLY NO FASTENERS MARKED "B"
5
A
A
A
A
A
A
A
A
D
D
D
D
D
B
B
B
B
90°
NEARSIDE 1.
NOTE ORIENTATION IS WITHIN 90° AREA SHOWN
4 REF

DETAIL "B"
(PC BOARD TO FRONT PANEL INSTALLATION)

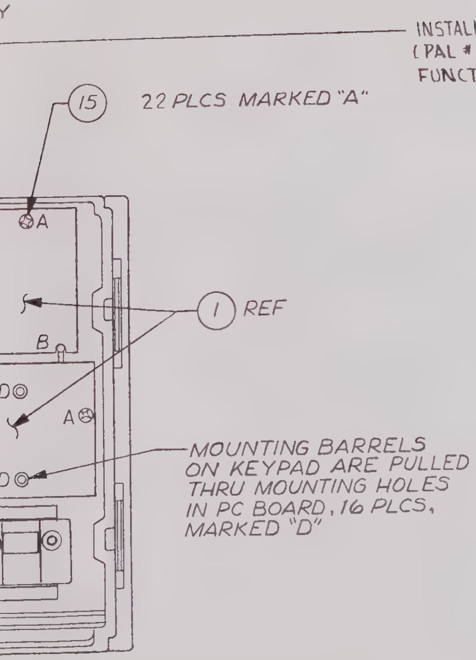
NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP



SECTION VIEW A-A

INSTALL PRESS ON FASTNER WVTK P/N 2800-09-0034 (PAL # PS 094032) AFTER FRONT PANEL HAS BEEN FUNCTIONALLY TESTED . 1 PLC.



22 PLCS MARKED "A"

MOUNTING BARRELS ON KEYPAD ARE PULLED THRU MOUNTING HOLES IN PC BOARD, 16 PLCS, MARKED "D"

1101-00-3344 B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN SC	DATE 5-17-90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENG	6/5/90	TITLE ASSEMBLY, FRONT PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX — .XX — ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO. 95 · DWG NO. 1101-00-3344 · REV B
	SCALE NONE		CODE IDENT 23338 · SHEET 2 OF 2

115685

D

C

B

A

NOTE UNLESS OTHERWISE SPECIFIED

4 3 2 1

REV	ECO	BY	DATE	APP

D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, DISPLAY/ KEYBOARD	1100-00-3322	WVTK	1100-00-3322	1
NONE	A/D, ASSY, FRONT PANEL	1101-00-3344	WVTK	1101-00-3344	1
8	ENCODER KNOB ASSY REF: A/D 1201-00-3380	1200-00-3380	WVTK	1200-00-3380	1
11	CABLE ASSY, AC SWITCH AND CABLE	1200-00-3391	WVTK	1200-00-3391	1
4	WIRE ASSY	1207-00-3010	WVTK	1207-00-3010	1
14	KEY PAD, MODEL 95	1400-02-3420-02	CRT	1400-02-3420	1
12	CORNER BRACKET, PAINTED	1400-02-5034	WVTK	1400-02-5034	2
6	OVERLAY FRONT PANEL MODEL 95	1400-02-5072	WVTK	1400-02-5072	1
3	WINDOW, DISPLAY	1400-02-5073	WVTK	1400-02-5073	1
5	FRONT PANEL MOLDED	1400-02-5087	WVTK	1400-02-5087	1
7	LUG, GROUNDING	159	SMITH	2100-04-0043	1
20	WASHER, LOCK, REQ S/S #6	MS 35338-136	CMRCL	2800-45-6000	1
13	SCREW, 8-32 X 1/2, 100 DEG, FH, PHLPS, SS	2800-54-8108	CMCRL	2800-54-8108	4

WAVETEK PARTS LIST

TITLE ASSY, FRONT PANEL

ASSEMBLY NO. 1100-00-3344

REV E

PAGE 1

C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
15	SCREW, 2 X 5/16, TYPE B, THD FORM, PH, SS	2800-57-2905	CMRCL	2800-57-2905	23
19	SCREW, PH, 6-32 X 5/16, PHLPS, NYLOK, SS	2800-59-6105	CMRCL	2800-59-6105	1

WAVETEK PARTS LIST

TITLE ASSY, FRONT PANEL

ASSEMBLY NO. 1100-00-3344

REV E

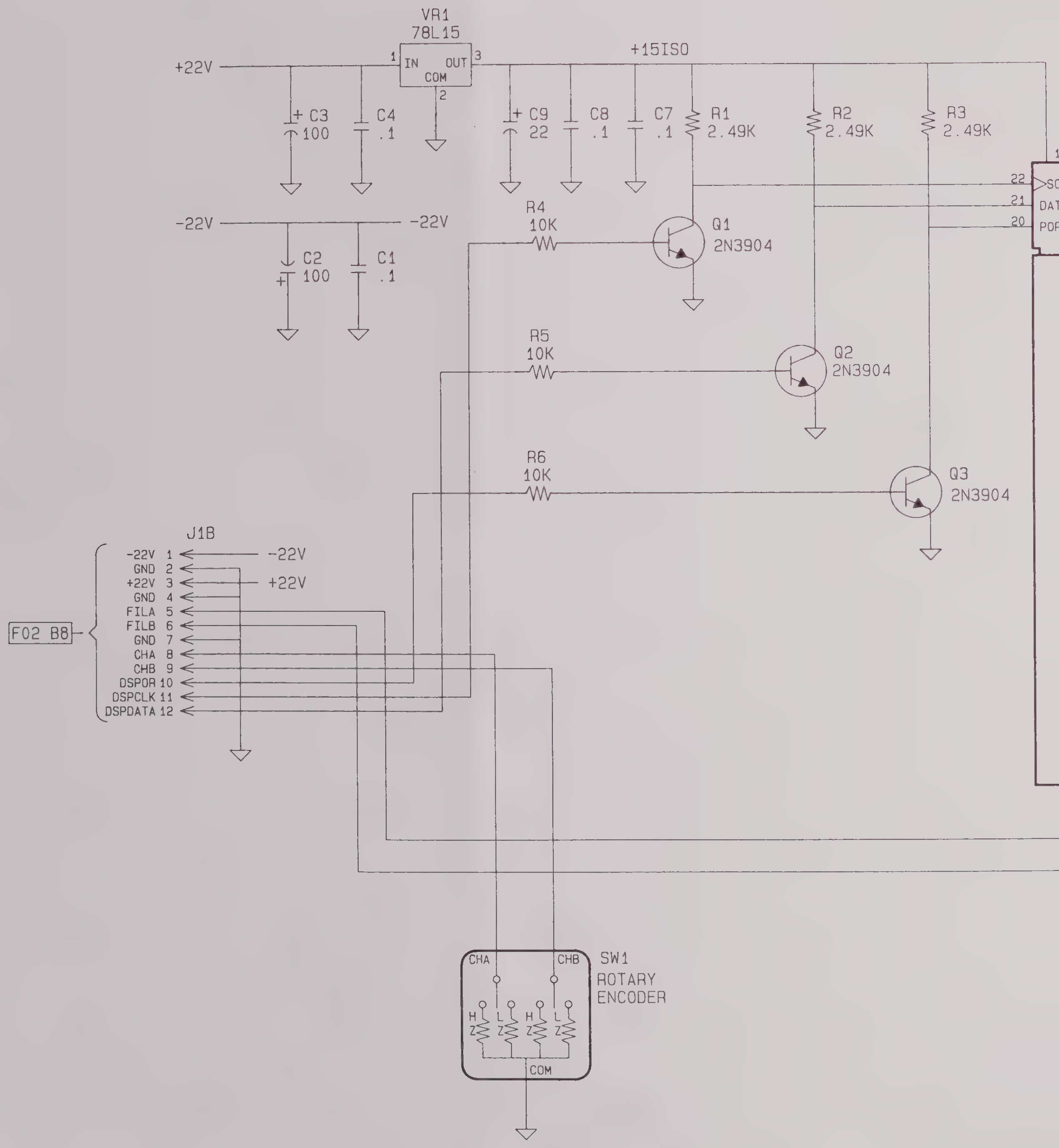
PAGE 2

B

A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	CHECKED		TITLE PARTS LIST FRONT PANEL	
	PROJ. ENGR.			
	RELEASE APPROV.			
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D	FSCM NO. 23338 · DWG. NO. 1100-00-3344 · REV E
DO NOT SCALE DRAWING			SCALE	MODEL 95 · SHEET 1 OF 1

4 3 2 1


VR1
78L15
+22V
1
IN
OUT
COM
3
2
+15ISO
C3
100
C4
.1
C9
22
C8
.1
C7
.1
R1
2.49K
R2
2.49K
R3
2.49K
22
21
20
SC
DAT
POF
-22V
-22V
C2
100
C1
.1
R4
10K
Q1
2N3904
R5
10K
Q2
2N3904
R6
10K
Q3
2N3904
J1B
-22V 1
GND 2
+22V 3
GND 4
FILA 5
FILB 6
GND 7
CHA 8
CHB 9
DSPOR 10
DSPCLK 11
DSPDATA 12
-22V
+22V
F02 B8
CHA
CHB
SW1
ROTARY
ENCODER
H
L
H
L
COM

△4 THESE PARTS ARE NOT INSTALLED.

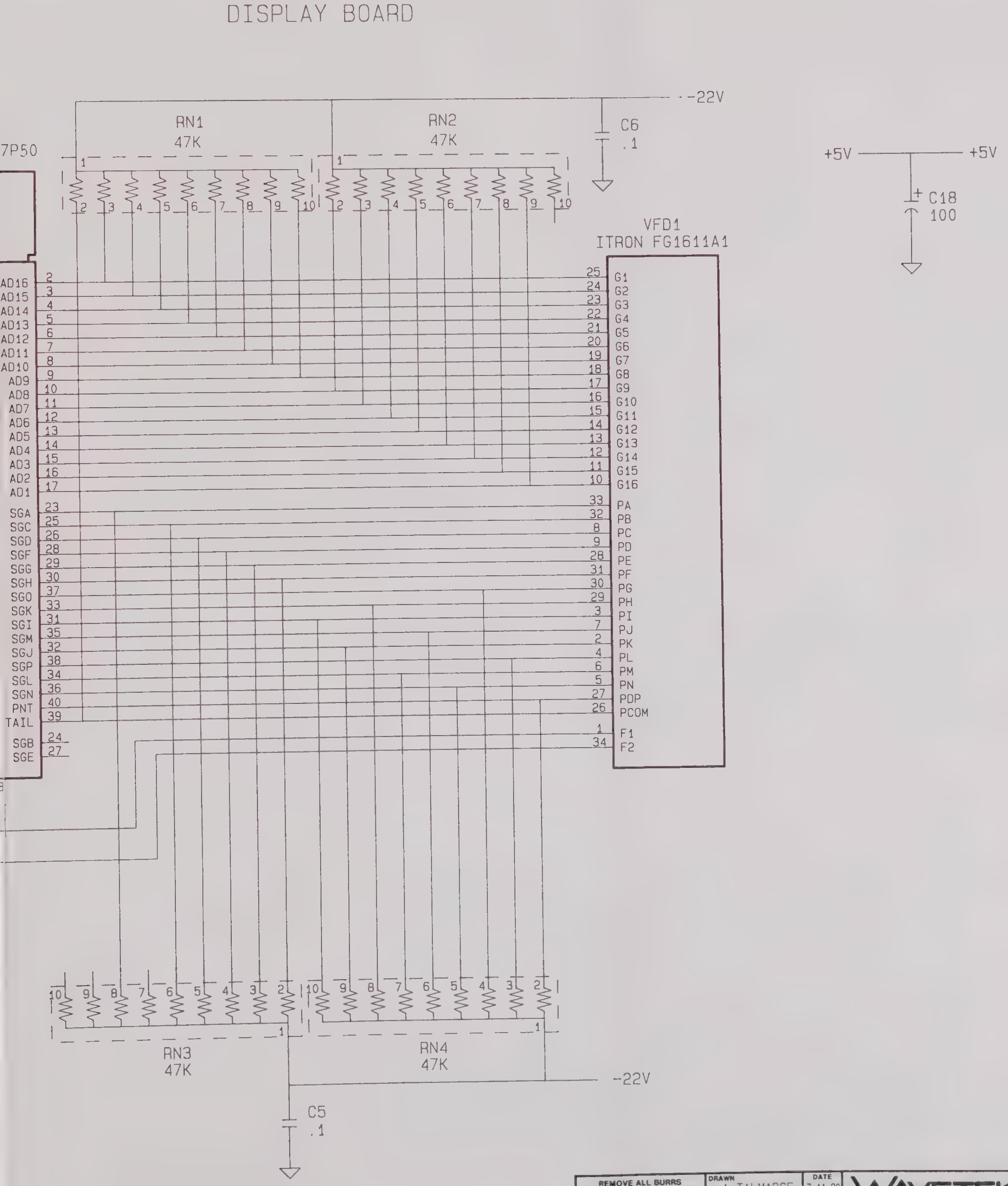
3. FOR INSTRUMENT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

2. ALL CAPACITORS ARE IN MICROFARADS (uF).

1. ALL RESISTORS ARE IN OHMS, 1/8W, 1%, MF.

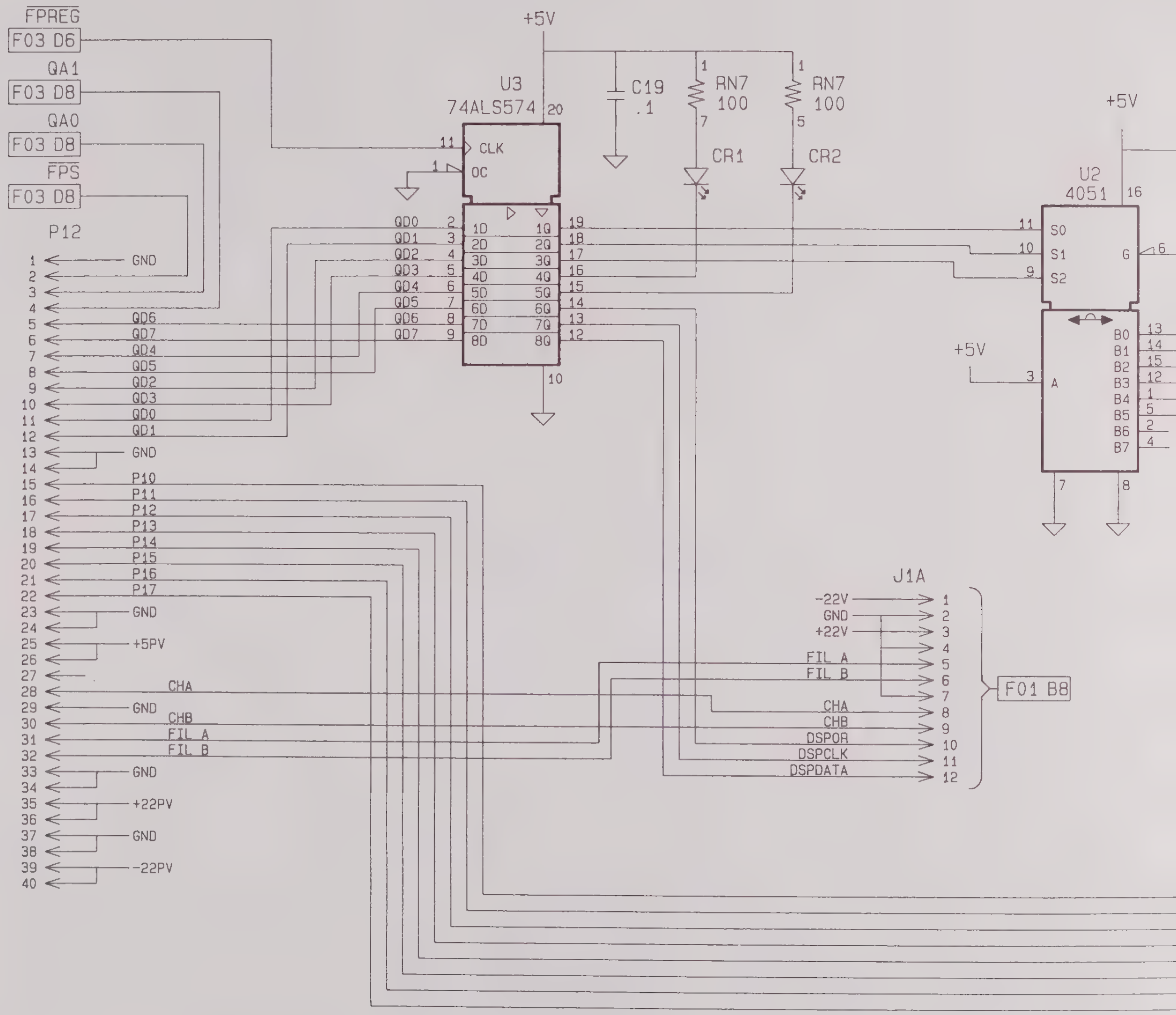
NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
B	ECO 93-067	SC	12-2-92	ՈՊ


DISPLAY BOARD
-22V
RN1
47K
RN2
47K
C6
.1
7P50
+5V
+5V
C18
100
VFD1
ITRON FG1611A1
AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1
SGA SGC SGD SGF SGG SGH SGO SGK SGI SGM SGJ SGP SGL SGN PNT TAIL SGB SGE
G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 G16
PA PB PC PD PE PF PG PH PI PJ PK PL PM PN PDP PCOM F1 F2
RN3
47K
RN4
47K
-22V
C5
.1

1104-00-3341 B

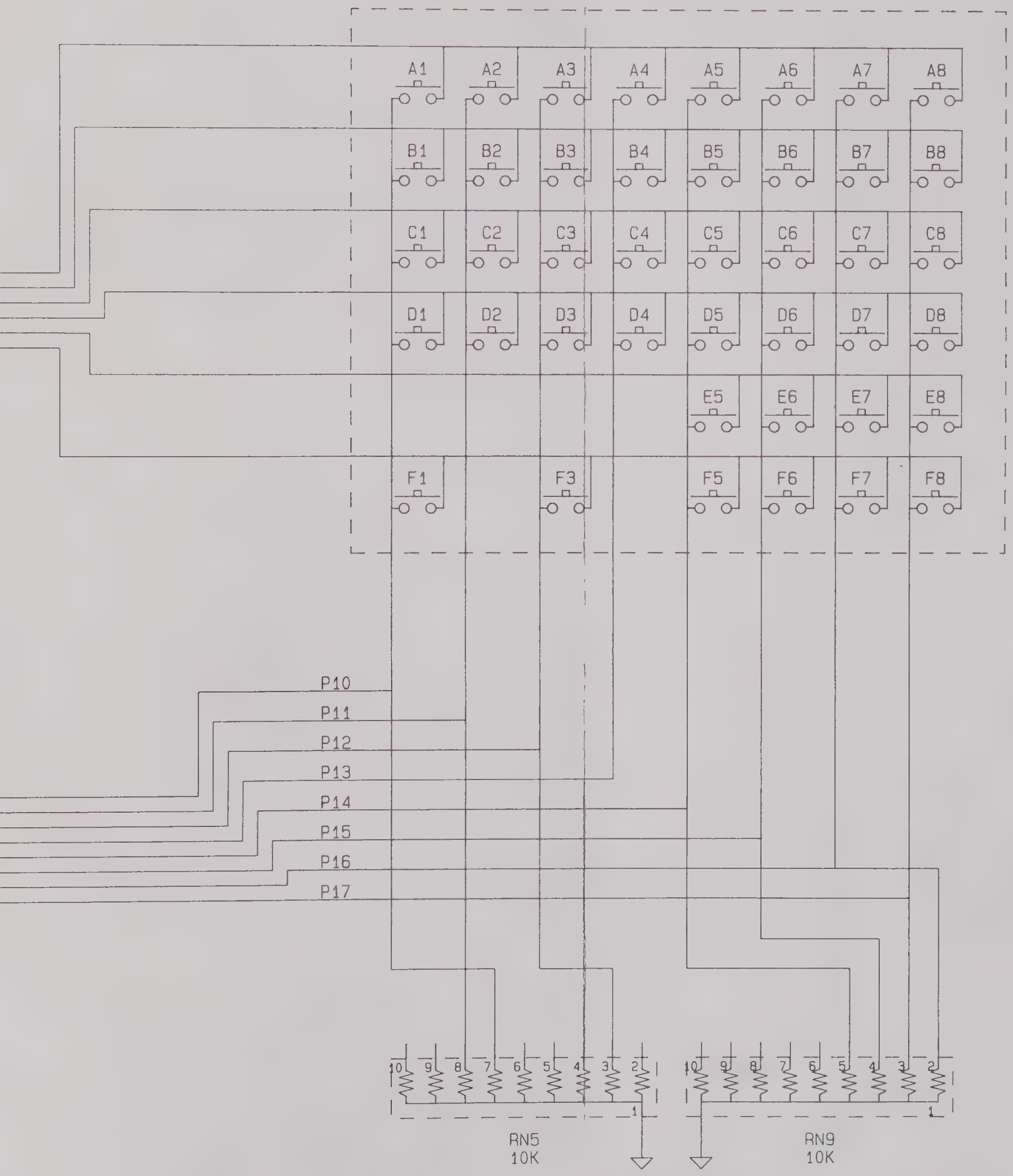
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 7-11-90	**WAVETEK** SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED Gary Good	7-26-90	TITLE SCHEMATIC, DISPLAY/KEYBOARD
	PROJ. ENGR	7/24/90	
FINISH WAVETEK PROCESS	RELEASE APPROV.	7/26/90	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO 23338 · DWG NO. 1104-00-3322 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES · SHEET 1 OF 4


FPREG
F03 D6
QA1
F03 D8
QA0
F03 D8
FPS
F03 D8
P12
1 GND
2
3
4
5 QD6
6 QD7
7 QD4
8 QD5
9 QD2
10 QD3
11 QD0
12 QD1
13 GND
14
15 P10
16 P11
17 P12
18 P13
19 P14
20 P15
21 P16
22 P17
23 GND
24
25 +5PV
26
27
28 CHA
29 GND
30 CHB
31 FIL A
32 FIL B
33 GND
34
35 +22PV
36
37 GND
38
39 -22PV
40
+5V
U3
74ALS574
20
11 CLK
1 OC
QD0 2 1D 1Q 19
QD1 3 2D 2Q 18
QD2 4 3D 3Q 17
QD3 5 4D 4Q 16
QD4 6 5D 5Q 15
QD5 7 6D 6Q 14
QD6 8 7D 7Q 13
QD7 9 8D 8Q 12
10
C19
.1
RN7
100
1
7
RN7
100
1
5
CR1
CR2
+5V
U2
4051
16
11 S0
10 S1
9 S2
G 6
+5V
3 A
B0 13
B1 14
B2 15
B3 12
B4 1
B5 5
B6 2
B7 4
7
8
J1A
-22V 1
GND 2
+22V 3
4
FIL A 5
FIL B 6
7
CHA 8
CHB 9
DSPOR 10
DSPCLK 11
DSPDATA 12
F01 B8

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

* SEE SHEET 4 FOR KEY ASSIGNMENTS


A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
C1
C2
C3
C4
C5
C6
C7
C8
D1
D2
D3
D4
D5
D6
D7
D8
E5
E6
E7
E8
F1
F3
F5
F6
F7
F8
P10
P11
P12
P13
P14
P15
P16
P17
10
9
8
7
6
5
4
3
2
1
RN5
10K
10
9
8
7
6
5
4
3
2
1
RN9
10K

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

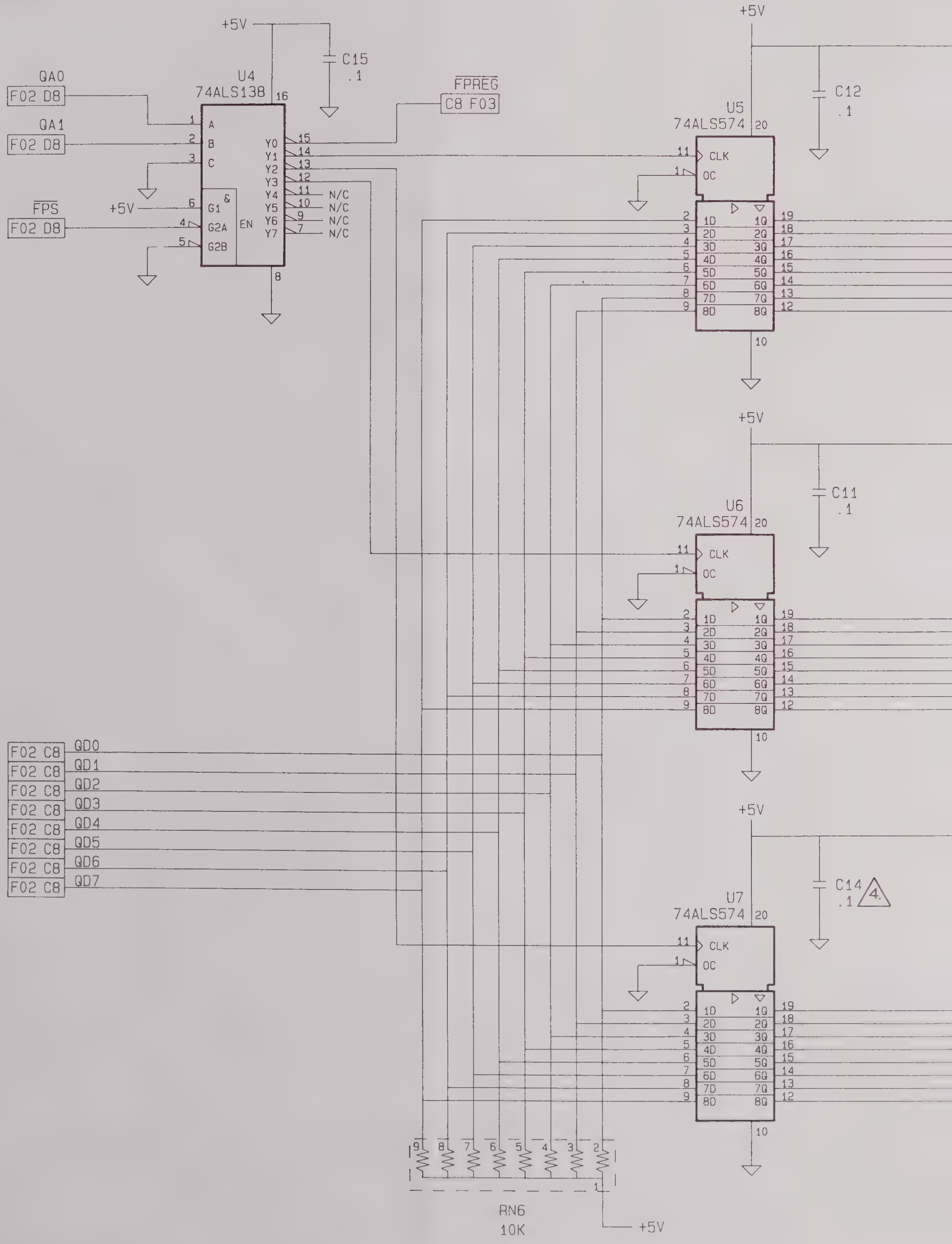
DRAWN A. TALMADGE — DATE 7-11-90
CHECKED — 7-26-90
PROJ ENGR — 7/26/90
RELEASE APPROV — 7/26/90

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

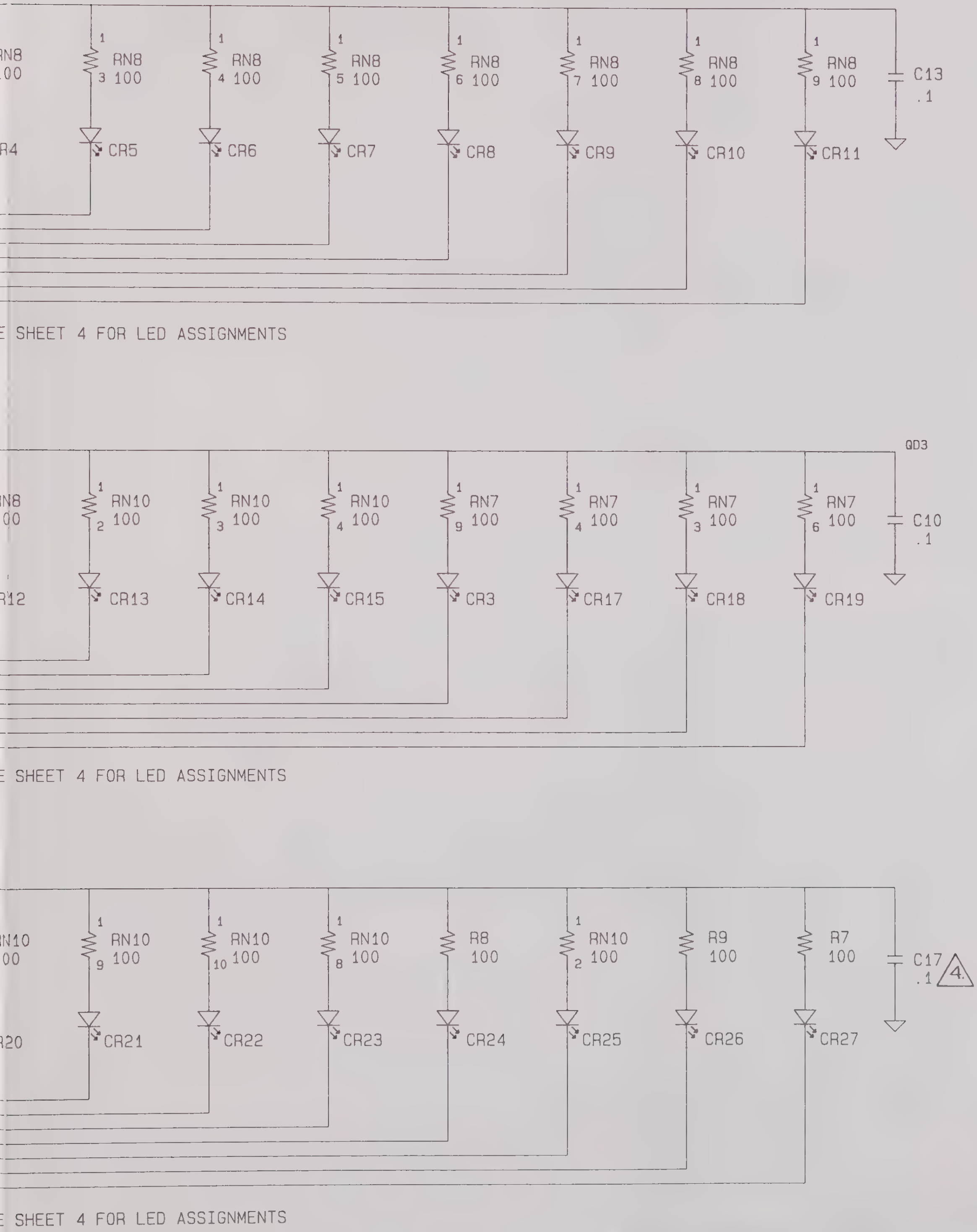
TITLE
SCHEMATIC,
DISPLAY/KEYBOARD

SIZE D
FSCM NO 23338
DWG. NO. 1104-00-3322
REV B
SCALE NONE
MODEL 90 SERIES
SHEET 2 OF 4


8
7
6
5
D
C
B
A
+5V
C15
.1
QA0
F02 D8
QA1
F02 D8
FPS
F02 D8
U4
74ALS138
16
A
B
C
G1
G2A
G2B
EN
&
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
N/C
N/C
N/C
N/C
FPREG
C8 F03
U5
74ALS574
20
CLK
OC
1D
2D
3D
4D
5D
6D
7D
8D
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
10
C12
.1
U6
74ALS574
C11
.1
U7
74ALS574
C14
.1
4
F02 C8
QD0
QD1
QD2
QD3
QD4
QD5
QD6
QD7
RN6
10K

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


RN8
100
RN8 3 100
CR4
CR5
RN8 4 100
CR6
RN8 5 100
CR7
RN8 6 100
CR8
RN8 7 100
CR9
RN8 8 100
CR10
RN8 9 100
CR11
C13
.1
SHEET 4 FOR LED ASSIGNMENTS
QD3
RN8
100
CR12
RN10 2 100
CR13
RN10 3 100
CR14
RN10 4 100
CR15
RN7 9 100
CR3
RN7 4 100
CR17
RN7 3 100
CR18
RN7 6 100
CR19
C10
.1
SHEET 4 FOR LED ASSIGNMENTS
RN10
100
CR20
RN10 9 100
CR21
RN10 10 100
CR22
RN10 8 100
CR23
R8
100
CR24
RN10 2 100
CR25
R9
100
CR26
R7
100
CR27
C17
.1
4
SHEET 4 FOR LED ASSIGNMENTS

REMOVE ALL BURRS
AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN	A. TALMADGE	DATE 7-11-90
CHECKED	D. Hood	7-26-90
PROJ. ENGR		7/26/90
RELEASE APPROV.	John B.	7/26/90

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
DISPLAY/KEYBOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3322	B

SCALE NONE | MODEL 90 SERIES | SHEET 3 OF 4

LED ASSIGNMENTS

	90	95
CR1	UNLOCK	UNLOCK
CR2	EXT	EXT
CR3		DL
CR4	600	600
CR5	135	135
CR6	75	75
CR7	BAL	BAL
CR8	50	50
CR9	ENABLE	ENABLE
CR10	REMOTE	REMOTE
CR11	HV OPT	
CR12	AM	AM
CR13	FM	FM
CR14	SWEEP	SWEEP
CR15	SCM	SCM
CR17		∿
CR18		⎍
CR19		⋀
CR20	TRIG	TRIG
CR21	GATE	GATE
CR22	CONT	CONT
CR23	BURST	BURST
CR24	DC	ARB4
CR25	⎍	ARB3
CR26	⋀	ARB2
CR27	∿	ARB1

KEY

	1	2
A	AMPL	FREQ
B	OFFSET	DISPLAY
C	STORE	RESET
D	→	
E		
F	MAN TRIG	

KEY

	1	2
A	AMPL	FREQ
B	OFFSET	Z-AXIS
C	STORE	RESET
D	EDIT	SOURCE
E		
F	MAN TRIG	

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

D

GNMENTS - MODEL 90

	4	5	6	7	8
	SYMM	1	0	7	4
	SOURCE	2	.	8	5
E	FUNCTION	3	+/-	9	6
—	BURST CNT	EXP	ENTER	KNOB	CE
		CMD RECALL	ON/OFF	LOCAL	SHIFT
P E			MODE	TRIG FREQ	TIME

C

GNMENTS - MODEL 95

	4	5	6	7	8
C R	FILTER	1	0	7	4
RS	PHASE	2	.	8	5
SS	FUNCTION	3	+/-	9	6
-	BURST CNT	EXP	ENTER	KNOB	CE
		CMD RECALL	ON/OFF	LOCAL	SHIFT
P			MODE	TRIG FREQ	TIME

B

B

1104-00-3322

CAD JOB #: B068A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 7-11-90
MATERIAL	CHECKED Gary Good	7-16-90
	PROJ ENGR	7/16/90
FINISH WAVETEK PROCESS	RELEASE APPROV	7/16/90
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

SCHEMATIC,
DISPLAY/KEYBOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3322	B

SCALE NONE | MODEL 90 SERIES | SHEET 4 OF 4

A

D

NOTES:

1. COMPONENTS MOUNTED ON COMPONENT SIDE OF PCB SHOWN ON SHEET 1, COMPONENTS MOUNTED ON SOLDER SIDE OF PCB SHOWN ON SHEET 2.

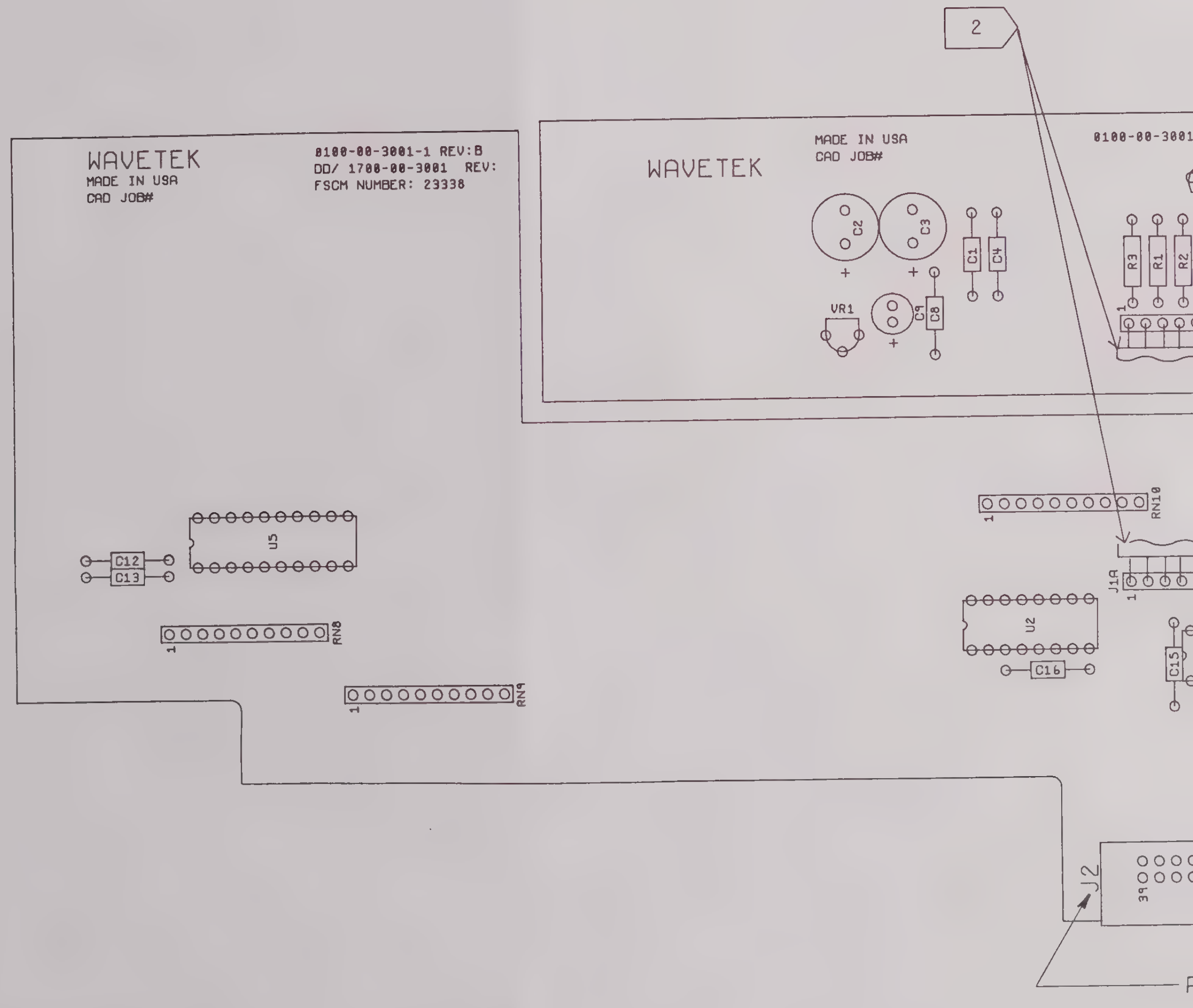
2 RIBBON CABLE IS INSTALLED BETWEEN J1A ON LOWER KEYBOARD PCB AND J1B ON UPPER DISPLAY PCB.

3 LEADS OF COMPONENTS MOUNTED ON COMPONENT SIDE OF PCB OPPOSITE DISPLAY (VFD1), MUST HAVE LEADS TRIMMED TO WITHIN .050 OF PCB SURFACE.

4 MOUNTING OF DI
A. INSTALL AND
B. TRIM LEADS
C. ATTACH DISP
POSITIONINC
D. PLACE DISPL
SIDE OF PCE
IS FLUSH TO
PINS OF CO
PIERCE THE
E. ALLOW DISPL
BEFORE SOL

5 LEDS (CR1 THRU

C


2
WAVETEK
MADE IN USA
CAD JOB#
0100-00-3001-1 REV:B
DD/ 1700-00-3001 REV:
FSCM NUMBER: 23338
WAVETEK
MADE IN USA
CAD JOB#
0100-00-3001
C2
C3
C1
C4
+
+
VR1
C9
C8
+
R3
R1
R2
1
C12
C13
U5
RN8
1
RN9
1
RN10
1
J1A
1
U2
C16
C15
J2
39
F

B

COMPONENT SIDE

A

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS ACCUPRESS

REV	ECN	BY	DATE	APP
A	ERO#90-462	𝒥T	7-11-90	
B	ECO 93-067	SC	12-2-92	JM

(VFD1):

ER COMPONENTS ON COMPONENT SIDE OF PCB.

MPONENT ON UPPER BOARD PER NOTE 3.

USHION (ITEM NO.3) TO DISPLAY,

ION SO THAT IT DOES NOT OVERLAP DISPLAY.

FD1) WITH ATTACHED CUSHION ON SOLDER

NG SURE THAT THE SURFACE OF THE CUSHION

PCB SURFACE.

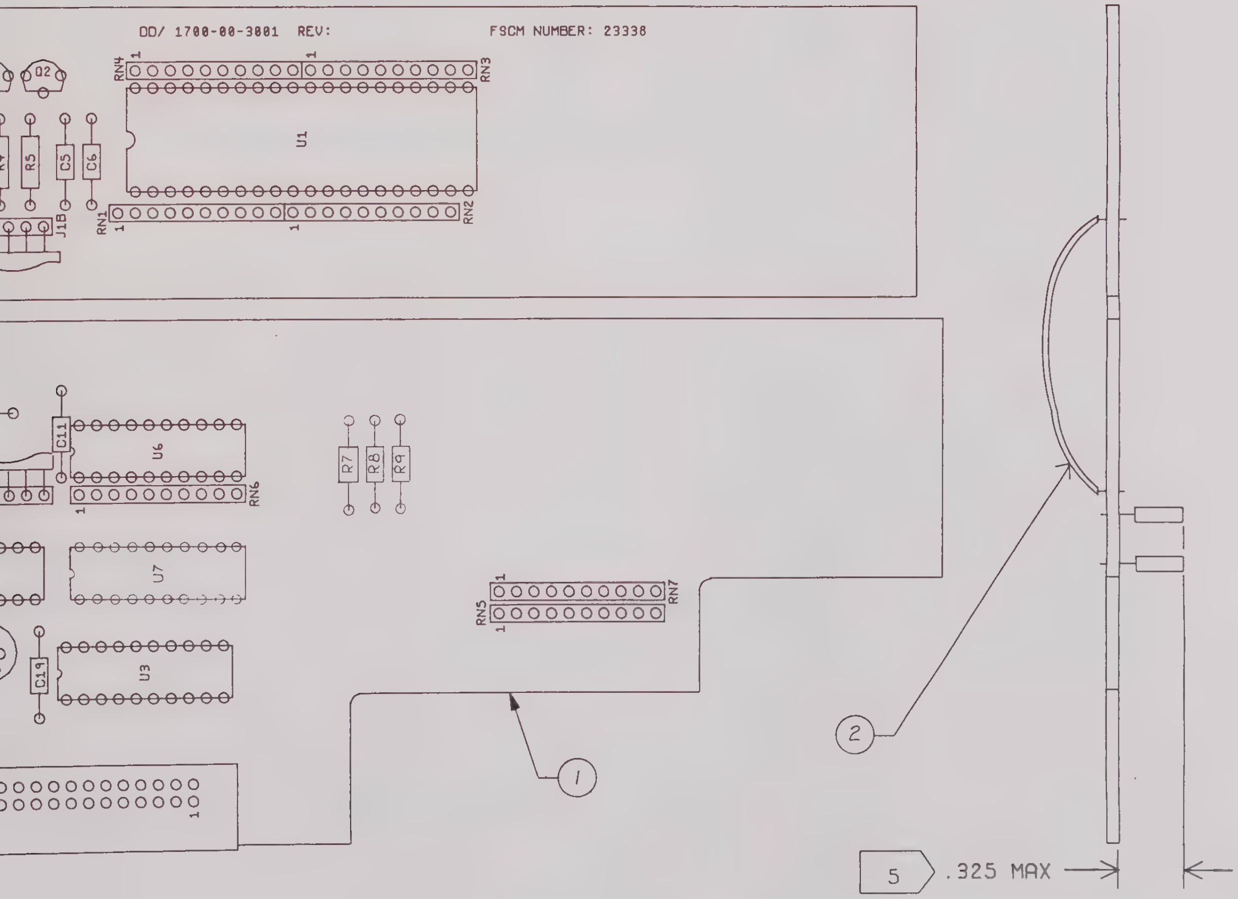
NTS ON OPPOSITE SIDE OF PCB WILL

ON.

FD1 ON COMPONENT SIDE) TO SELF-LEVEL

THE PINS OF DISPLAY.

) MAY BE MOUNTED FLUSH TO PCB.


DD/ 1700-00-3001 REV:
FSCM NUMBER: 23338
D2
RN4
1
1
RN3
U1
R5
C5
C6
J1B
RN1
1
1
RN2
C11
U6
1
RN6
R7
R8
R9
U7
1
RN5
1
RN7
C19
U3
10
①
②
5
.325 MAX

HIS CONNECTOR IS MARKED

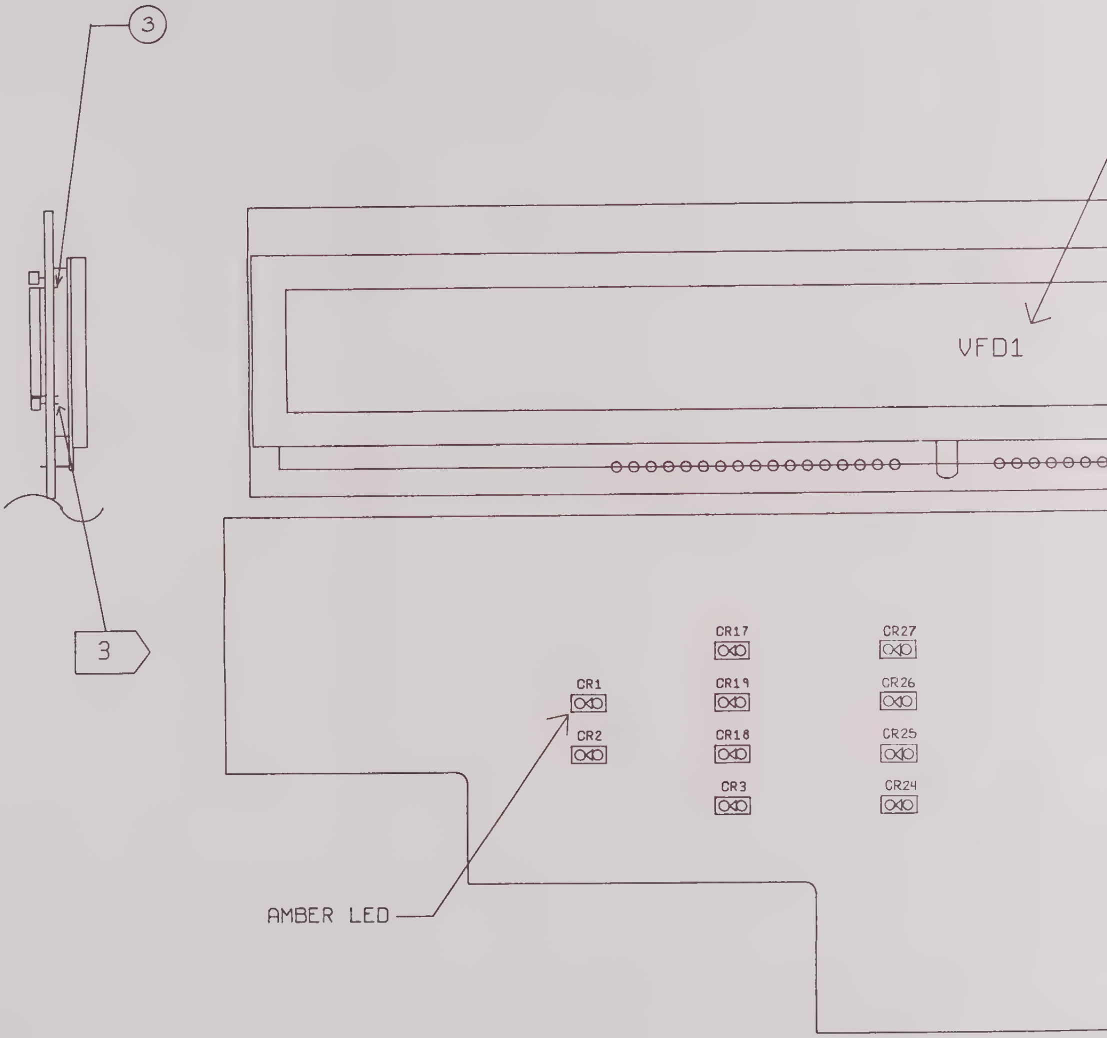
2 ON THE PC BOARD

ILKSCREEN

SEE SEPARATE PARTS LIST

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 7-1-90	WAVETEK SAN DIEGO • CALIFORNIA		
MATERIAL	PROJ ENGR [illegible]	7/9/90	TITLE PCB ASSEMBLY - DISPLAY/KEYBOARD		
	RELEASE APPROV JW	7/9/90			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± 010 ANGLES ± 1° .XX ± 030				
	DO NOT SCALE DWG		MODEL NO 90 SERIES	DWG NO 1101 -00-3322	REV B
	SCALE NONE		CODE IDENT 23338	SHEET 1 OF 2	

1101-00-3322 B

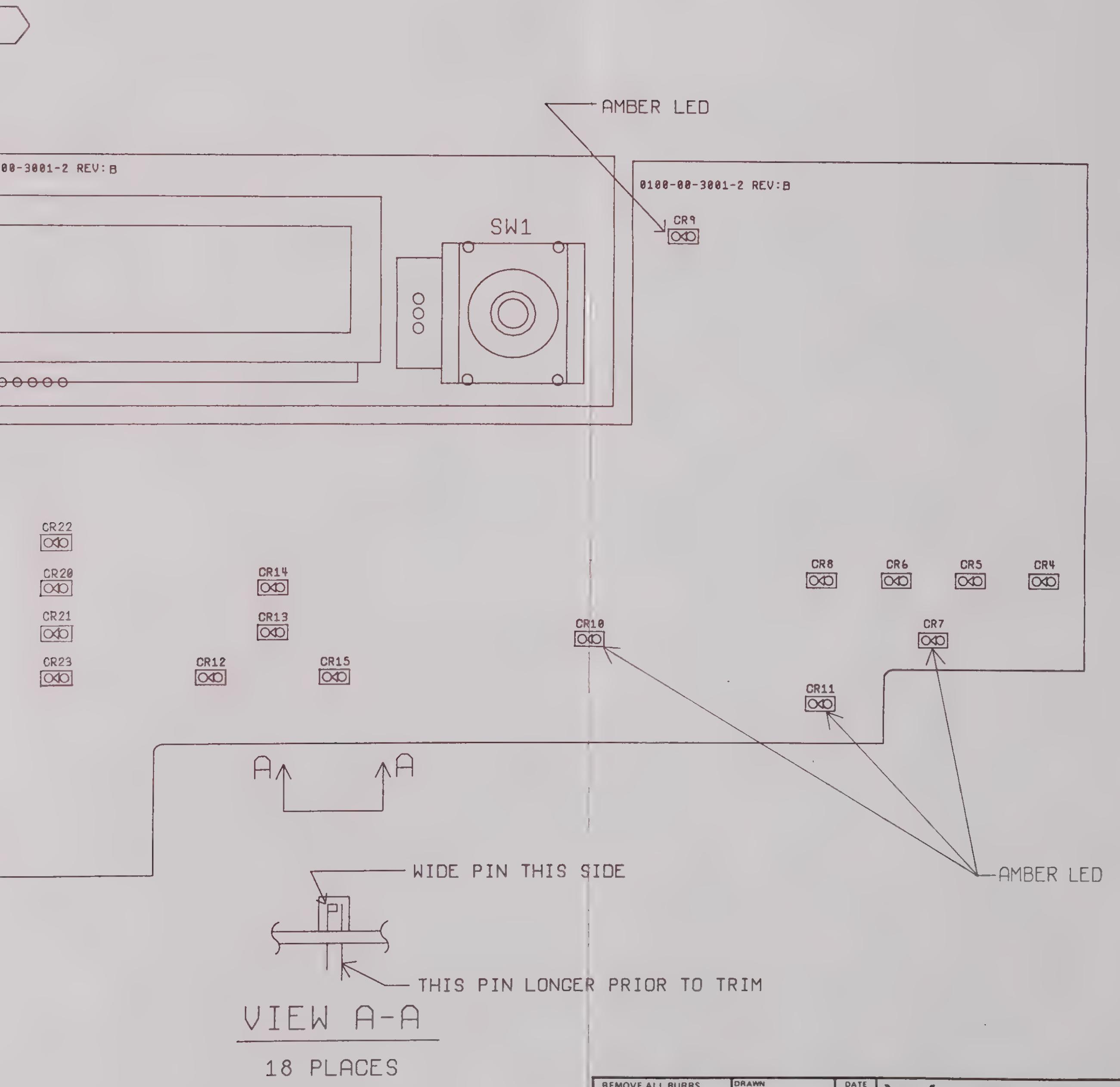

③
3
VFD1
CR17
CR27
CR1
CR19
CR26
CR2
CR18
CR25
CR3
CR24
AMBER LED

SOLDER SIDE

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS

REV	ECN	BY	DATE	APP


AMBER LED
00-3001-2 REV:B
0100-00-3001-2 REV:B
SW1
CR9
CR22
CR20
CR21
CR23
CR14
CR13
CR12
CR15
CR10
CR8
CR6
CR5
CR4
CR7
CR11
A
A
WIDE PIN THIS SIDE
P1
THIS PIN LONGER PRIOR TO TRIM
AMBER LED
VIEW A-A
18 PLACES

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN A. TALMADGE DATE 7-1-90
PROJ ENGR J. McCosh 7/9/90
RELEASE APPROV JM 7/9/90

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PCB ASSEMBLY -
DISPLAY/KEYBOARD

MODEL NO. 90 SERIES
DWG NO 1101-00-3322
REV B
CODE IDENT 23338
SHEET 2 OF 2

1101-00-3322 B

REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	A/D, DISPLAY/ KEYBOARD
NONE	S/D DISPLAY, KEYBOARD
NONE	CUSHION, DISPLAY
C1 C10 C11 C12 C13 C15 C16 C19 C4 C5 C6 C7 C8	CAP,CER,MON,.1MF,50V, AXIAL
C18 C2 C3	CAP,ELECT,100MF,35V RADIAL LEAD,SP .20
C9	CAP,ELECT,22MF,25V,RADIAL
NONE	PCB, DISPLAY/KEYBOARD REF: SPEC 0008-00-0455 REV C
NONE	CONN,HEADER,40 PIN,PCB MT, .1 CTR,2X20,SHRD
VFD1	DISPLAY,VAC,FLOUR
R7 R8 R9	RES,MF,1/8W,1%,100
R4 R5 R6	RES,MF,1/8W,1%,10K
R1 R2 R3	RES,MF,1/8W,1%,2.49K
RN5 RN6 RN9	RES NETWORK 10K 2%

WAVETEK
PARTS LIST

TITLE
PCA, DISPLAY/ KEYBOARD

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

G-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1-00-3322	WVTK	1101-00-3322	1
4-00-3322	WVTK	1104-00-3322	1
0-02-3510	WVTK	1400-02-3510	1
03Z5U104Z050A	CORNG	1500-01-0405	13
101M35V10X12.5	NIC	1500-31-0102	3
25VB22RM6X7LL	UNCON	1500-32-2002	1
0-00-3001	WVTK	1700-00-3001	1
02692-3	AMP	2100-02-0258	1
611A1	ITRON	2400-03-0019	1
5D-1000F	TRW	4701-03-1000	3
5D-1002F	TRW	4701-03-1002	3
5D-2491F	TRW	4701-03-2491	3
0R-101-103	BOURN	4770-00-0008	3

ASSEMBLY NO. 1100-00-3322 REV C

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	10PIN SIP BUSS				
RN1 RN2 RN3 RN4	RES NETWORK 47K 2% 10PIN SIP BUSS	4310R-101-473	BOURN	4770-00-0030	4
RN10 RN7 RN8	RES NETWORK 10PIN SIP 100 OHM BUSS	4310R-101-101	BOURN	4770-00-0054	3
CR1 CR10 CR11 CR7 CR9	LED, AMBER, RECT BAR	LTL-3271A	LITE	4899-00-0056	5
CR12 CR13 CR14 CR15 CR17 CR18 CR19 CR2 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR3 CR4 CR5 CR6 CR8	LED, GREEN, RECT BAR	LTL-3231A	LITE	4899-00-0057	21
Q1 Q2 Q3	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	3
SW1	ENCODER, ROTARY, MADE FROM 5104-00-0027	5109-00-0001	WVTK	5109-00-0001	1
J1A	CABLE, FLEX, JMP, ASSY	1-86943-1	AMP	6001-60-0017	1
VR1	VOLT REGULATOR, POSITIVE	78L15	TI	7000-78-1501	1
U2	MUX/DEMUX, ANALOG	CD4051BE	RCA	8000-40-5100	1
U1	CONTROLLER, ALPH NUM DISP, 40V	10957P-50	ROCK	8001-09-5700	1
U4	DECODER/DEMUX, 3 TO 8 LINE	SN74ALS138N	TI	8007-41-3800	1

WAVETEK
PARTS LIST

TITLE
PCA, DISPLAY/ KEYBOARD

ASSEMBLY NO. 1100-00-3322 REV C

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U3 U5 U6 U7	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	4

WAVETEK
PARTS LIST

TITLE
PCA, DISPLAY/ KEYBOARD

ASSEMBLY NO. 1100-00-3322 REV C

PAGE 3

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

	DATE
DRAWN	
CHECKED	
PROJ. ENGR.	
RELEASE APPROV.	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:

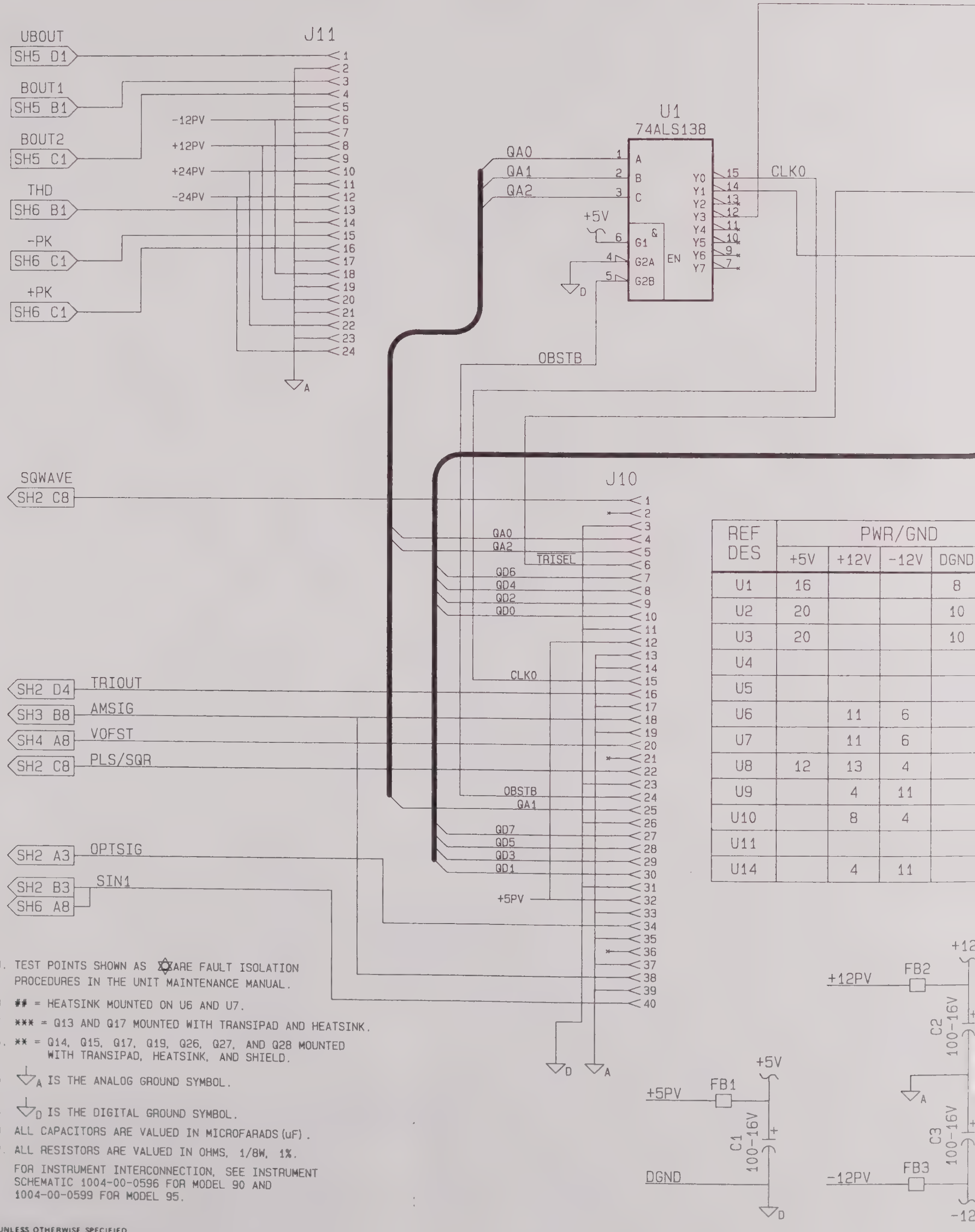
FRACTIONS	DECIMALS	ANGLES
±	.XX ± .XXX ±	±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
FRONT PANEL

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-3322	C

SCALE MODEL 95 SHEET 1 OF 1


D
C
B
A
UBOUT
SH5 D1
BOUT1
SH5 B1
BOUT2
SH5 C1
THD
SH6 B1
-PK
SH6 C1
+PK
SH6 C1
-12PV
+12PV
+24PV
-24PV
J11
U1
74ALS138
QA0
QA1
QA2
A
B
C
+5V
G1
G2A
G2B
EN
&
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
CLK0
OBSTB
SQWAVE
SH2 C8
J10
QA0
QA2
TRISEL
QD6
QD4
QD2
QD0
CLK0
SH2 D4
TRIOUT
SH3 B8
AMSIG
SH4 A8
VOFST
SH2 C8
PLS/SQR
OBSTB
QA1
QD7
QD5
QD3
QD1
SH2 A3
OPTSIG
SH2 B3
SH6 A8
SIN1
+5PV
+5V
+5PV
FB1
C1
100-16V
DGND
+12PV
FB2
C2
100-16V
-12PV
FB3
C3
100-16V
+12
-12

REF DES	PWR/GND			
	+5V	+12V	-12V	DGND
U1	16			8
U2	20			10
U3	20			10
U4				
U5				
U6		11	6	
U7		11	6	
U8	12	13	4	
U9		4	11	
U10		8	4	
U11				
U14		4	11	

9. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.

8 ## = HEATSINK MOUNTED ON U6 AND U7.

7 *** = Q13 AND Q17 MOUNTED WITH TRANSIPAD AND HEATSINK.

6. ** = Q14, Q15, Q17, Q19, Q26, Q27, AND Q28 MOUNTED WITH TRANSIPAD, HEATSINK, AND SHIELD.

5 ▽A IS THE ANALOG GROUND SYMBOL.

4 ▽D IS THE DIGITAL GROUND SYMBOL.

3 ALL CAPACITORS ARE VALUED IN MICROFARADS (uF).

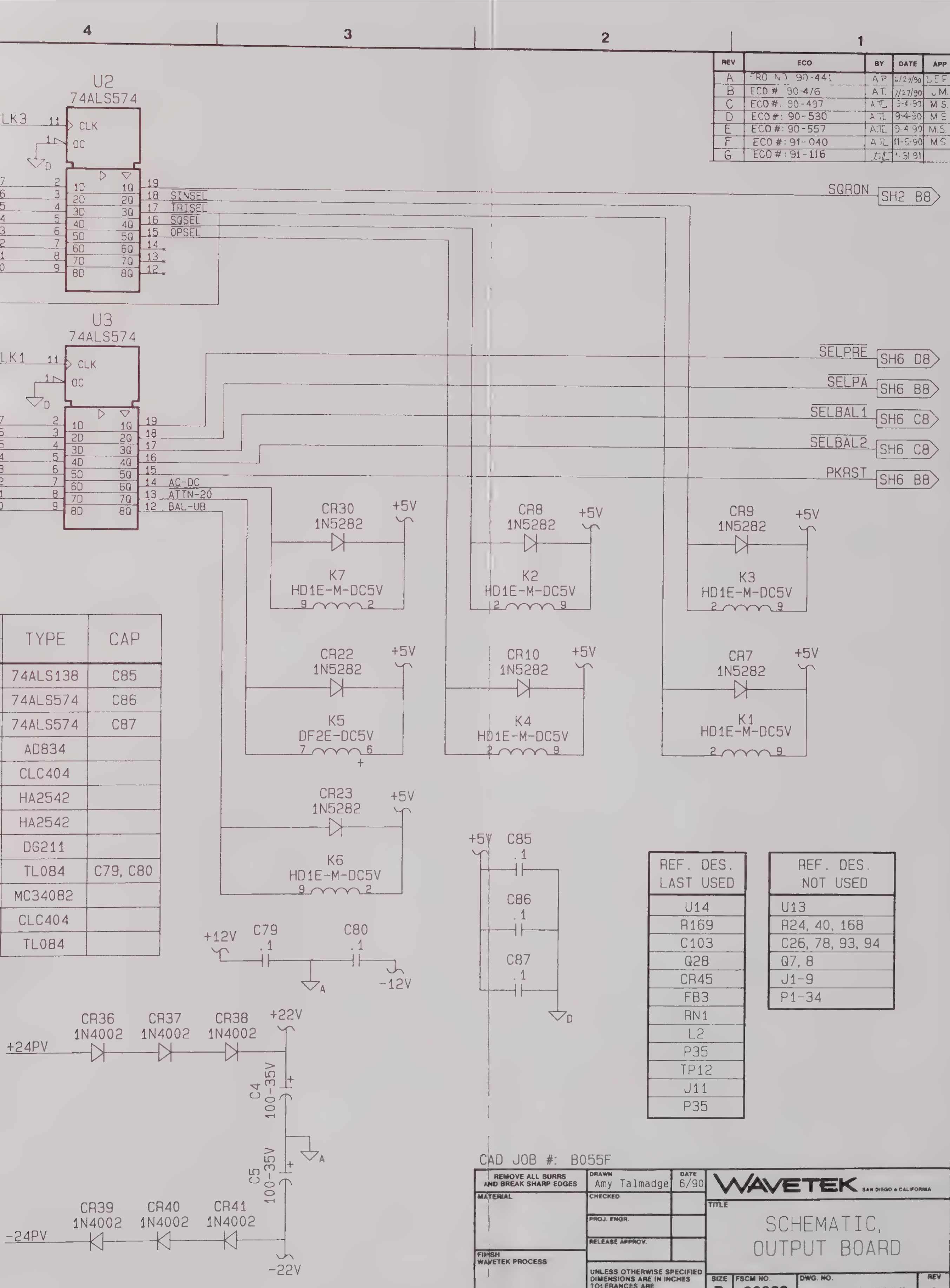
2. ALL RESISTORS ARE VALUED IN OHMS, 1/8W, 1%.

1 FOR INSTRUMENT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596 FOR MODEL 90 AND 1004-00-0599 FOR MODEL 95.

NOTE UNLESS OTHERWISE SPECIFIED

]

REV	ECO	BY	DATE	APP
A	ERO NO 90-441	AP	6/29/90	UEF
B	ECO # 90-416	AT.	7/27/90	JM.
C	ECO #. 90-497	ATL	9-4-90	M S.
D	ECO #: 90-530	ATL	9-4-90	M S
E	ECO #: 90-557	ATL	9-4 90	M.S.
F	ECO #: 91-040	ATL	11-5-90	M S
G	ECO #: 91-116	ATL	1-31 91	


4
3
2
1
D
B
A
U2
74ALS574
LK3
11
CLK
1
OC
D
2 1D 1Q 19
3 2D 2Q 18 SINSEL
4 3D 3Q 17 TRISEL
5 4D 4Q 16 SQSEL
6 5D 5Q 15 OPSEL
7 6D 6Q 14
8 7D 7Q 13
9 8D 8Q 12
SQRON
SH2 B8
U3
74ALS574
LK1
11
CLK
1
OC
D
2 1D 1Q 19
3 2D 2Q 18
4 3D 3Q 17
5 4D 4Q 16
6 5D 5Q 15
7 6D 6Q 14 AC-DC
8 7D 7Q 13 ATTN-20
9 8D 8Q 12 BAL-UB
SELPRE
SH6 D8
SELPA
SH6 B8
SELBAL1
SH6 C8
SELBAL2
SH6 C8
PKRST
SH6 B8
CR30
1N5282
+5V
K7
HD1E-M-DC5V
9 2
CR8
1N5282
+5V
K2
HD1E-M-DC5V
2 9
CR9
1N5282
+5V
K3
HD1E-M-DC5V
2 9
CR22
1N5282
+5V
K5
DF2E-DC5V
7 6
+
CR10
1N5282
+5V
K4
HD1E-M-DC5V
2 9
CR7
1N5282
+5V
K1
HD1E-M-DC5V
2 9
CR23
1N5282
+5V
K6
HD1E-M-DC5V
9 2
+5V
C85
.1
C86
.1
C87
.1
D
+12V
C79
.1
C80
.1
A
-12V
CR36
1N4002
CR37
1N4002
CR38
1N4002
+22V
+24PV
C4
100-35V
+
A
C5
100-35V
+
CR39
1N4002
CR40
1N4002
CR41
1N4002
-24PV
-22V

TYPE	CAP
74ALS138	C85
74ALS574	C86
74ALS574	C87
AD834	
CLC404	
HA2542	
HA2542	
DG211	
TL084	C79, C80
MC34082	
CLC404	
TL084	

REF. DES. LAST USED
U14
R169
C103
Q28
CR45
FB3
RN1
L2
P35
TP12
J11
P35

REF. DES. NOT USED
U13
R24, 40, 168
C26, 78, 93, 94
Q7, 8
J1-9
P1-34

93-028

1104-00 3335 K.L

92-049

1104-00 3335

1104-00-3335 G

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/90
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO • CALIFORNIA

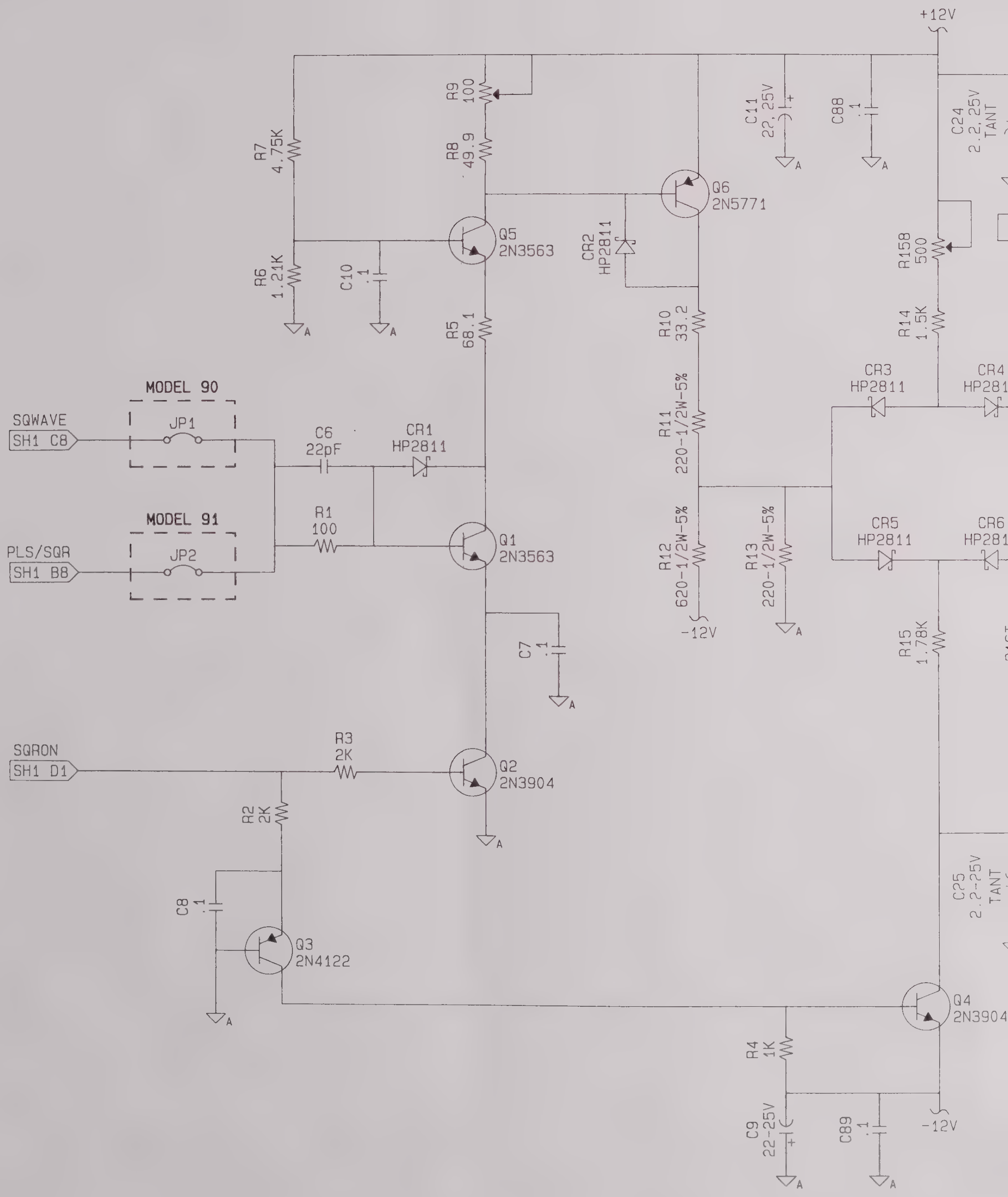
TITLE

SCHEMATIC,
OUTPUT BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3335	G

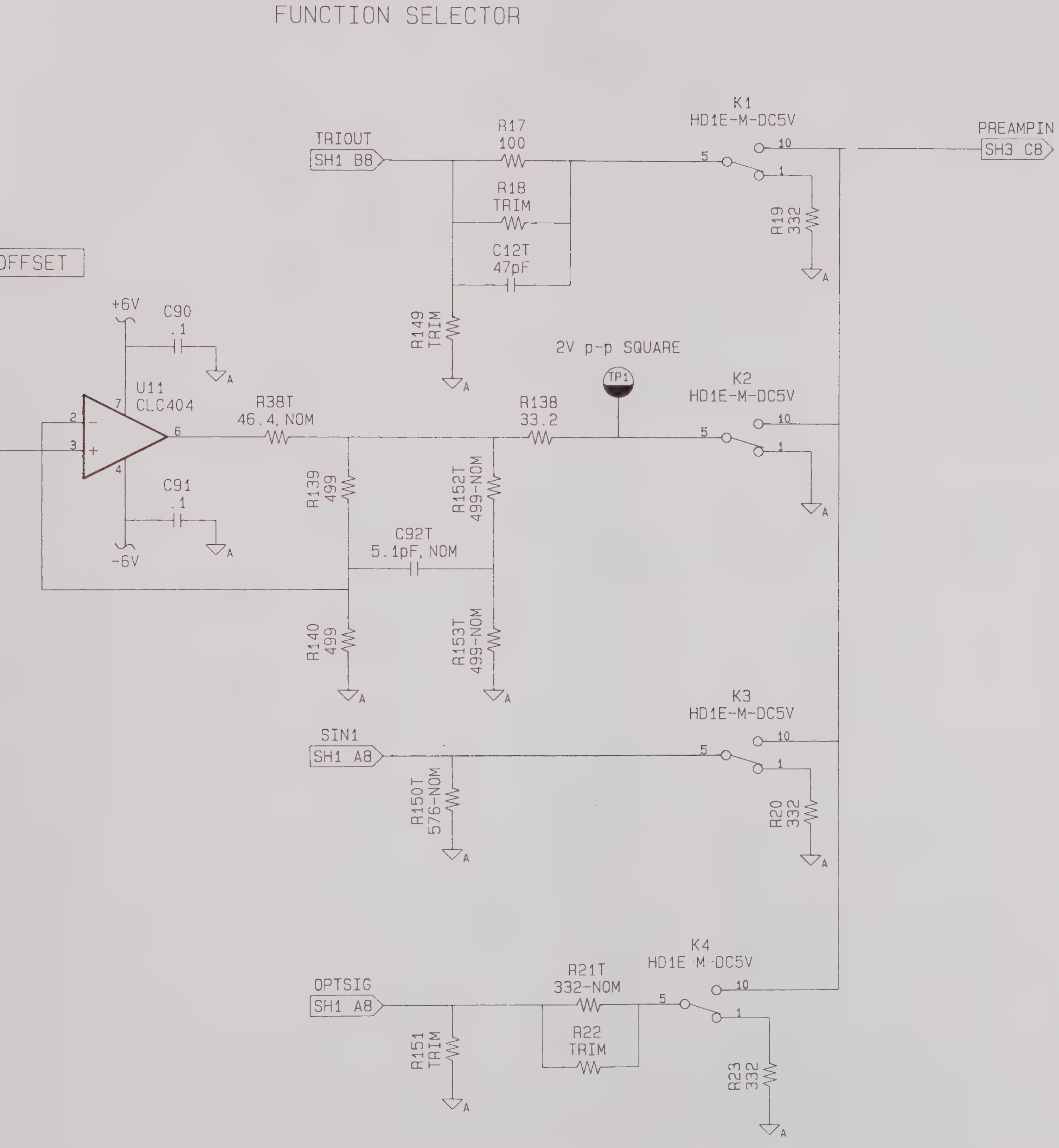
SCALE NONE MODEL 90 SERIES SHEET 1 OF 6

SQUARE SHAPER


8
7
6
5
D
C
B
A
+12V
R9 100
R8 49.9
R7 4.75K
R6 1.21K
C10 .1
R5 68.1
Q5 2N3563
Q6 2N5771
CR2 HP2811
C11 22,25V
C88 .1
C24 2.2,25V TANT
R158 500
R10 33.2
R14 1.5K
R11 220-1/2W-5%
CR3 HP2811
CR4 HP281
MODEL 90
SQWAVE
SH1 C8
JP1
C6 22pF
CR1 HP2811
MODEL 91
PLS/SQR
SH1 B8
JP2
R1 100
Q1 2N3563
R12 620-1/2W-5%
R13 220-1/2W-5%
-12V
CR5 HP2811
CR6 HP281
C7 .1
R15 1.78K
SQRON
SH1 D1
R3 2K
Q2 2N3904
R2 2K
C8 .1
Q3 2N4122
C25 2.2-25V TANT
Q4 2N3904
R4 1K
C9 22-25V
C89 .1
-12V
A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


FUNCTION SELECTOR
TRIOUT
SH1 B8
R17
100
R18
TRIM
C12T
47pF
R149
TRIM
K1
HD1E-M-DC5V
5
10
1
R19
332
A
PREAMPIN
SH3 C8
FFSET
+6V
C90
.1
U11
CLC404
2
3
7
4
6
C91
.1
-6V
R38T
46.4, NOM
R139
499
R152T
499-NOM
C92T
5.1pF, NOM
R140
499
R153T
499-NOM
R138
33.2
2V p-p SQUARE
TP1
K2
HD1E-M-DC5V
SIN1
SH1 A8
R150T
576-NOM
K3
HD1E-M-DC5V
R20
332
OPTSIG
SH1 A8
R151
TRIM
R21T
332-NOM
R22
TRIM
K4
HD1E M DC5V
R23
332

1104-00-3335 G

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN Amy Talmadge DATE 6/90
CHECKED
PROJ. ENGR.
RELEASE APPROV

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES

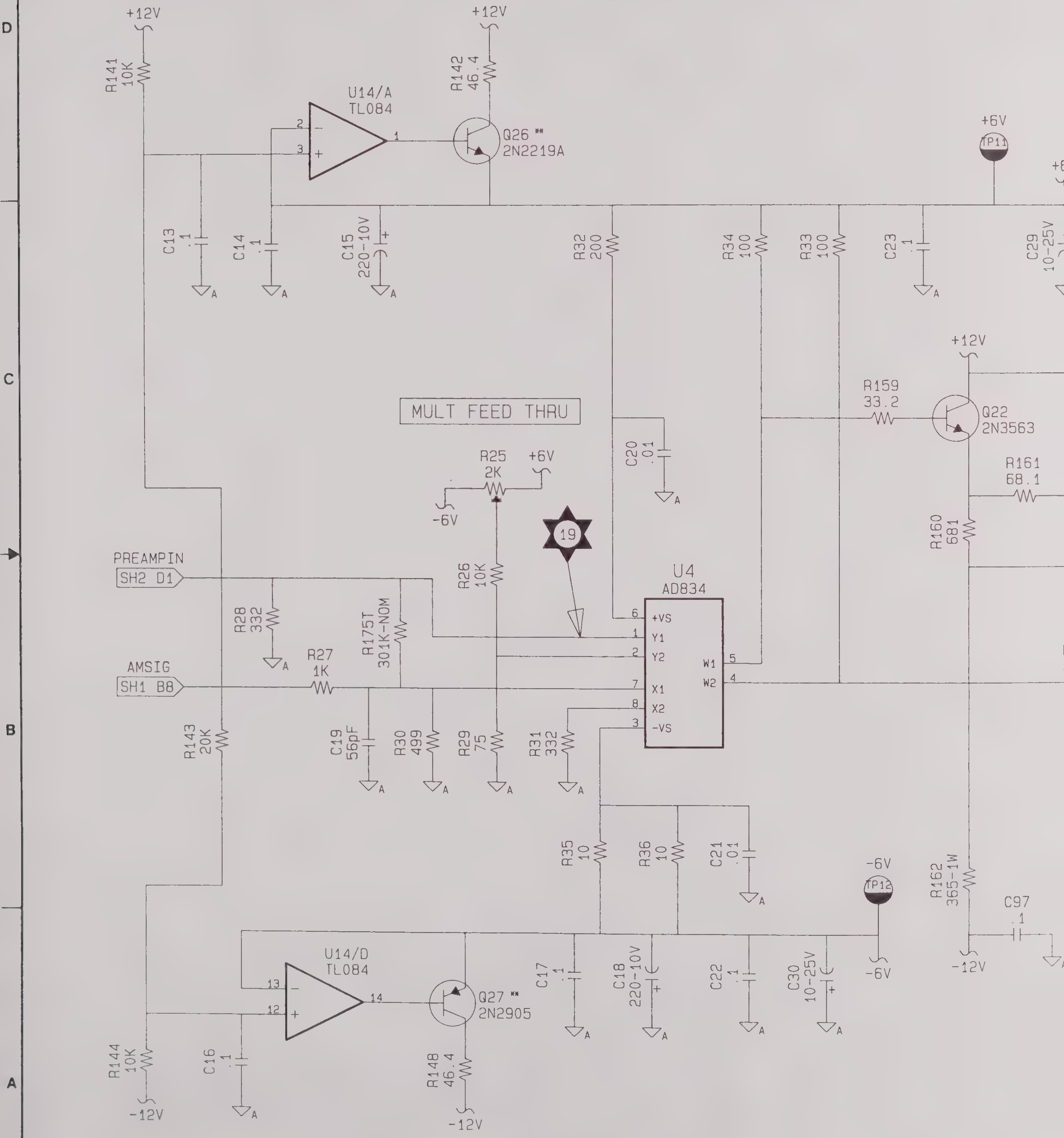
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
OUTPUT BOARD

SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3335 REV G
SCALE NONE MODEL 90 SERIES SHEET 2 OF 6

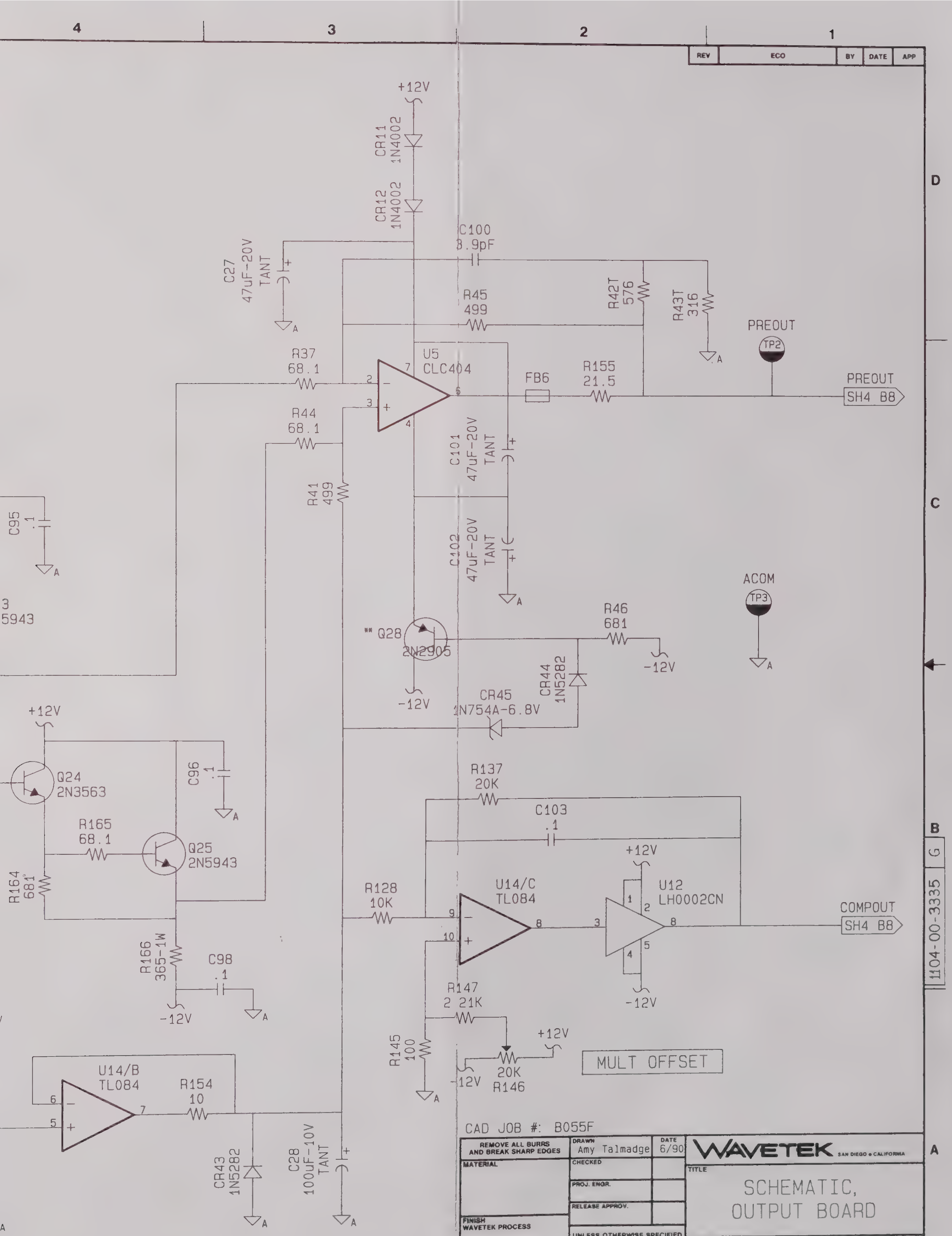
8 7 6 5

PREAMPLIFIER AND MULTIPLIER


D
C
B
A
+12V
R141 10K
U14/A TL084
2
3
1
R142 46.4
Q26 ** 2N2219A
+6V
TP11
C13 .1
C14 .1
C15 220-10V
R32 200
R34 100
R33 100
C23 .1
C29 10-25V
A
+12V
R159 33.2
Q22 2N3563
R161 68.1
R160 681
MULT FEED THRU
R25 2K
+6V
-6V
C20 .01
19
PREAMPIN
SH2 D1
R26 10K
U4 AD834
6 +VS
1 Y1
2 Y2
7 X1
8 X2
3 -VS
W1 5
W2 4
R28 332
R175T 301K-NOM
AMSIG
SH1 B8
R27 1K
R143 20K
C19 56pF
R30 499
R29 75
R31 332
R35 10
R36 10
C21 .01
-6V
TP12
R162 365-1W
C97 .1
-6V
-12V
U14/D TL084
13
12
14
Q27 ** 2N2905
C17 .1
C18 220-10V
C22 .1
C30 10-25V
R144 10K
C16 .1
R148 46.4
-12V
-12V

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5


4
3
2
1
REV
ECO
BY
DATE
APP
D
C
B
A
+12V
CR11
1N4002
CR12
1N4002
C100
3.9pF
C27
47uF-20V
TANT
R45
499
R42T
576
R43T
316
PREOUT
TP2
R37
68.1
U5
CLC404
2
3
7
6
4
FB6
R155
21.5
PREOUT
SH4 B8
R44
68.1
C101
47uF-20V
TANT
R41
499
C95
.1
C102
47uF-20V
TANT
3
5943
ACOM
TP3
R46
681
** Q28
2N2905
-12V
CR44
1N5282
-12V
CR45
1N754A-6.8V
+12V
Q24
2N3563
C96
.1
R137
20K
C103
.1
R165
68.1
Q25
2N5943
+12V
R164
681
R128
10K
U14/C
TL084
9
10
8
U12
LH0002CN
1
2
3
8
5
4
COMPOUT
SH4 B8
R166
365-1W
C98
.1
-12V
R147
2 21K
-12V
+12V
R145
100
-12V
20K
R146
MULT OFFSET
U14/B
TL084
6
5
7
R154
10
CR43
1N5282
C28
100uF-10V
TANT
A
1104-00-3335
G

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES

DRAWN Amy Talmadge DATE 6/90

CHECKED

PROJ. ENGR.

RELEASE APPROV.

MATERIAL

FINISH
WAVETEK PROCESS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

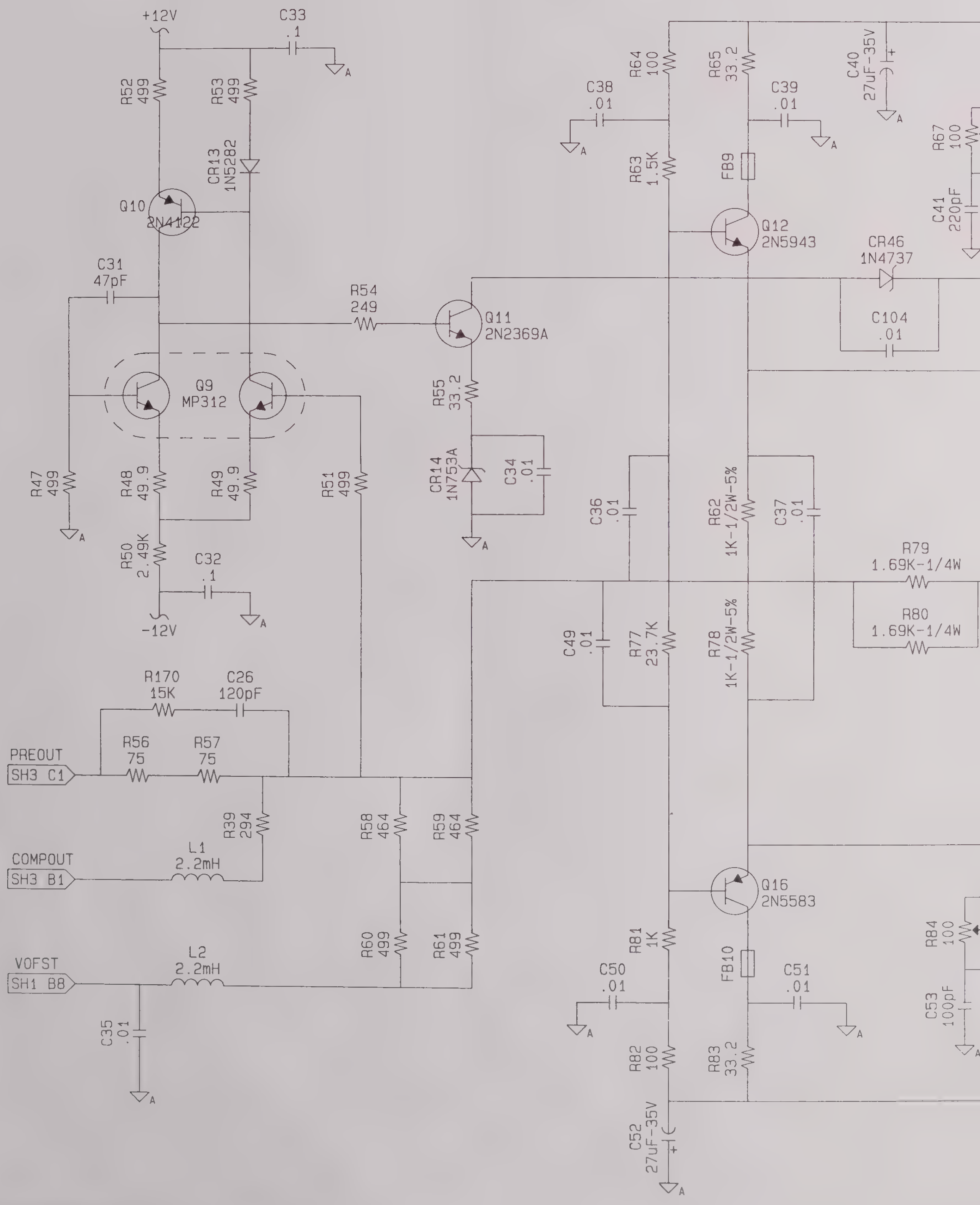
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
OUTPUT BOARD

SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3335 REV G

SCALE NONE MODEL 90 SERIES SHEET 3 OF 6

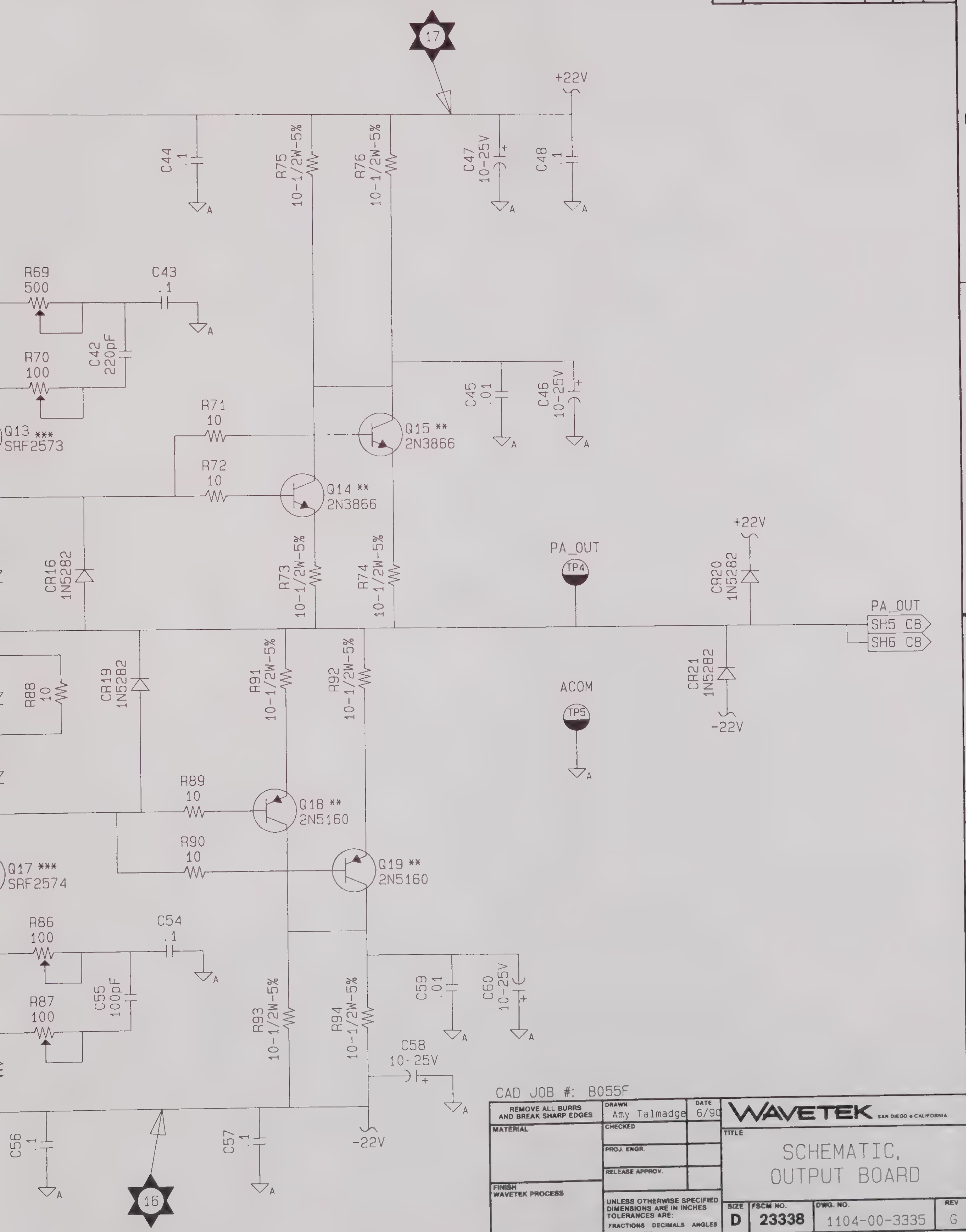
POWER AMP



8
7
6
5
D
C
B
A
+12V
C33
.1
R52
499
R53
499
CR13
1N5282
Q10
2N4122
C31
47pF
R54
249
Q11
2N2369A
Q9
MP312
R55
33.2
CR14
1N753A
C34
.01
R47
499
R48
49.9
R49
49.9
R51
499
R50
2.49K
C32
.1
-12V
R170
15K
C26
120pF
PREOUT
SH3 C1
R56
75
R57
75
R39
294
COMPOUT
SH3 B1
L1
2.2mH
R58
464
R59
464
R60
499
R61
499
VOFST
SH1 B8
L2
2.2mH
C35
.01
C38
.01
R64
100
R65
33.2
C39
.01
C40
27uF-35V
R67
100
R63
1.5K
FB9
Q12
2N5943
C41
220pF
CR46
1N4737
C104
.01
C36
.01
R62
1K-1/2W-5%
C37
.01
R79
1.69K-1/4W
R80
1.69K-1/4W
C49
.01
R77
23.7K
R78
1K-1/2W-5%
Q16
2N5583
R84
100
R81
1K
FB10
C50
.01
C51
.01
C53
100pF
R82
100
R83
33.2
C52
27uF-35V
A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP



17
+22V
C44
.1
R75
10-1/2W-5%
R76
10-1/2W-5%
C47
10-25V
C48
.1
A
R69
500
C43
.1
R70
100
C42
220pF
C45
.01
C46
10-25V
R71
10
Q13 ***
SRF2573
Q15 **
2N3866
R72
10
Q14 **
2N3866
+22V
PA_OUT
TP4
CR16
1N5282
R73
10-1/2W-5%
R74
10-1/2W-5%
CR20
1N5282
PA_OUT
SH5 C8
SH6 C8
R88
10
CR19
1N5282
R91
10-1/2W-5%
R92
10-1/2W-5%
CR21
1N5282
ACOM
TP5
-22V
R89
10
Q18 **
2N5160
R90
10
Q17 ***
SRF2574
Q19 **
2N5160
R86
100
C54
.1
C55
100pF
R87
100
R93
10-1/2W-5%
R94
10-1/2W-5%
C59
.01
C60
10-25V
C58
10-25V
C56
.1
C57
.1
-22V
16
4
3
2
1
D
C
B
A
1104-00-3335 G

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES

DRAWN Amy Talmadge DATE 6/90

CHECKED

PROJ. ENGR.

RELEASE APPROV.

MATERIAL

FINISH
WAVETEK PROCESS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

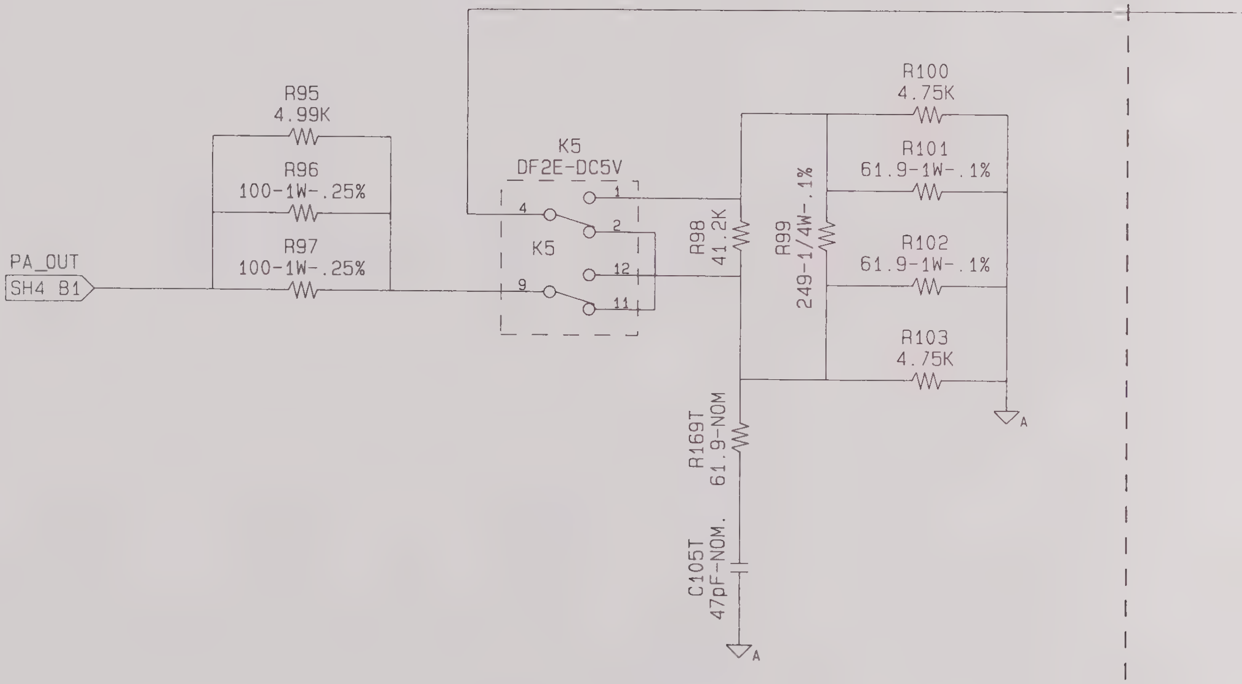
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
OUTPUT BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3335	G

SCALE NONE MODEL 90 SERIES SHEET 4 OF 6

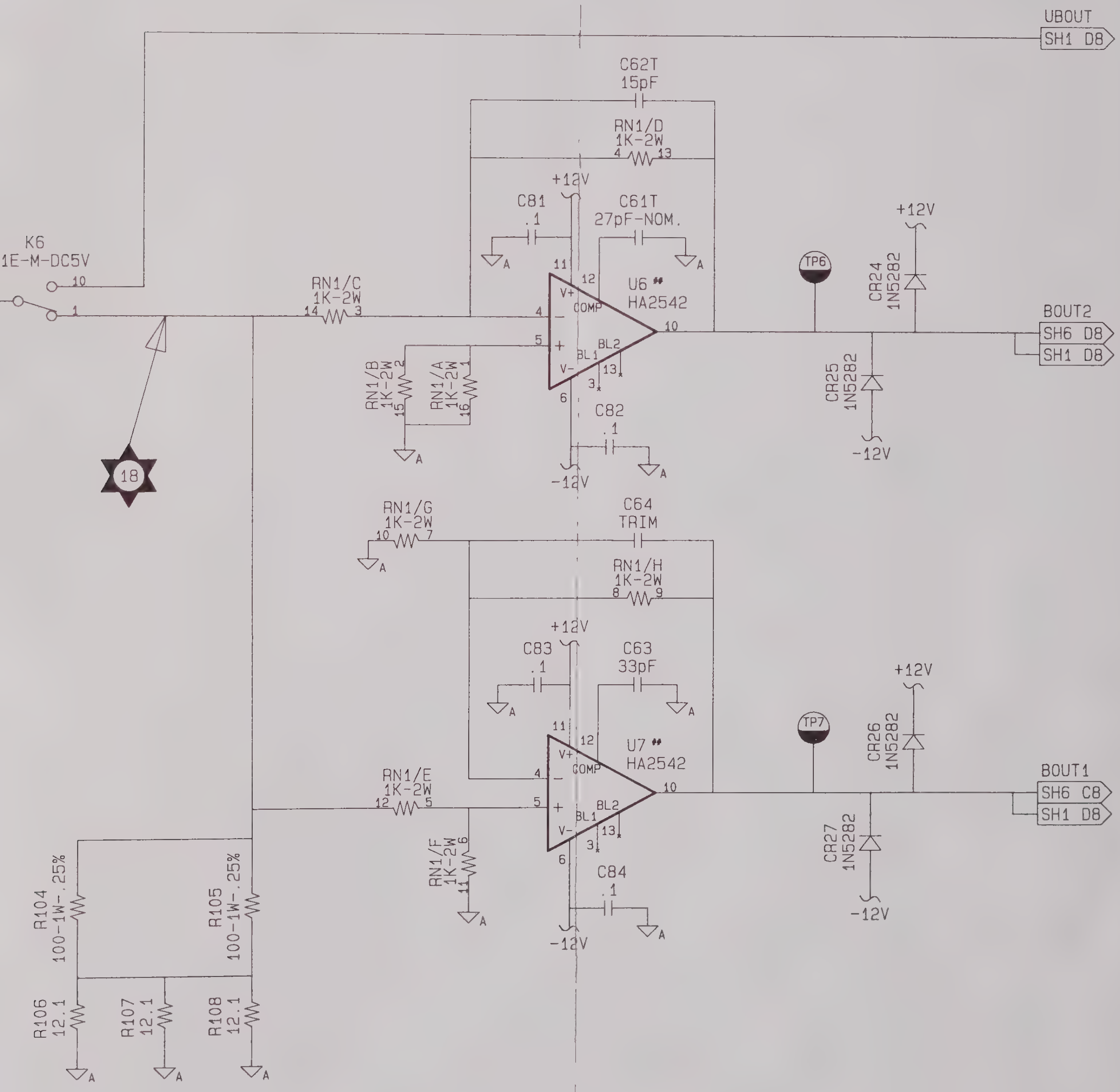
-20dB ATTENUATOR


PA_OUT
SH4 B1
R95
4.99K
R96
100-1W-.25%
R97
100-1W-.25%
K5
DF2E-DC5V
K5
4
1
2
12
9
11
R98
41.2K
R99
249-1/4W-.1%
R100
4.75K
R101
61.9-1W-.1%
R102
61.9-1W-.1%
R103
4.75K
A
R169T
61.9-NOM
C105T
47pF-NOM.
A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

BALANCED DRIVERS


UBOUT
SH1 D8
C62T
15pF
RN1/D
1K-2W
4
13
+12V
C81
.1
C61T
27pF-NOM.
K6
1E-M-DC5V
10
1
RN1/C
1K-2W
14
3
11
12
U6 **
HA2542
V+
COMP
4
5
BL2
BL1
V-
13
3
6
10
TP6
+12V
CR24
1N5282
BOUT2
SH6 D8
SH1 D8
CR25
1N5282
-12V
RN1/B
1K-2W
2
15
RN1/A
1K-2W
1
16
C82
.1
-12V
A
18
RN1/G
1K-2W
10
7
C64
TRIM
RN1/H
1K-2W
8
9
+12V
C83
.1
C63
33pF
11
12
U7 **
HA2542
TP7
+12V
CR26
1N5282
BOUT1
SH6 C8
SH1 D8
RN1/E
1K-2W
12
5
4
5
10
BL2
BL1
13
3
6
RN1/F
1K-2W
6
11
C84
.1
CR27
1N5282
-12V
-12V
R104
100-1W-.25%
R105
100-1W-.25%
R106
12.1
R107
12.1
R108
12.1

1104-00-3335 | G

CAD JOB #: B055F

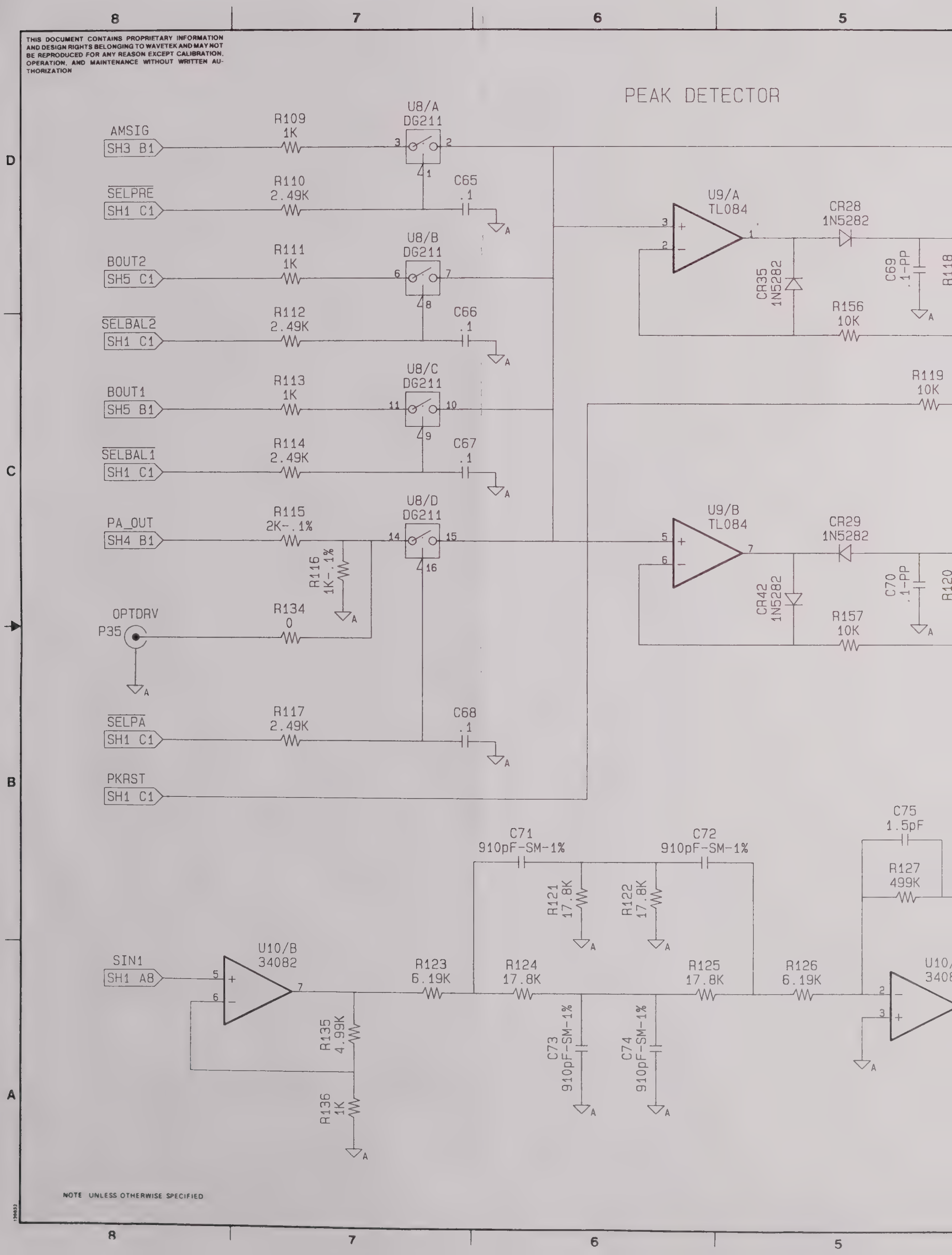
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

DRAWN Amy Talmadge DATE 6/90
CHECKED
PROJ. ENGR
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

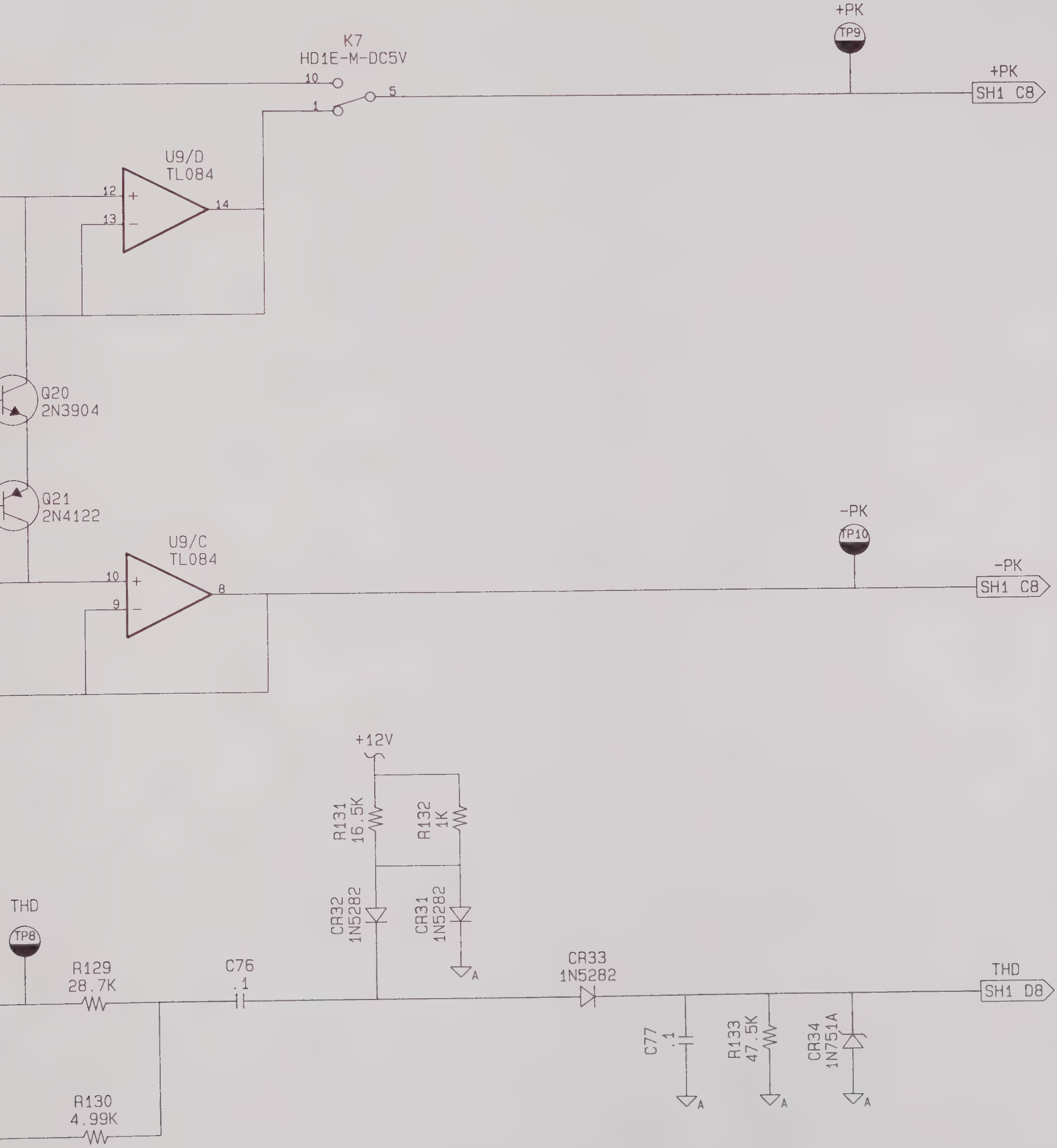
TITLE
SCHEMATIC,
OUTPUT BOARD

SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3335 REV G
SCALE NONE MODEL 90 SERIES SHEET 5 OF 6


8
7
6
5
D
C
B
A
PEAK DETECTOR
AMSIG
SH3 B1
R109
1K
U8/A
DG211
SELPRE
SH1 C1
R110
2.49K
C65
.1
BOUT2
SH5 C1
R111
1K
U8/B
DG211
SELBAL2
SH1 C1
R112
2.49K
C66
.1
BOUT1
SH5 B1
R113
1K
U8/C
DG211
SELBAL1
SH1 C1
R114
2.49K
C67
.1
PA_OUT
SH4 B1
R115
2K-.1%
R116
1K-.1%
U8/D
DG211
OPTDRV
P35
R134
0
SELPA
SH1 C1
R117
2.49K
C68
.1
PKRST
SH1 C1
U9/A
TL084
CR28
1N5282
CR35
1N5282
C69
.1-PP
R118
R156
10K
R119
10K
U9/B
TL084
CR29
1N5282
CR42
1N5282
C70
.1-PP
R120
R157
10K
C71
910pF-SM-1%
C72
910pF-SM-1%
R121
17.8K
R122
17.8K
C75
1.5pF
R127
499K
SIN1
SH1 A8
U10/B
34082
R123
6.19K
R124
17.8K
R125
17.8K
R126
6.19K
U10/
3408
R135
4.99K
R136
1K
C73
910pF-SM-1%
C74
910pF-SM-1%
A

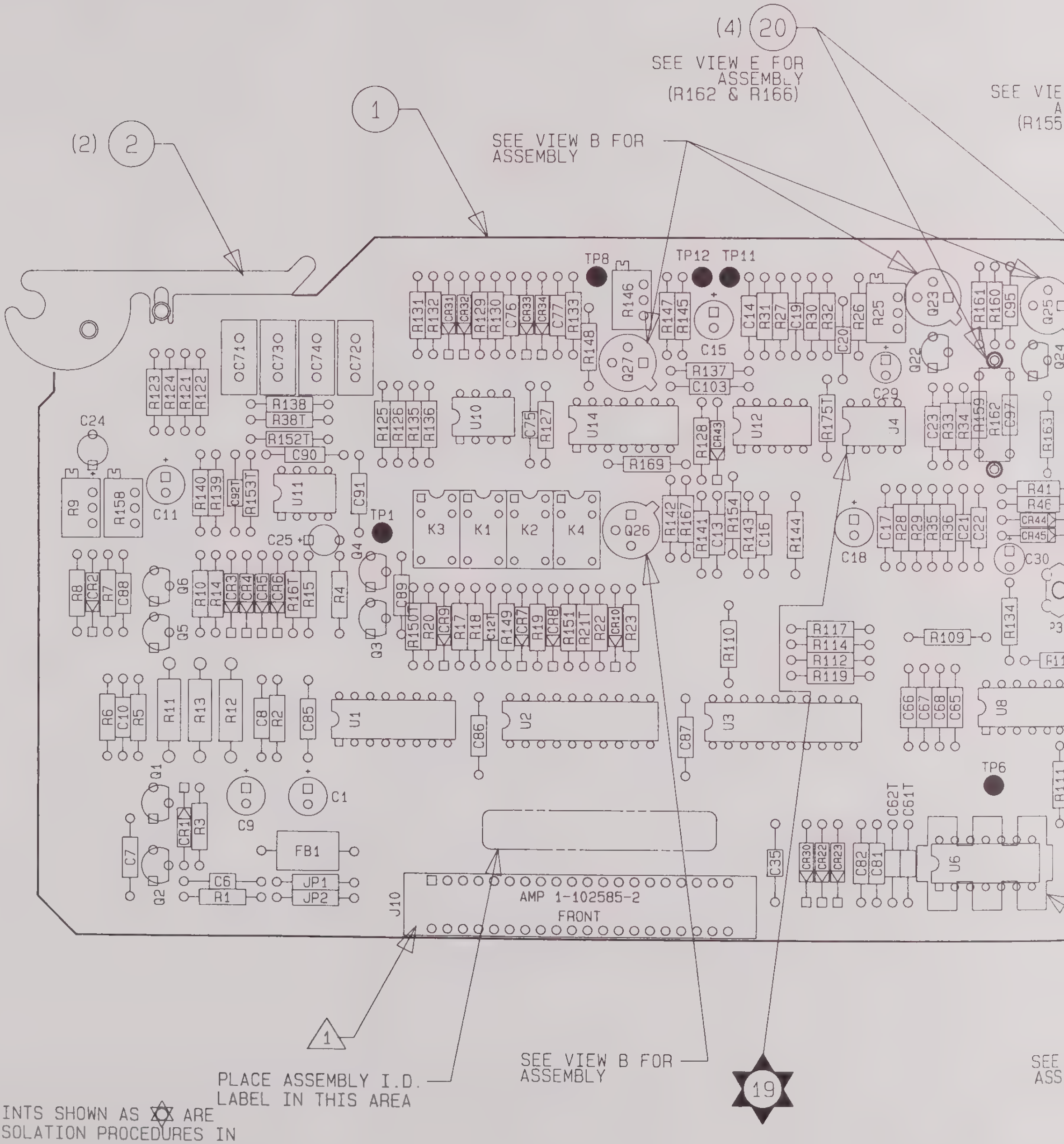
NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


K7
HD1E-M-DC5V
10
1
5
+PK
TP9
+PK
SH1 C8
U9/D
TL084
12
13
14
Q20
2N3904
Q21
2N4122
U9/C
TL084
10
9
8
-PK
TP10
-PK
SH1 C8
+12V
R131
16.5K
R132
1K
CR32
1N5282
CR31
1N5282
A
THD
TP8
R129
28.7K
C76
.1
CR33
1N5282
THD
SH1 D8
C77
.1
R133
47.5K
CR34
1N751A
A
A
A
R130
4.99K

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE SCHEMATIC, OUTPUT BOARD
	PROJ ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3335 REV G
DO NOT SCALE DRAWING			SCALE NONE MODEL 90 SERIES SHEET 6 OF 6


8
7
6
5
D
C
B
A
(4) 20
SEE VIEW E FOR ASSEMBLY (R162 & R166)
SEE VIE
A
(R155
1
(2) 2
SEE VIEW B FOR ASSEMBLY
TP8
TP12
TP11
TP1
TP6
R131 R132 CR31 CR32 R129 R130 C76 CR33 CR34 C77 R133
R146
R148
Q27
R147 R145
C15
C14 R31 R27 C19 R30 R32 C20 R26 R25
Q23
R161 R160 C95
Q25
Q22
Q24
R137
C103
C29
C71 C73 C74 C72
R123 R124 R121 R122
R138
R38T
R152T
C90
R125 R126 R135 R136
U10
C75 R127
U14
R169
R128 CR43
U12
R175T
J4
C23 R33 R34 R159 R162 C97
R163
C24
R9
R158
C11
R140 R139 C92T R153T
U11
C91
K3 K1 K2 K4
C25
Q26
R142 R167 R141 C13 R154 R143 C16
R144
C18
C17 R28 R29 R35 R36 C21 C22
R41
R46
CR44
CR45
C30
R8 CR2 R7 C88
Q6
Q5
R10 R14 CR3 CR4 CR5 CR6 R16T R15
R4
Q4
Q3
C89
R150T R20 CR9 R17 R18 C12T R149 CR7 R19 CR8 R151 R21T R22 CR10 R23
R110
R117
R114
R112
R119
R109
R134
P3
R11
R6 C10 R5
R11 R13 R12
C8 R2
C85
U1
C86
U2
C87
U3
C66 C67 C68 C65
U8
R111
Q1
CR1 R3
C9
C1
C62T C61T
C7
Q2
FB1
C6
R1
JP1
JP2
C35
CR30 CR22 CR23
C82 C81
U6
J10
AMP 1-102585-2
FRONT
1
PLACE ASSEMBLY I.D. LABEL IN THIS AREA
SEE VIEW B FOR ASSEMBLY
19
SEE
ASS

6. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.

5. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.

4. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

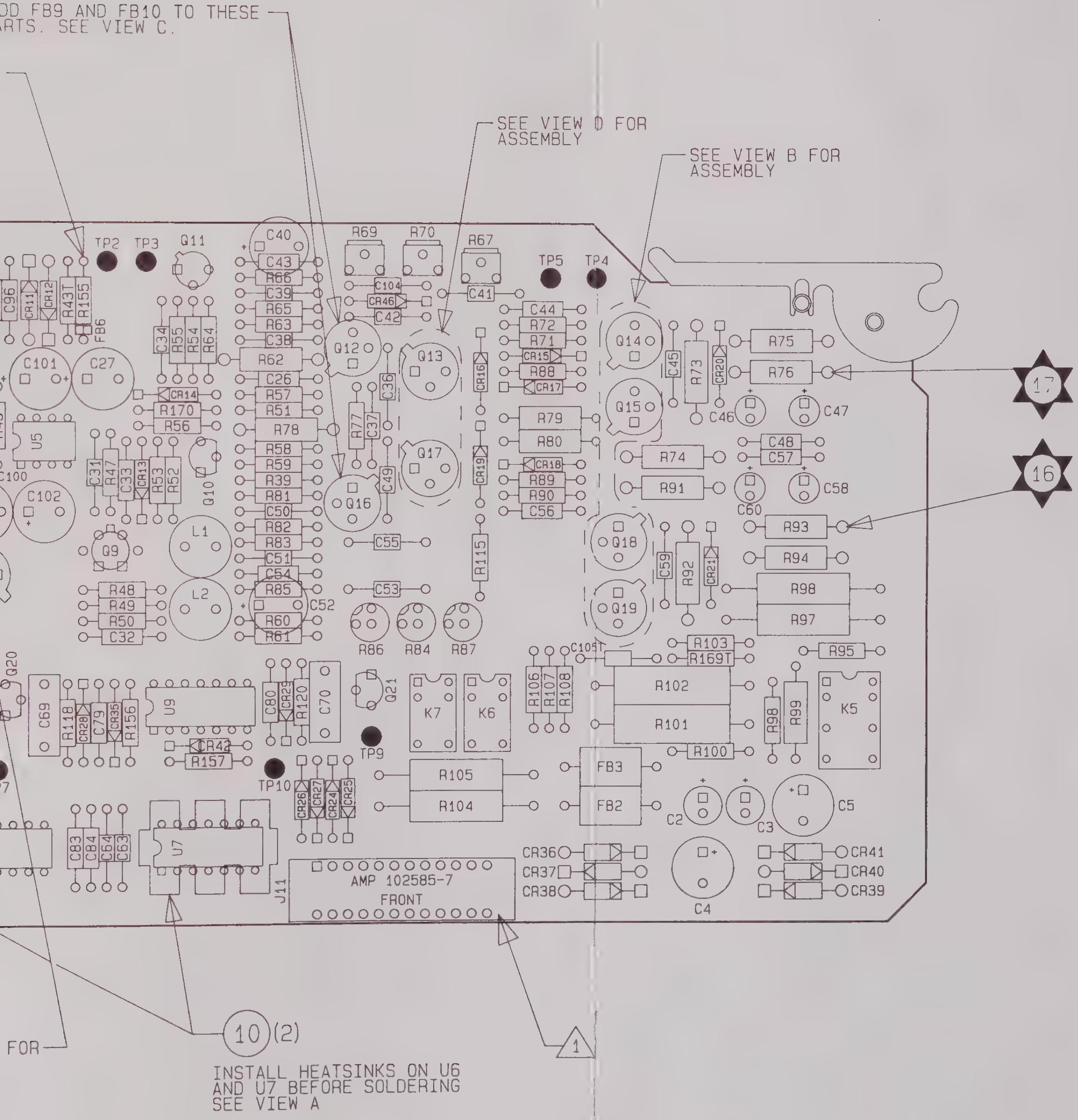
3. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

2. SEE 1104-00-3335 FOR SCHEMATIC.

△1 MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
B	ERO NO. 90-493	AT	7/30/90	J.M.
C	ECO #: 90-530	AT	9/5/90	M.S.
D	ECO NO. 90-557	A.T.L.	9/5/90	M.S.
E	ECO NO. 91-040	A.T.L.	11/5/90	M.S.
F	ECO #: 91-116	TL	2/1/91	



TP2
TP3
Q11
C40
C43
R66
C39
R65
R63
C38
R62
C26
R57
R51
R78
R58
R59
R39
R81
C50
R82
R83
C51
C54
R85
C52
R60
R61
R69
R70
R67
C104
CR46
C42
C41
TP5
TP4
C44
R72
R71
CR15
R88
CR17
R79
R80
CR18
R89
R90
C56
Q12
Q13
Q16
Q17
R77
C37
C36
C49
CR16
CR19
R115
C55
C53
R86
R84
R87
Q14
Q15
C45
R73
CR20
R75
R76
C46
C47
R74
C48
C57
R91
C60
C58
R93
R94
Q18
Q19
C59
R92
CR21
R98
R97
R103
R169T
R95
C105T
R102
R101
R100
R98
R99
K5
R106
R107
R108
K7
K6
FB3
FB2
R105
R104
C2
C3
C5
C4
CR36
CR37
CR38
CR41
CR40
CR39
AMP 102585-7
FRONT
J11
C96
CR11
CR12
R43T
R155
FB6
C101
C27
C34
R55
R54
R64
CR14
R170
R56
U5
C31
R47
C33
CR13
R53
R52
Q10
C100
C102
Q9
L1
L2
R48
R49
R50
C32
Q20
C69
R118
CR28
C79
CR35
R156
U9
CR42
R157
C80
CR29
R120
C70
Q21
TP9
TP10
CR26
CR27
CR24
CR25
C83
C84
C64
C63
U7
17
16

DD FB9 AND FB10 TO THESE
ARTS. SEE VIEW C.

SEE VIEW D FOR
ASSEMBLY

SEE VIEW B FOR
ASSEMBLY

FOR

10 (2)

INSTALL HEATSINKS ON U6
AND U7 BEFORE SOLDERING
SEE VIEW A

1

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	
DO NOT SCALE DRAWING		

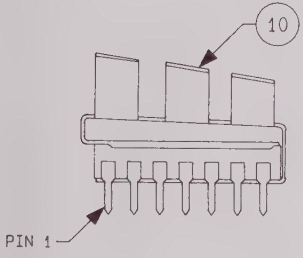
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PCA,
OUTPUT BOARD

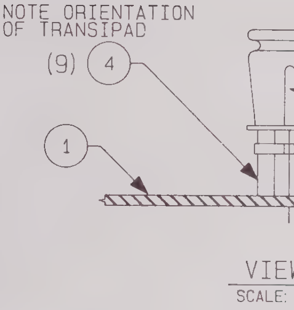
SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1101-00-3335	F

SCALE 2/1 MODEL 90 SERIES SHEET 1 OF 3

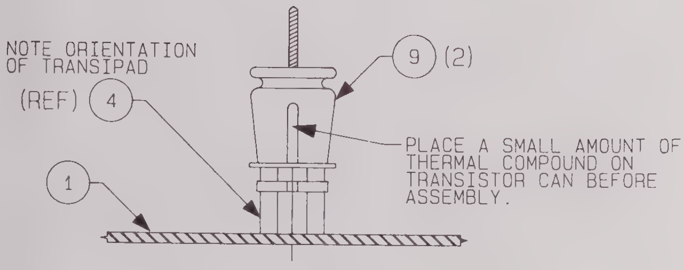
1101-00-3335 F



VIEW A
SCALE: NONE


NOTE ORIENTATION
OF TRANSIPAD
(9) 4
1

VIE
SCALE:

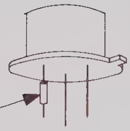

NOTE ORIENTATION
OF TRANSIPAD
(REF) 4
9 (2)
1
PLACE A SMALL AMOUNT OF
THERMAL COMPOUND ON
TRANSISTOR CAN BEFORE
ASSEMBLY.

VIEW D
SCALE: NONE

NOTE UNLESS OTHERWISE SPECIFIED

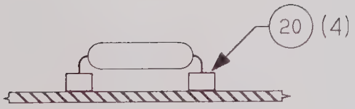
REV	ECO	BY	DATE	APP

-PLACE A SMALL AMOUNT OF THERMAL COMPOUND ON TRANSISTOR CAN BEFORE ASSEMBLY.

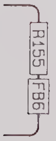


PLACE FB9 ON COLLECTOR LEAD OF Q12 AND FB10 ON COLLECTOR LEAD OF Q16

VIEW C
SCALE: NONE



VIEW E
SCALE: NONE



INSTALL FB6 ON THE BOTTOM LEAD OF R155.

VIEW F
SCALE: NONE

1101-00-3335 F

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

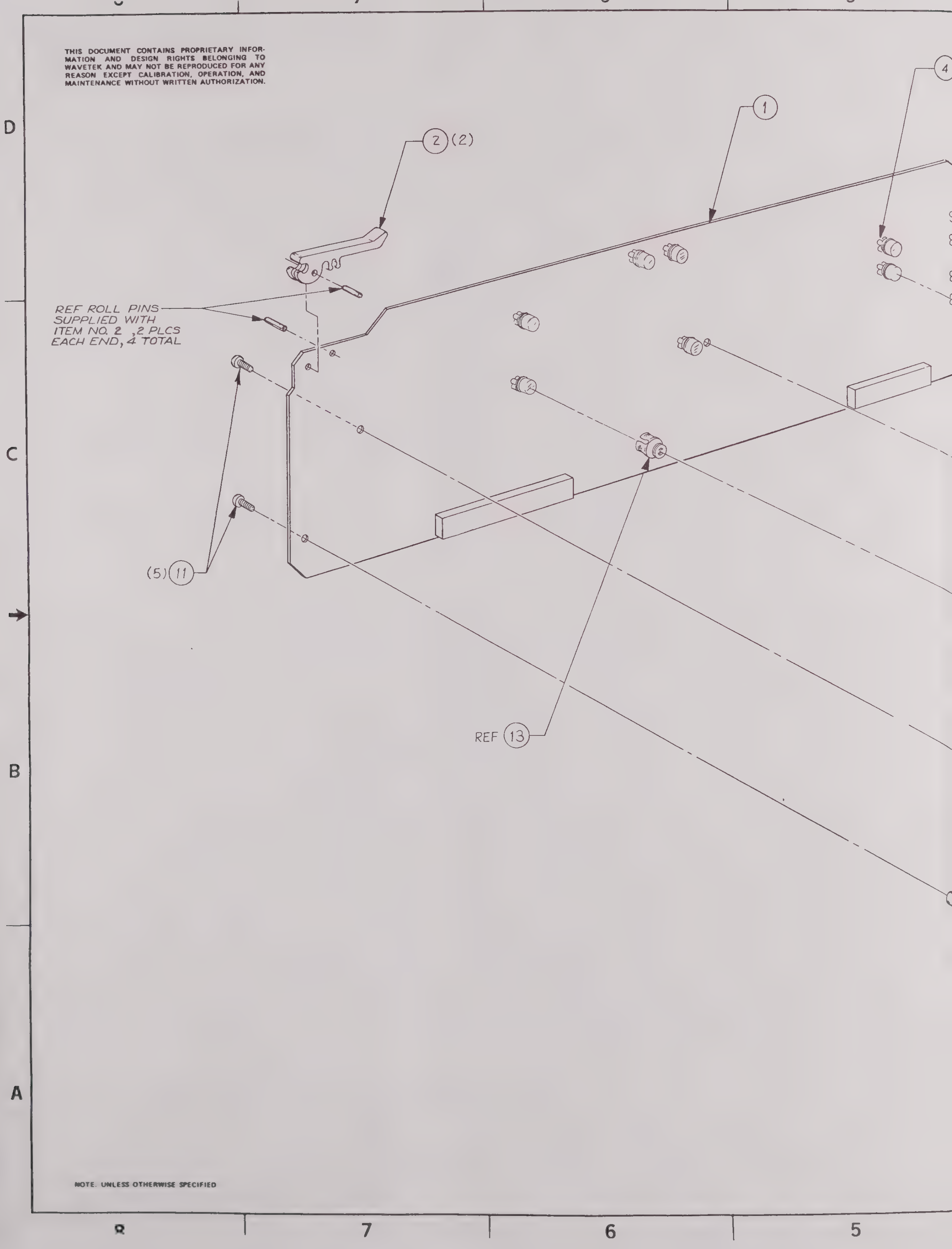
DRAWN Amy Talmadge DATE 7/90
CHECKED
PROJ. ENGR.
RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

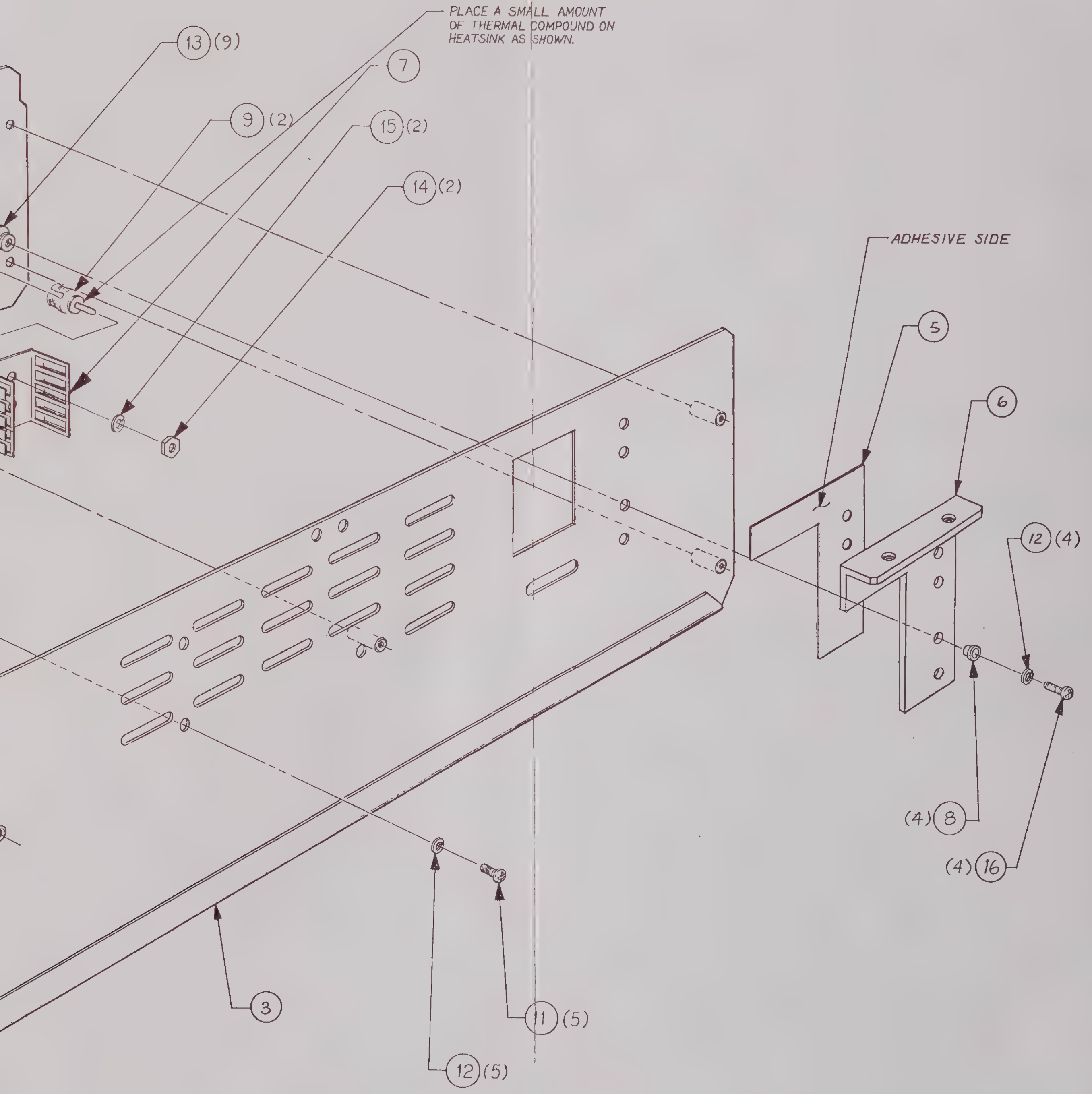
TITLE
PCA,
OUTPUT BOARD

SIZE D FSCM NO. 23338 DWG. NO. 1101-00-3335 REV F
SCALE NONE MODEL 90 SERIES SHEET 2 OF 3


D
C
B
A
4
1
2 (2)
REF ROLL PINS SUPPLIED WITH ITEM NO. 2 ,2 PLCS EACH END, 4 TOTAL
(5) 11
REF 13
8
7
6
5

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP


PLACE A SMALL AMOUNT OF THERMAL COMPOUND ON HEATSINK AS SHOWN.
13 (9)
7
9 (2)
15 (2)
14 (2)
ADHESIVE SIDE
5
6
12 (4)
(4) 8
(4) 16
3
11 (5)
12 (5)
D
C
B
A
4
3
2
1

1101-00-3335 F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.C. / A.T.	DATE 7/90	**WAVETEK** SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR	7/90	TITLE PCA, OUTPUT BOARD	
	RELEASE APPROV 7/90			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030			
	DO NOT SCALE DWG		MODEL NO. 90 SERIES	DWG NO. 1101-00-3335 REV F
	SCALE NONE		CODE IDENT 23338	SHEET 3 OF 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR46	DIODE ZENER, 1N4737 1W 7.5V 10%	1N4737A	MOT	0374-00082	1
R162 R166	RES, MF, 1/2W, 1%, 365 OHM	RN65D3650F	DALE	0588-03650	2
NONE	A/D, OUTPUT BOARD	1101-00-3335	WVTK	1101-00-3335	1
NONE	SCHEMATIC, OUTPUT BD	1104-00-3335	WVTK	1104-00-3335	1
U12	U: CURRENT AMP, 100MA	LH0002CN	NSC	120.1022	1
CR14	SL ZR 6.2V 5% 400MW (1N753A)	1N753A	ROHM	131.9620	1
3	SHIELD, OUT PUT BOARD	1400-02-5066	WVTK	1400-02-5066	1
6	HEAT SINK, OUT PUT BOARD	1400-02-5067	WVTK	1400-02-5067	1
NONE	THERMAL GASKET, OUT PUT BOARD	1400-02-5068	WVTK	1400-02-5068	1
7	HEAT SINK, MODIFICATION	1400-02-5085	WVTK	1400-02-5085	1
C53 C55	CAP, CER, 100PF, 100V, AXIAL	CAC02COG101J100A	CORNG	1500-01-0106	2
C104 C20 C21 C34 C35 C36 C37 C38 C39 C45 C49 C50 C51 C59	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	14

WAVETEK PARTS LIST
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REFERENCE DESIGNATORS	PART DESCRIPTION	O
C92T	CAP, CER, 5.1PF, 200V, AXIAL	S
C19	CAP, CER, 56PF, 100V, 5%, AXIAL	C
C71 C72 C73 C74	CAP, MICA, 910PF, 100V, 1%, RADIAL	D
C29 C30 C46 C47 C58 C60	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	N
C4 C5	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	N
C1 C2 C3	CAP, ELECT, 100MF/16V RADIAL LEAD, SP .20	N
C15 C18	CAP, ELECT, 220MF/10V	E
C11 C9	CAP, ELECT, 22MF, 25V, RADIAL	S
C69 C70	C05 CAP, MET POLY, .1MF, 100V/160V DC, .4 LS	1
C28	CAP, TANT, 100MF, 10V	1
C24 C25	CAP, TANT, 2.2MF, 25V	1
C40 C52	CAP, TANT	1

WAVETEK PARTS LIST
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C10 C103 C13 C14 C16 C17 C22 C23 C32 C33 C43 C44 C48 C54 C56 C57 C65 C66 C67 C68 C7 C76 C77 C79 C8 C80 C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C95 C96 C97 C98	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	41
C26	CAP, CER, 120PF, 100V, 5%, AXIAL	CAC02COG121J100A	CORNG	1500-01-2106	1
C62T	CAP, CER, 15PF, 100V, AXIAL	CAC02COG150J100A	CORNG	1500-01-5006	1
C75	CAP, CER, 1.5PF, 200V, AXIAL	SA102A1R5DAA	AVX	1500-01-5906	1
C6	CAP, CER, 22PF, 100V, AXIAL	CAC02COG220J100A	CORNG	1500-02-2006	1
C41 C42	CAP, CER, 220PF, 100V, AXIAL	CAC02COG221J100A	CORNG	1500-02-2106	2
C61T	CAP, CER, 27PF, 5%, COG, 100V, AXIAL	CAC02COG270J100A	CORNG	1500-02-7006	1
C63	CAP, CER, 33PF, 100V+-5%, AXIAL	CAC02COG330J100A	CORNG	1500-03-3006	1
C100T	CAP, CERAMIC, 3.9PF + .5PF, 200V AXIAL.	C114C399D2G5CA	KEMET	1500-03-9906	1
C105T C12T C31	CAP, CER, 47PF, 100V, AXIAL	CAC02COG470J100A	CORNG	1500-04-7006	3

WAVETEK PARTS LIST
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REFERENCE DESIGNATORS	PART DESCRIPTION	O
	27UF, 35V+/-10%, 0.25LS	
C101 C102 C27	CAP, TANT, 47MF, 20V	1
1	PCB, OUTPUT BOARD	1
L1 L2	INDUCTOR, 2.2 MHY, 40MA, RADIAL	1
J11	CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT	1
J10	CONN, HEADER, 40 PIN, RECPT, 2X20, .1 CTR PCMT	1
TP3 TP5	TEST POINT, BLK, PC	T
TP1 TP10 TP11 TP12 TP2 TP4 TP6 TP7 TP8 TP9	TEST POINT, RED, PC	T
P35	CONN, SUB MIN	2
20	SPACER, COMP, MUNTING, .085OD, .032ID, .300LG	9
2	PC BD EJECTOR	8
4	TRANSIPAD	5
9	HEATSINK	2

WAVETEK PARTS LIST
TITLE
PCA, OUTPUT BOARD

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

-PART-NO	MFGR	WAVETEK NO.	QTY/PT
DAA	AVX	1500-05-1906	1
60J100A	CORNG	1500-05-6000	1
	ARCO	1500-19-1101	4
	NIC	1500-31-0002	6
V10X12.5	NIC	1500-31-0102	2
V6.3X11	NIC	1500-31-0111	3
1	PANAS	1500-32-2001	2
RM6X7LL	UNCON	1500-32-2002	2
D	MALRY	1500-41-0434	2
D10EE4	SPRAG	1500-71-0711	1
D25AA2	SPRAG	1500-72-2502	2
D35FE4	SPRAG	1500-72-7602	2

ASSEMBLY NO. 1100-00-3335 REV R

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-PART-NO	MFGR	WAVETEK NO.	QTY/PT
D20PE4	SPRAG	1500-74-7601	3
335	WVTK	1700-00-3335	1
J	TOKO	1800-00-0046	2
	AMP	2100-02-0255	1
2	AMP	2100-02-0256	1
-00	COMPO	2100-04-0054	2
-02	COMPO	2100-04-0055	10
	AMPH	2100-07-0011	1
	BIVAR	2800-04-0024	4
	BRIT	2800-07-0032	2
	BIVAR	2800-11-0004	11
	WAKE	2800-11-0012	2

ASSEMBLY NO. 1100-00-3335 REV R

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
8	WASHER	5607-150	SESTM	2800-11-0015	4
13	HEATSINK, TO5, EPOXY INS	260-4T5E	WAKE	2800-11-0031	9
10	HEATSINK, 14-16 PIN DIP, ALUM, BLK AN, CLIPON	5802B	AAVID	2800-11-0034	2
14	NUT, HEX, 6-32, Z	MS35649-264	COML	2800-14-6100	2
11	SCREW, 4-40X3/16, PHP, NYLOK PATCH	4-40 X 3/16	CMRCL	2800-23-4103	10
12	WASHER, LOCK REG, S/S #4	MS 35338-135	CMRCL	2800-45-4000	9
15	WASHER, LOCK, REG S/S #6	MS 35338-136	CMRCL	2800-45-6000	2
16	SCREW, 4-40X3/8 PHP, NYLOK PATCH, Z	4-40 X 3/8 PH, SL	CMRCL	2800-56-9106	4
FB6	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	1
FB1 FB2 FB3	BALUN CORE, FERRITE, 680 OHMS	2943666671	FARIT	3100-00-0017	3
FB10 FB9	FERRITE BEAD	2673004701	FRITE	3100-00-0020	2
K5	RELAY, 2 FORMC, 5V, DIP 14	DF2E-DC5V	AROMT	4500-00-0033	1

WAVETEK PARTS LIST

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
K1 K2 K3 K4 K6 K7	RELAY, 1 FORMC, 5V, .312H, .296W	HD1E-M-DC5V	AROMT	4500-00-0034	6
R84 R86 R87	POT, TRIM, 100	3329H-1-101	BOURN	4600-01-0100	3
R67 R70	POT, 1 TURN, SIDE TRIM, 1/4" DIA, 100ohm	3329W-1-101	BOURN	4601-01-0101	2
R69	POT, 1 TURN, SIDE TRIM, 1/4" DIA, 500 OHM	3329W-1-501	BOURN	4601-01-0500	1
R25	POT, SIDE TRIM. 20T, 2K	68XR2K	BECK	4609-90-0010	1
R146	POT, SIDE TRIM, 20T, 20K	68XR20K	BECK	4609-90-0011	1
R158	POT, SIDE TRIM, 20T, 500	68XR500	BECK	4609-90-0014	1
R9	POT, SIDE TRIM, 20T, 100	68XR100	BECK	4609-90-0017	1
R73 R74 R75 R76 R91 R92 R93 R94	RES, C, 1/2W, 5%, 10	RC-1/2-10J	STKPL	4700-25-0100	8
NONE NONE1	RES, C, 1/2W, 5%, 1K	RC-1/2-102J	STKPL	4700-25-1001	2
R11 R13	RES, C, 1/2W, 5%, 220	RC-1/2-221J	STKPL	4700-25-2200	2
R12	RES, C, 1/2W, 5%, 620	RC-1/2-621J	STKPL	4700-25-6200	1
R116	RES, MF, 1/8W, .1%, 1K	RN55E-1001B	MEPCO	4701-02-1001	1
R115	RES, MF, 1/8W, .1%, 2K	RN55E-2001B	MEPCO	4701-02-2001	1
R1 R145 R17 R33 R34 R64 R82	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	7

WAVETEK PARTS LIST

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PCA, OUTPUT BOARD

ASSEMBLY NO. 1100-00-3335 REV R

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REMOVE ALL BURRS
AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN | DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
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OUTPUT BOARD

SIZE D | FSCM NO. 23338 | DWG. NO. 1100-00-3335 | REV R

SCALE | MODEL 95 | SHEET 1 OF 2

D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R109 R111 R113 R132 R136 R27 R4 R81	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	8
R119 R128 R141 R144 R156 R157 R26	RES,MF,1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	7
R118 R120	RES,MF,1/4W,10M,1%	5053YD10M000F	MEPCO	4701-03-1005	2
R154 R35 R36 R71 R72 R88 R89 R90	RES,MF,1/8W,1%,10	5043ED10R100F	MEPCO	4701-03-1009	8
R6	RES,MF,1/8W,1%,1.21K	RN55D-1211F	TRW	4701-03-1211	1
R106 R107 R108	RES,MFLM,1/8W,1%,12.1	5033RD12R1F	MEPCO	4701-03-1219	3
R14 R63	RES,MF,1/8W,1%,1.5K	RN55D-1501F	TRW	4701-03-1501	2
R170	RES,MF,1/8W,1%,15K	RN55D-1502F	TRW	4701-03-1502	1
R131	RES,MF,1/8W,1%,16.5K	RN55D-1652F	TRW	4701-03-1652	1
R15	RES,MF,1/8W,1%,1.78K	RN55D-1781F	TRW	4701-03-1781	1
R121 R122 R124 R125	RES,MFLM,1/8W,1%,17.8K	5033RD1782F	MEPCO	4701-03-1782	4
R32	RES,MF,1/8W,1%,200	RN55D-2000F	TRW	4701-03-2000	1
R2 R3	RES,MF,1/8W,1%,2K	RN55D-2001F	TRW	4701-03-2001	2
R137 R143	RES,MF,1/8W,1%,20K	RN55D-2002F	TRW	4701-03-2002	2

WAVETEK
PARTS LIST
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REFERENCE DESIGNATORS	PART DESCRIPTION
R142 R148 R38T	RES,MF,1.8W,1%,46.4
R100 R103 R7	RES,MF,1/8W,1%,4.75
R133	RES,MF,1/8W,1%,47.5
R139 R140 R152T R153T R30 R41 R45 R47 R51 R52 R53 R60 R61	RES,MF,1/8,1%,499
R130 R135 R95	RES,MF,1/8W,1%,4.99
R127	RES,MF,1/8W,1%,499K
R48 R49 R8	RES,MF,1/8W,1%,49.9
R150T R42T	RES,MF,1/8W,1%,576
R16T	RES,MF,1/8W,1%,59
R123 R126	RES,MF,1/8W,1%,6.19
R169T	RES,MF,1/8W,1%,61.9
R160 R164 R46	RES,MF,1/8W,1%,681
R161 R165 R37 R44 R5	RES,MF,1/8W,1%,68.1
R29 R56 R57	RES,MFLM,1/8W,1%,75
R99	RES,MFLM,1/4W,.1%,2

WAVETEK
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PCA, OUTPUT BOARD

C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R155	RES,MF,1/8W,1%,21.5	RN55D-21R5F	TRW	4701-03-2159	1
R147	RES,MF,1/8W,1%,2.21K	RN55D-2211F	TRW	4701-03-2211	1
R77	RES,MF,1/8W,1%,23.7K	RN55D-2372F	TRW	4701-03-2372	1
R54	RES,MF,1/8W,1%,249	RN55D-2490F	TRW	4701-03-2490	1
R110 R112 R114 R117 R50	RES,MF,1/8W,1%,2.49K	RN55D-2491F	TRW	4701-03-2491	5
R167	RES,MF,1/8W,1%,24.9K	RN55D-2492F	TRW	4701-03-2492	1
R129	RES,MF,1/8W,1%,28.7K	RN55D-2872F	TRW	4701-03-2872	1
R39	RESISTOR, METAL FILM, 1/8W, 1%, 294 OHM.	5043ED294R0F	MEPCO	4701-03-2940	1
R175T	RES,MF,1/8W,1%,301K	RN55D-3013F	TRW	4701-03-3013	1
R43T	RES,MF,1/8W,1%,316	RN55D-3160F	TRW	4701-03-3160	1
R19 R20 R21T R23 R28 R31	RES,MF,1/8W,1%,332	RN55D-3320F	TRW	4701-03-3320	6
R10 R138 R159 R163 R55 R65 R83	RES,MF,1/8W,1%,33.2	RN55D-33R2F	TRW	4701-03-3329	7
R169	RES,MF,1/8W,1%,35.7K	RN55D-3572F	TRW	4701-03-3572	1
R66 R85	RES,MF,1/8W,1%,39.2	RN55D-39R2F	TRW	4701-03-3929	2
R98	RES,MF,1/8W,1%,41.2K	RN55D-4122F	TRW	4701-03-4122	1
R58 R59	RES,MF,1/8W,1%,464	RN55D-4640F	TRW	4701-03-4640	2

WAVETEK
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REFERENCE DESIGNATORS	PART DESCRIPTION
R101 R102	RES,MFLM,1W,.1%,61.
R79 R80	RES,MF,1/4W(1/2W@70C),1%,1.69K ohm
R104 R105 R96 R97	RES, MF,1W,.25%, T2 100
RN1	RES NETWORK 1K 2W 16PIN DIP
JP1 R134	RES, 0 OHM JUMPER
CR34	DIODE, ZENOR, 5.1V, 500MW, GIB, IN751A
CR45	DIODE, ZENER, 6.8V
CR10 CR13 CR15 CR16 CR17 CR18 CR19 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR30 CR31 CR32 CR33 CR35 CR42 CR43 CR44 CR7 CR8 CR9	DIODE, HIGH CONDUCTANCE, ULTRA FAST
CR11 CR12 CR36 CR37 CR38 CR39 CR40 CR41	DIODE,1N4002 GEN PURPOSE RECT. 100V,
CR1 CR2 CR3 CR4 CR5 CR6	DIODE 5082-2811 SCHOTTKY,15V,20MA
Q26	TRANS 2N2219A NPN GENERAL PURPOSE TO-

WAVETEK
PARTS LIST
TITLE
PCA, OUTPUT BOARD

B

A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
D-46R4F	TRW	4701-03-4649	3
D-4751F	TRW	4701-03-4751	3
D-4752F	TRW	4701-03-4752	1
D-4990F	TRW	4701-03-4990	13
D-4991F	TRW	4701-03-4991	3
D-4993F	TRW	4701-03-4993	1
D-49R9F	CORNG	4701-03-4999	3
D-5760F	TRW	4701-03-5760	2
D-59R0F	TRW	4701-03-5909	1
D-6191F	TRW	4701-03-6191	2
D-61R9F	TRW	4701-03-6199	1
D-6810F	TRW	4701-03-6810	3
D-68R1F	TRW	4701-03-6819	5
RD75R0F	MEPCO	4701-03-7509	3
RE2490B	MEPCO	4701-12-2490	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q11	TRANS, SILICON, PLANAR, EPITAXIAL, NPN, TO-18	2N2369A	MOT	4901-02-3691	1
Q27 Q28	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	2
Q1 Q22 Q24 Q5	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	4
Q14 Q15	TRANS	2N3866	MOT	4901-03-8660	2
Q2 Q20 Q4	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	3
Q10 Q21 Q3	TRANS, GENERAL PURPOSE, PNP, TO-92	PN4122	NSC	4901-04-1220	3
Q18 Q19	TRANS	2N5160-18	MOT	4901-05-1600	2
Q16	TRANS 2N5583 PNP HIGH FREQ TO-39	2N5583	MOT	4901-05-5830	1
Q6	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	1
Q12 Q23 Q25	TRANS, NPN, HIGH FREQ	2N5943	MOT	4901-05-9430	3
Q13	TRANS	4902-02-5730	WVTK	4902-02-5730	1
Q17	TRANS	4902-02-5740	WVTK	4902-02-5740	1
U14 U9	OP AMP, QUAD BIMOS MOS/FET INPUT	TL084CN	TI	7000-00-8400	2

WAVETEK
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PCA, OUTPUT BOARD

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-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RE61R9B	MEPCO	4701-32-6199	2
1K691%100PPM	RCD	4701-33-1691	2
RC100R0C	MEPCO	4701-38-1000	4
R-001-102	BOURN	4770-00-0019	1
T68G	ROHM	4799-00-0087	2
1A	FAIR	4801-01-0751	1
4A	MOT	4801-01-0754	1
82	FAIR	4801-01-5282	28
02	FAIR	4801-02-0001	8
-2811	HP	4809-02-2811	6
19A	NSC	4901-02-2191	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U11 U5	WIDWBAND HIGH SLEW RATE OP AMP	CLC404AJP	COMLR	7000-04-0410	2
Q9	TRANS, MONO, DUAL, NPN	LS312-52	LINSY	7000-08-1200	1
U4	MULTIPLIER, ANALOG, WIDEBAND	AD834JN	ANDEV	7000-08-3410	1
U6 U7	OP AMP, WIDEBND, HI SL RTE, HI OUT	HA3-2542-5	HARIS	7000-25-4200	2
U10	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	1
U8	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	1
U1	DECODER/DEMUX, 3 TO 8 LINE	SN74ALS138N	TI	8007-41-3800	1
U2 U3	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	2

WAVETEK
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PCA, OUTPUT BOARD

ASSEMBLY NO. 1100-00-3335 REV R

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REMOVE ALL BURRS
AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

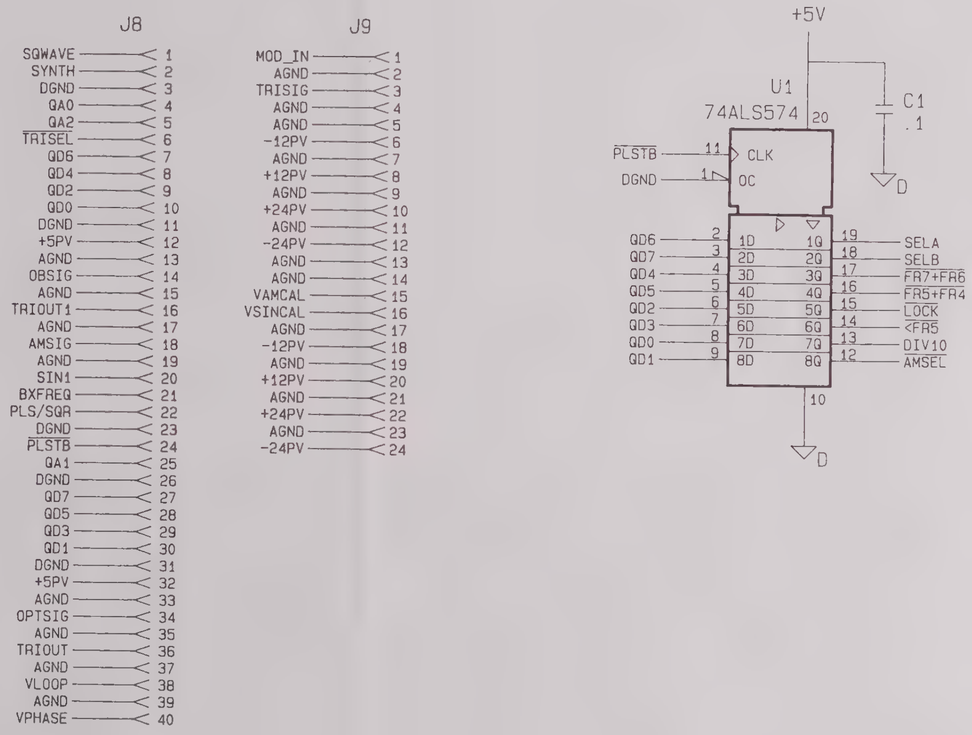
DRAWN | DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
OUTPUT BOARD

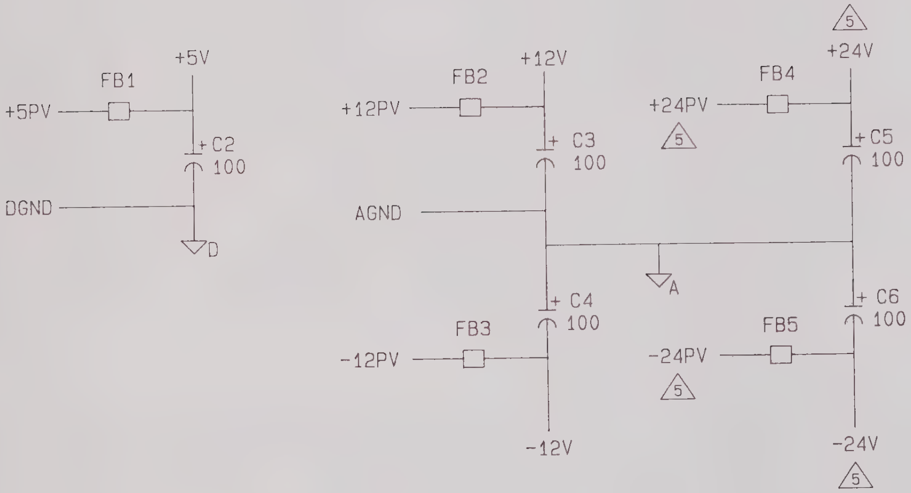
SIZE D | FSCM NO. 23338 | DWG. NO. 1100-00-3335 | REV R
SCALE | MODEL 95 | SHEET 2 OF 2


J8
SQWAVE 1
SYNTH 2
DGND 3
QA0 4
QA2 5
TRISEL 6
QD6 7
QD4 8
QD2 9
QD0 10
DGND 11
+5PV 12
AGND 13
OBSIG 14
AGND 15
TRIOUT1 16
AGND 17
AMSIG 18
AGND 19
SIN1 20
BXFREQ 21
PLS/SQR 22
DGND 23
PLSTB 24
QA1 25
DGND 26
QD7 27
QD5 28
QD3 29
QD1 30
DGND 31
+5PV 32
AGND 33
OPTSIG 34
AGND 35
TRIOUT 36
AGND 37
VLOOP 38
AGND 39
VPHASE 40
J9
MOD_IN 1
AGND 2
TRISIG 3
AGND 4
AGND 5
-12PV 6
AGND 7
+12PV 8
AGND 9
+24PV 10
AGND 11
-24PV 12
AGND 13
AGND 14
VAMCAL 15
VSINCAL 16
AGND 17
-12PV 18
AGND 19
+12PV 20
AGND 21
+24PV 22
AGND 23
-24PV 24
+5V
U1
74ALS574
20
C1
.1
D
PLSTB 11 CLK
DGND 1 OC
QD6 2 1D 1Q 19 SELA
QD7 3 2D 2Q 18 SELB
QD4 4 3D 3Q 17 FR7+FR6
QD5 5 4D 4Q 16 FR5+FR4
QD2 6 5D 5Q 15 LOCK
QD3 7 6D 6Q 14 <FR5
QD0 8 7D 7Q 13 DIV10
QD1 9 8D 8Q 12 AMSEL
10
D

6. * = MATCHED DIODE SET 4898-00-0015.
5. ⏚A = ANALOG GROUND SYMBOL.
4. ⏚D = DIGITAL GROUND SYMBOL.
3. ALL CAPACITORS ARE IN MICROFARADS (uF).
2. ALL RESISTORS ARE IN OHMS, 1/8W, 1%, MF.
1. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ECO 90-584 CLS I FROM: 1104-00-3341	KA	7 2 90	JM 10/9/90
B	ECO# 91-121	KA	2 7 91	HN



+5PV
FB1
+5V
C2
100
DGND
D
+12PV
FB2
+12V
C3
100
AGND
A
C4
100
FB3
-12PV
-12V
5
+24V
+24PV
5
FB4
C5
100
C6
100
-24PV
5
FB5
-24V
5

CAD JOB #: B063C

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN A.C.T. DATE 7/90

CHECKED JM 7/2/90

PROJ. ENGR

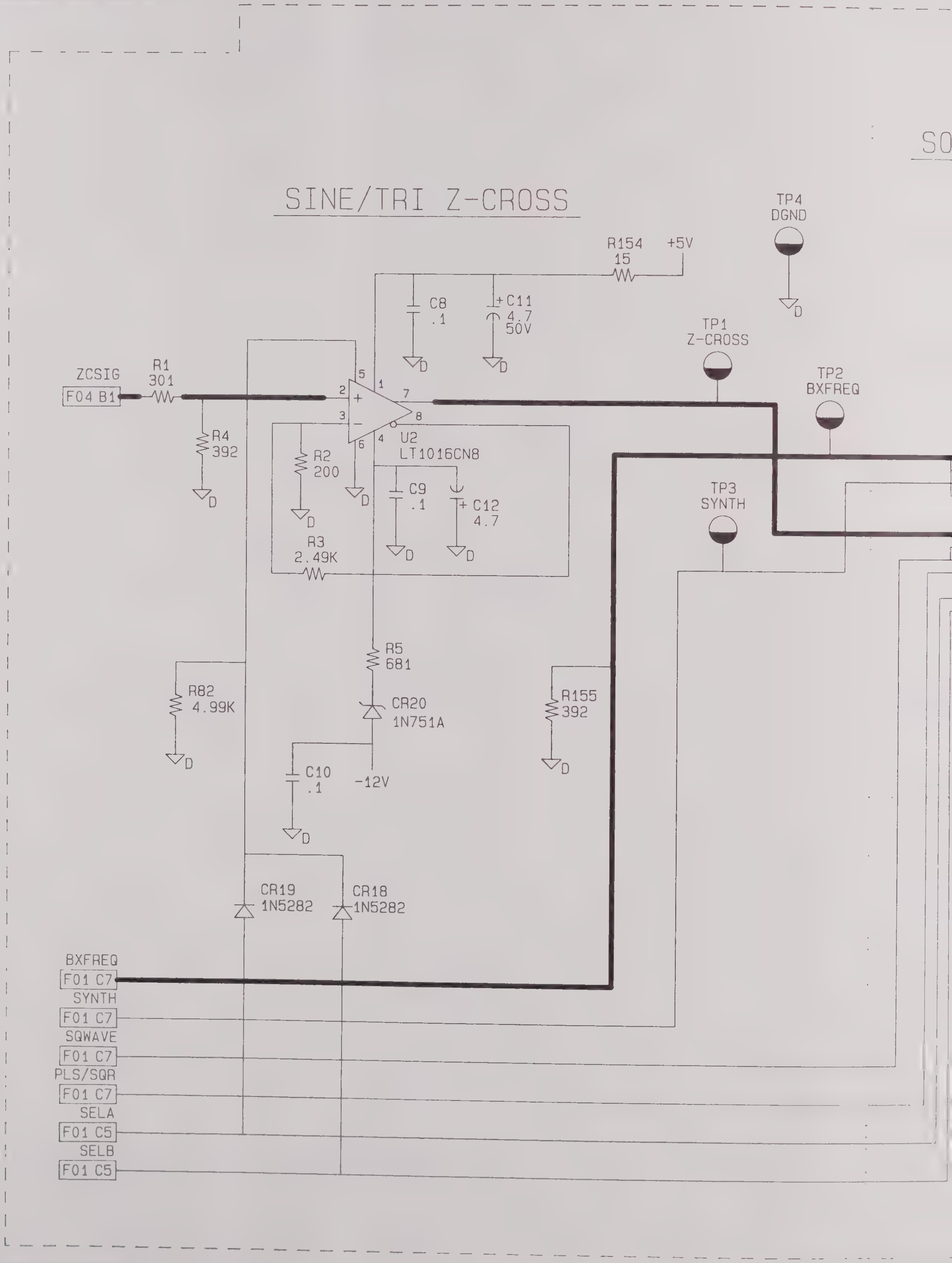
RELEASE APPROV. JM 10/9/90

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

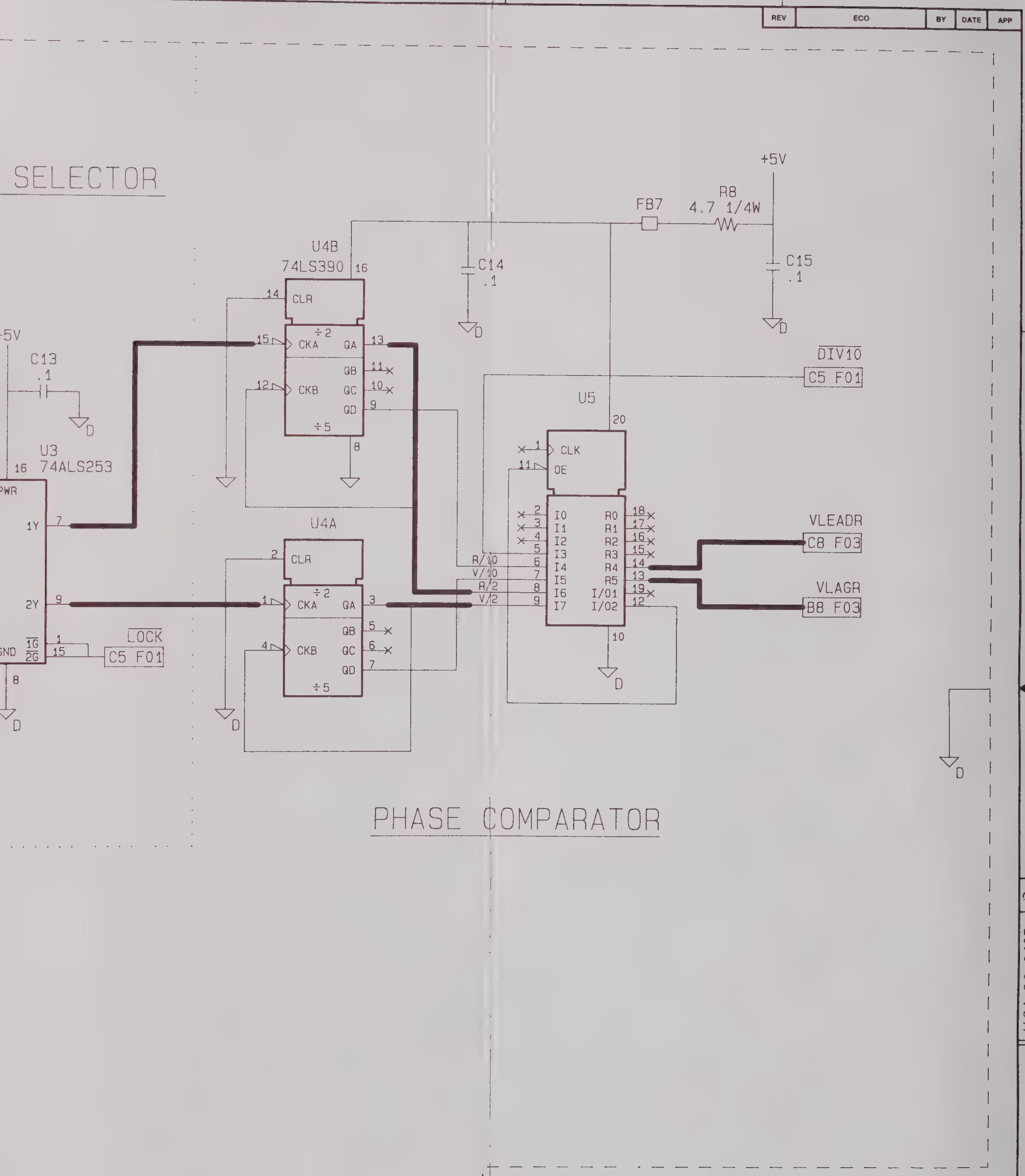
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
PHASE LOCK LOOP

SIZE D
FSCM NO. 23338
DWG. NO. 1104-00-3437
REV B
SCALE NONE
MODEL 90 SERIES
SHEET 1 OF 6


SINE/TRI Z-CROSS
SO
R154
15
+5V
TP4
DGND
C8
.1
C11
4.7
50V
TP1
Z-CROSS
ZCSIG
F04 B1
R1
301
R4
392
U2
LT1016CN8
TP2
BXFREQ
R2
200
C9
.1
C12
4.7
TP3
SYNTH
R3
2.49K
R5
681
CR20
1N751A
R82
4.99K
R155
392
C10
.1
-12V
CR19
1N5282
CR18
1N5282
BXFREQ
F01 C7
SYNTH
F01 C7
SQWAVE
F01 C7
PLS/SQR
F01 C7
SELA
F01 C5
SELB
F01 C5
D

NOTE UNLESS OTHERWISE SPECIFIED


REV
ECO
BY
DATE
APP
SELECTOR
+5V
FB7
R8
4.7 1/4W
C14
.1
C15
.1
U4B
74LS390
16
14 CLR
15 CKA ÷2 QA 13
QB 11
12 CKB QC 10
QD 9
÷5
8
-5V
C13
.1
U3
74ALS253
16
PWR
1Y 7
2Y 9
1G 1
2G 15
GND
8
LOCK
C5 F01
DIV10
C5 F01
U5
20
1 CLK
11 OE
2 I0 R0 18
3 I1 R1 17
4 I2 R2 16
5 I3 R3 15
6 I4 R4 14
7 I5 R5 13
8 I6 I/01 19
9 I7 I/02 12
10
R/10
V/10
R/2
V/2
U4A
2 CLR
1 CKA ÷2 QA 3
QB 5
4 CKB QC 6
QD 7
÷5
VLEADR
C8 F03
VLAGR
B8 F03
D
PHASE COMPARATOR
1104-00-3437 B

CAD JOB #: B063C

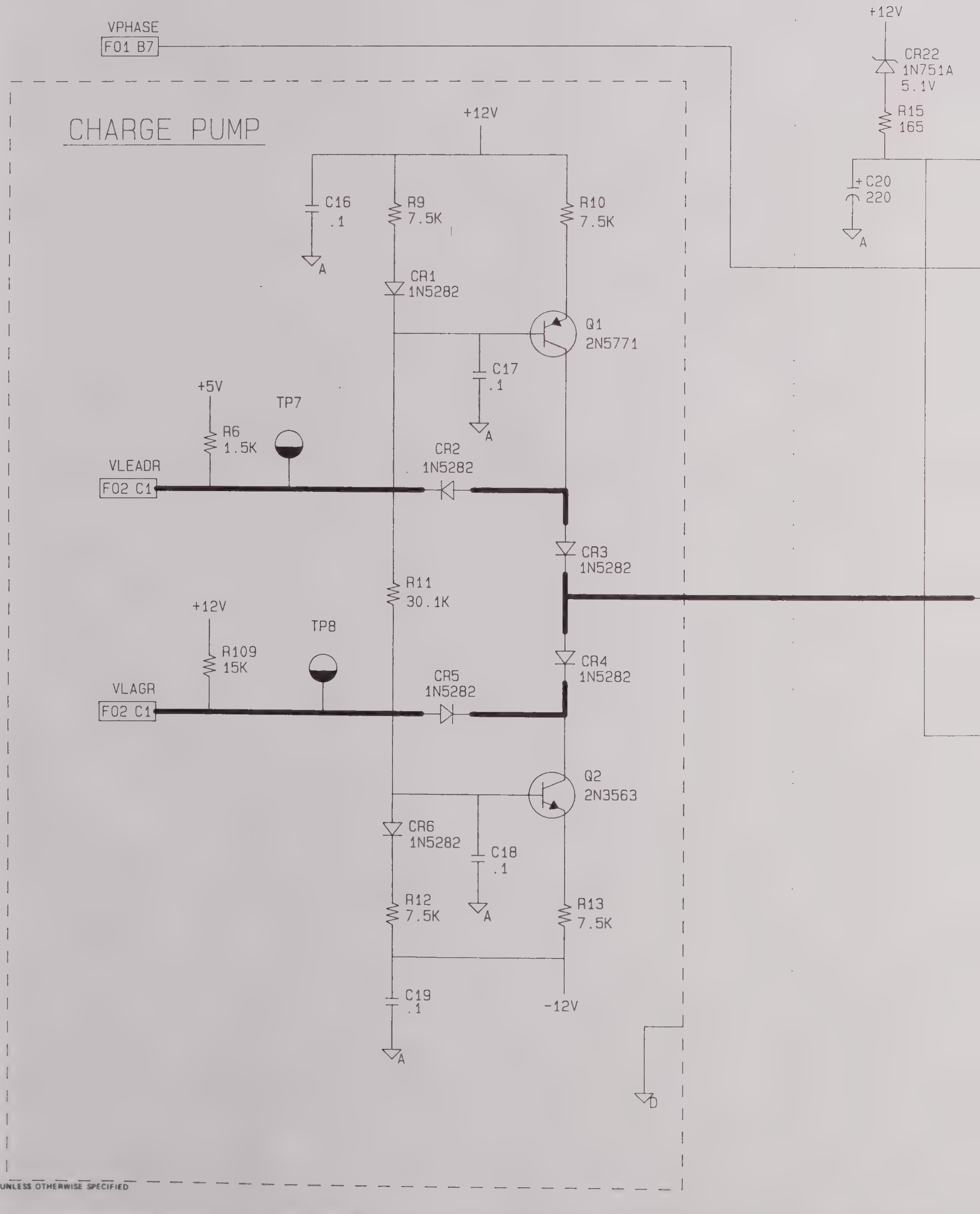
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 7/90
MATERIAL	CHECKED JM	7/2/90
	PROJ. ENGR.	
FINISH WAVETEK PROCESS	RELEASE APPROV	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, PHASE LOCK LOOP

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3437	B

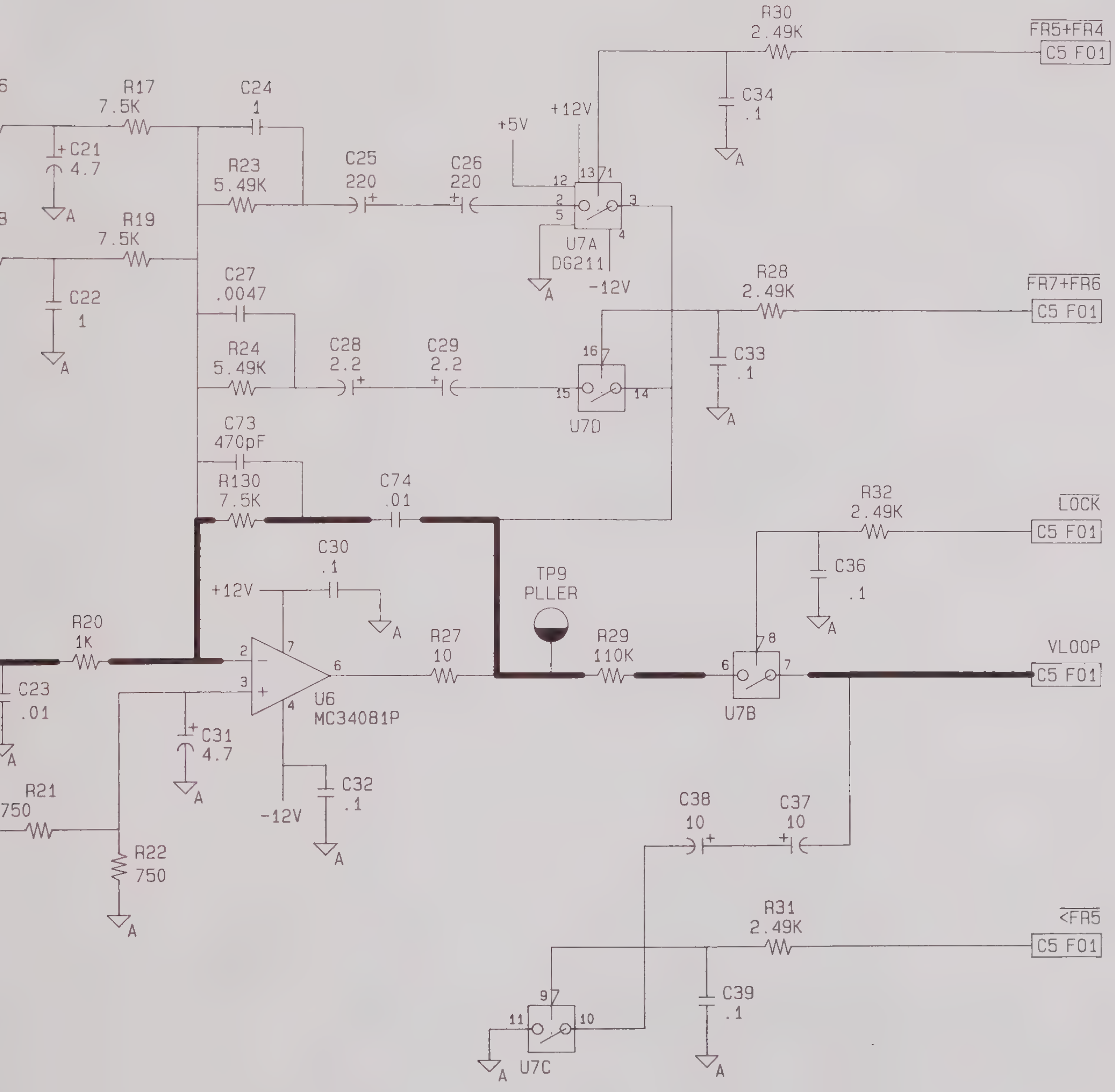
SCALE NONE MODEL 90 SERIES SHEET 2 OF 6


VPHASE
F01 B7
CHARGE PUMP
+12V
C16
.1
A
R9
7.5K
R10
7.5K
CR1
1N5282
Q1
2N5771
C17
.1
A
+5V
TP7
R6
1.5K
VLEADR
F02 C1
CR2
1N5282
CR3
1N5282
R11
30.1K
+12V
TP8
R109
15K
VLAGR
F02 C1
CR5
1N5282
CR4
1N5282
Q2
2N3563
CR6
1N5282
C18
.1
A
R12
7.5K
R13
7.5K
C19
.1
A
-12V
D
+12V
CR22
1N751A
5.1V
R15
165
+ C20
220
A
8
7
6
5
D
C
B
A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

LOCK LOOP FILTER



R17
7.5K
C24
1
C21
4.7
R23
5.49K
C25
220
C26
220
R19
7.5K
C22
1
+5V
+12V
U7A
DG211
-12V
R30
2.49K
C34
.1
FR5+FR4
C5 F01
C27
.0047
R24
5.49K
C28
2.2
C29
2.2
U7D
R28
2.49K
C33
.1
FR7+FR6
C5 F01
C73
470pF
R130
7.5K
C74
.01
C30
.1
+12V
TP9
PLLER
R32
2.49K
C36
.1
LOCK
C5 F01
R20
1K
C23
.01
U6
MC34081P
R27
10
R29
110K
U7B
VLOOP
C5 F01
C31
4.7
C32
.1
-12V
R21
750
R22
750
C38
10
C37
10
R31
2.49K
C39
.1
<FR5
C5 F01
U7C
A

CAD JOB #: B063C

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

		DATE
DRAWN	A.C.T.	7/90
CHECKED	JM	7/2/90
PROJ. ENGR.		
RELEASE APPROV.		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

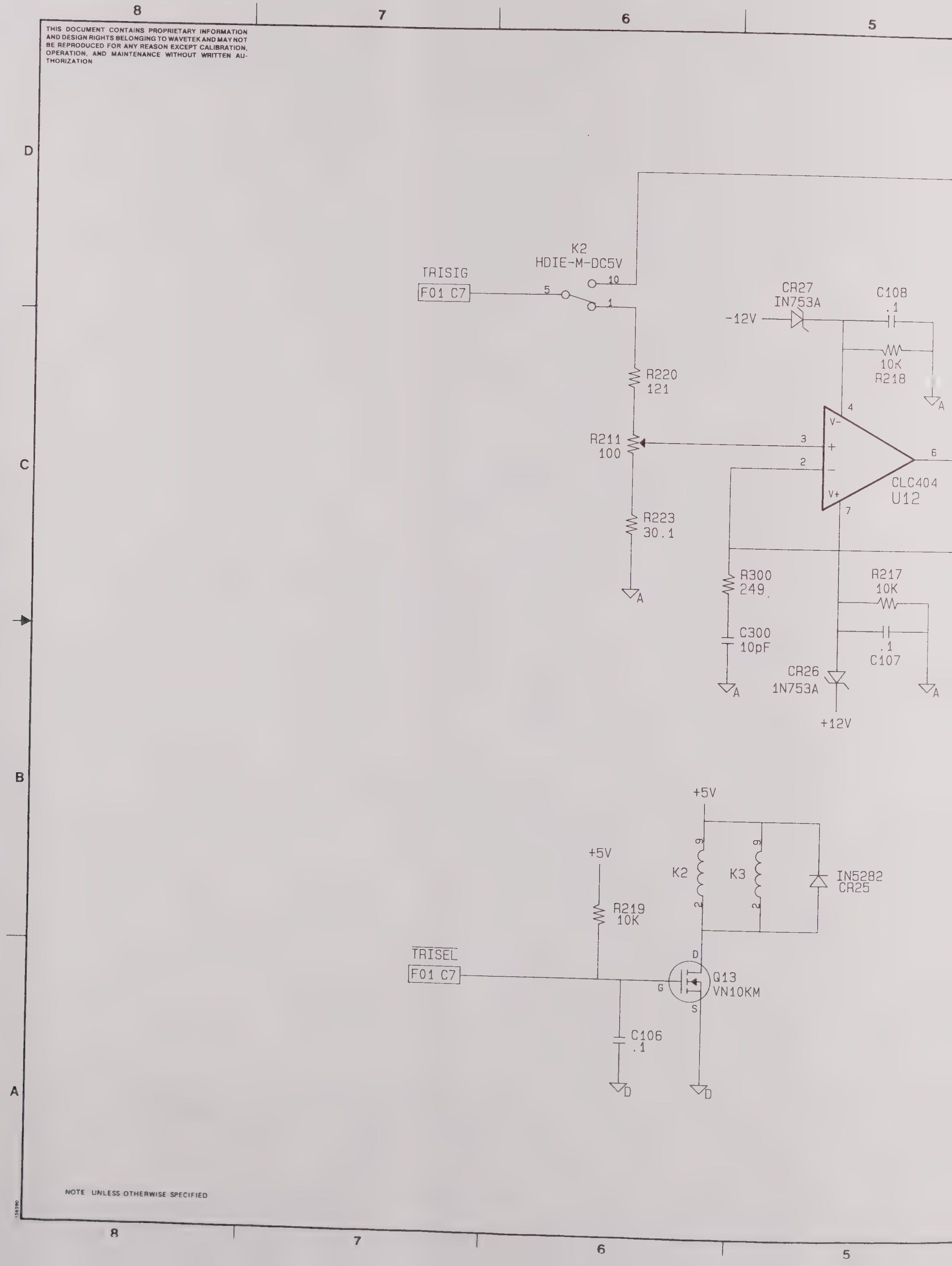
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
PHASE LOCK LOOP

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3437	B

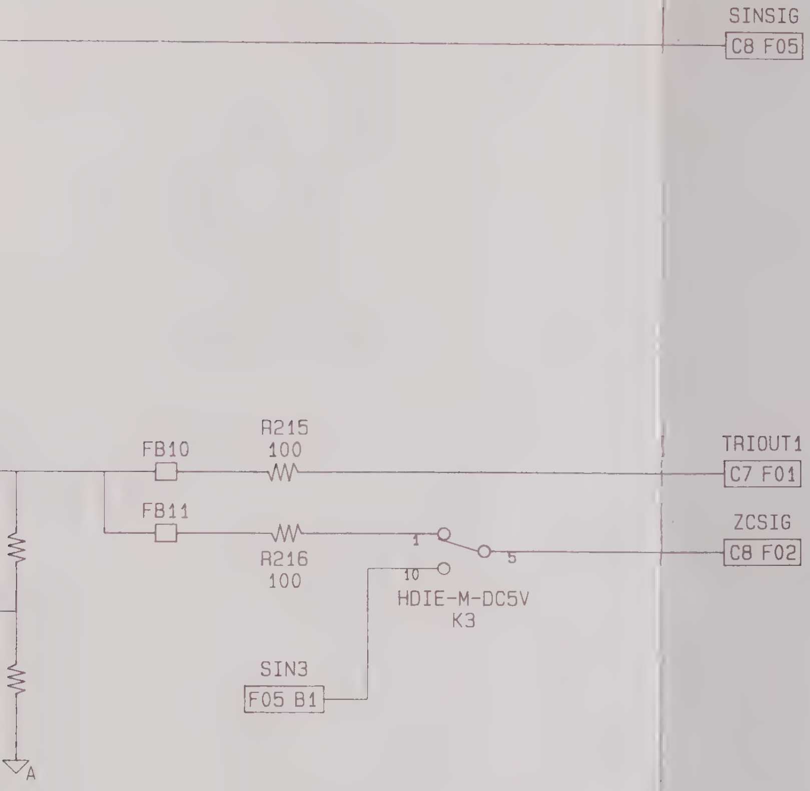
SCALE NONE MODEL 90 SERIES SHEET 3 OF 6

1104-00-3437 B


8
7
6
5
D
C
B
A
K2
HDIE-M-DC5V
TRISIG
F01 C7
5
10
1
CR27
1N753A
C108
.1
-12V
10K
R218
A
R220
121
R211
100
3
2
4
6
V-
V+
7
CLC404
U12
R223
30.1
A
R300
249
R217
10K
C300
10pF
.1
C107
CR26
1N753A
+12V
+5V
K2
K3
IN5282
CR25
+5V
R219
10K
TRISEL
F01 C7
D
G
S
Q13
VN10KM
C106
.1
D

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

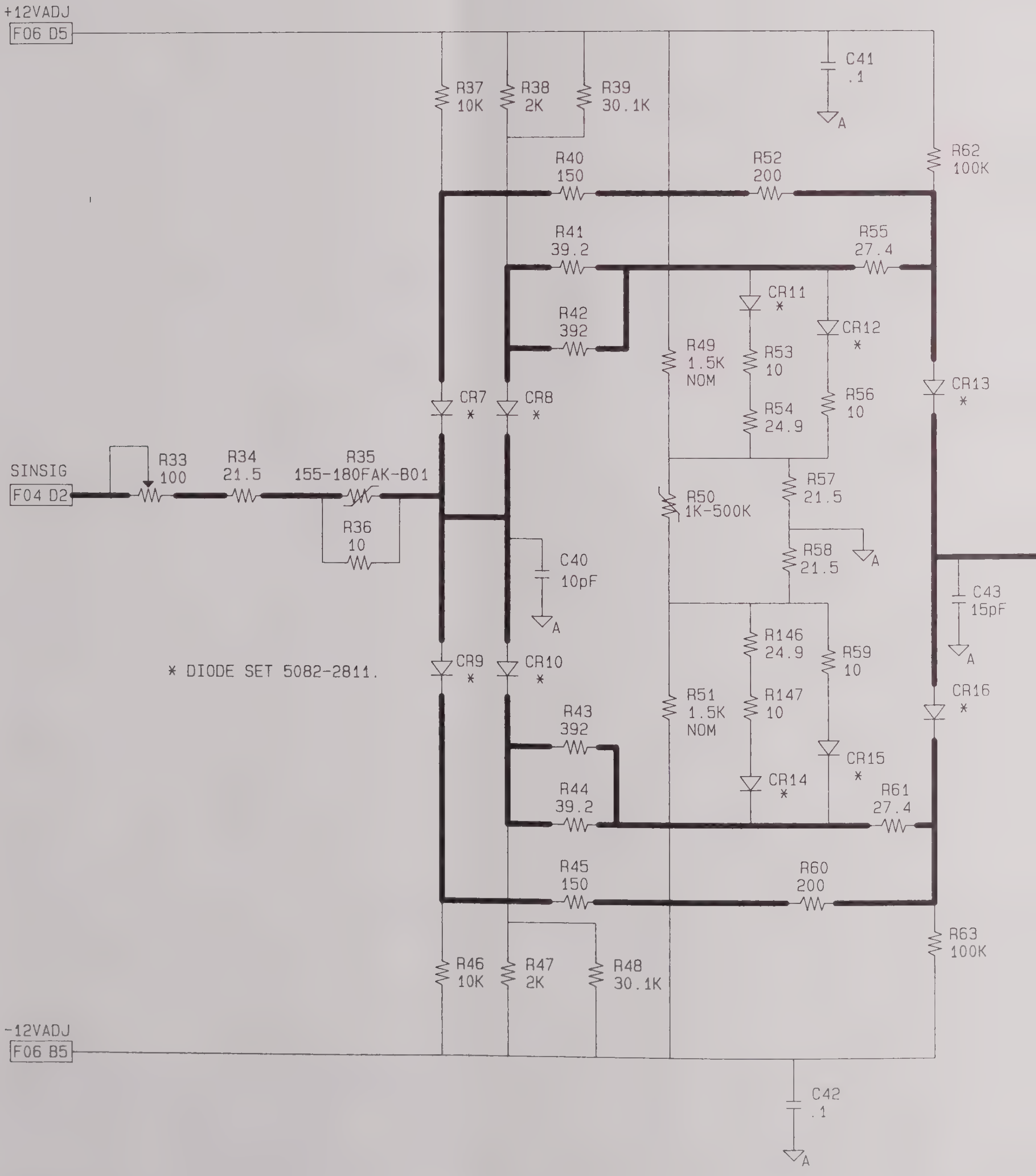

SINSIG
C8 F05
FB10
R215
100
TRIOUT1
C7 F01
FB11
ZCSIG
1
5
C8 F02
R216
100
10
HDIE-M-DC5V
K3
SIN3
F05 B1
A

1104-00-3437 | B

CAD JOB #: B063C

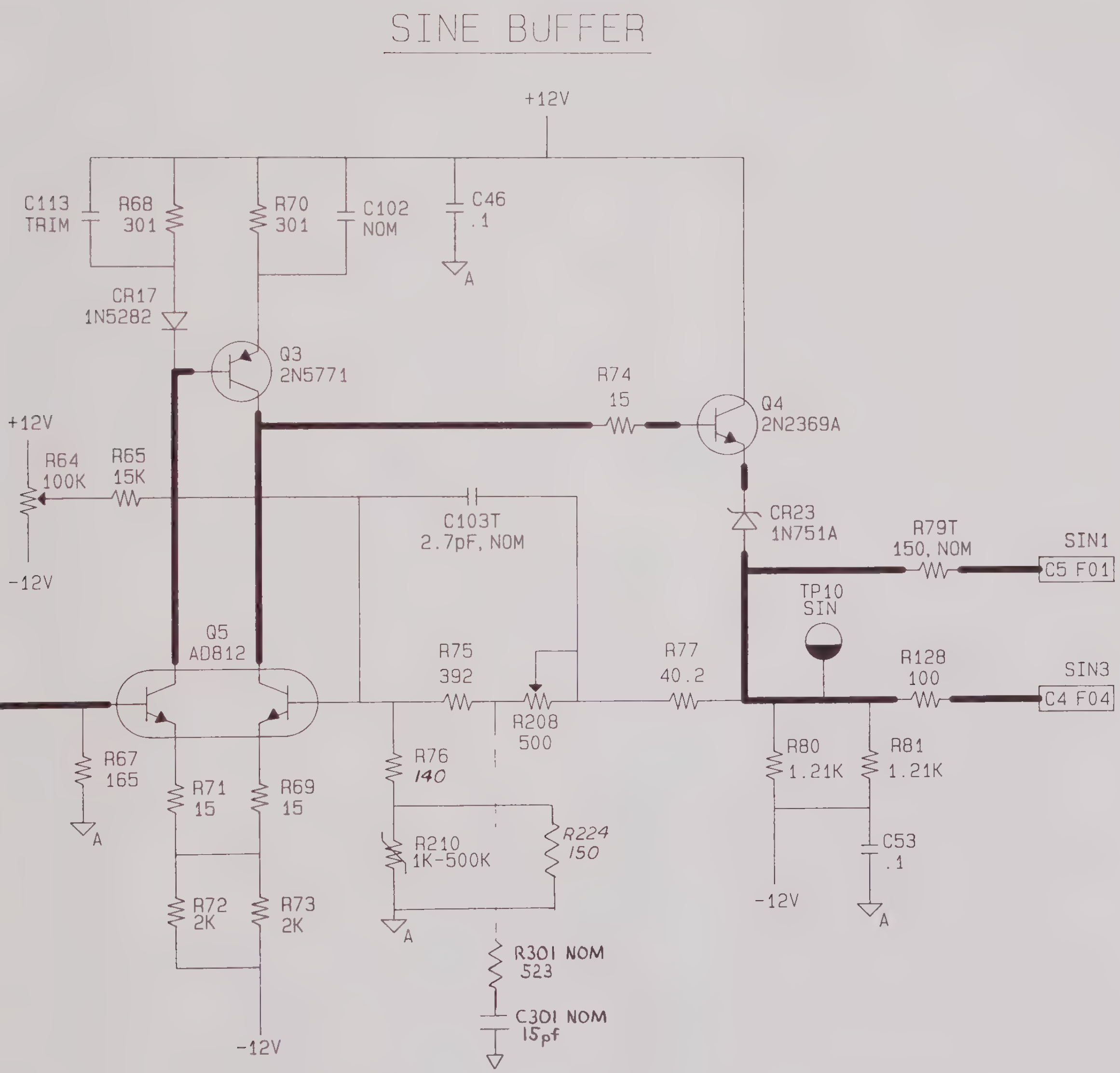
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 7/90	**WAVETEK** SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED JM	7/2/90	TITLE SCHEMATIC, PHASE LOCK LOOP
	PROJ. ENGR	7/2/90	
FINISH WAVETEK PROCESS	RELEASE APPROV.	7/2/90	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3437 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES · SHEET 4 OF 6

SINE CONVERTER

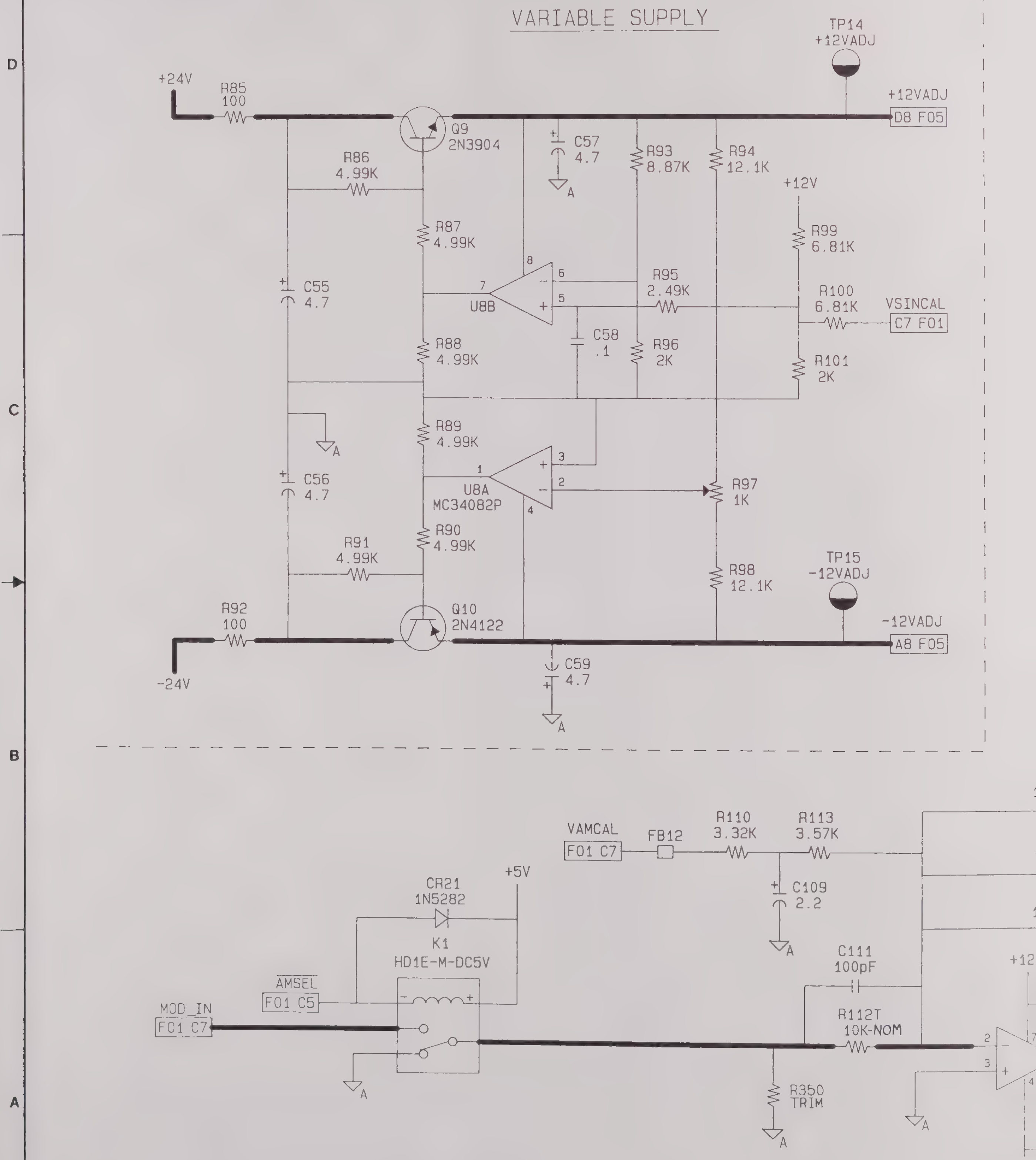

+12VADJ
F06 D5
C41
.1
A
R37
10K
R38
2K
R39
30.1K
R62
100K
R40
150
R52
200
R41
39.2
R55
27.4
CR11
*
CR12
*
R42
392
R49
1.5K
NOM
R53
10
R54
24.9
R56
10
CR13
*
CR7
*
CR8
*
SINSIG
F04 D2
R33
100
R34
21.5
R35
155-180FAK-B01
R36
10
R50
1K-500K
R57
21.5
R58
21.5
A
C40
10pF
A
C43
15pF
A
R146
24.9
R59
10
* DIODE SET 5082-2811.
CR9
*
CR10
*
R51
1.5K
NOM
R147
10
CR16
*
R43
392
CR15
*
CR14
*
R44
39.2
R61
27.4
R45
150
R60
200
R63
100K
R46
10K
R47
2K
R48
30.1K
-12VADJ
F06 B5
C42
.1
A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

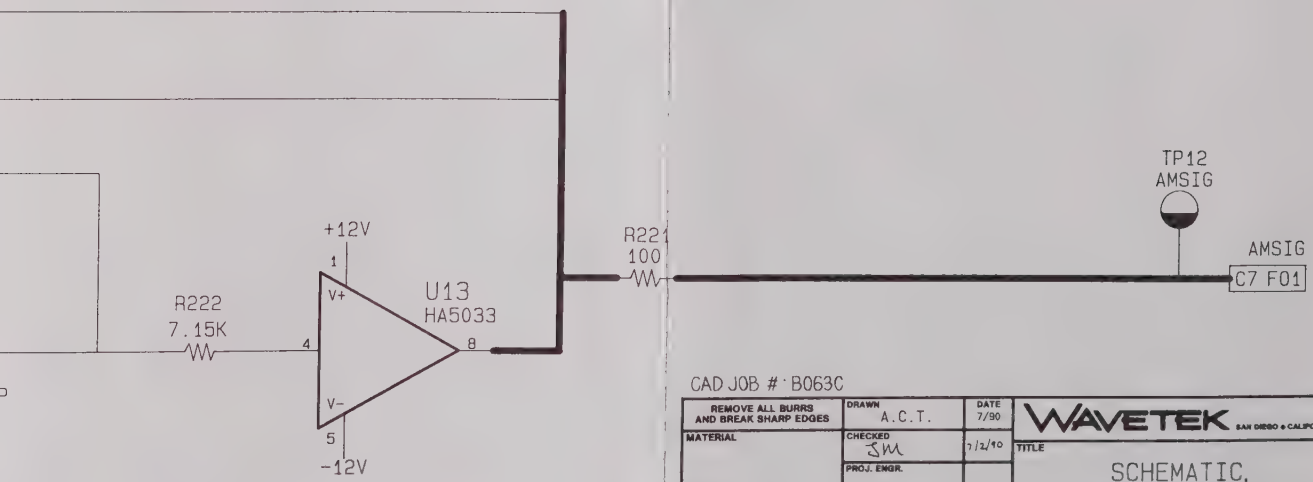

SINE BUFFER
+12V
C113
TRIM
R68
301
R70
301
C102
NOM
C46
.1
A
CR17
1N5282
Q3
2N5771
R74
15
Q4
2N2369A
+12V
R64
100K
R65
15K
-12V
C103T
2.7pF, NOM
CR23
1N751A
R79T
150, NOM
SIN1
C5 F01
TP10
SIN
R128
100
SIN3
C4 F04
Q5
AD812
R75
392
R77
40.2
R208
500
R67
165
A
R71
15
R69
15
R76
140
R80
1.21K
R81
1.21K
R210
1K-500K
R224
150
C53
.1
-12V
A
R72
2K
R73
2K
A
R301 NOM
523
C301 NOM
15pf
-12V

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 7/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED JM	7/2/90	TITLE SCHEMATIC, PHASE LOCK LOOP
	PROJ ENGR		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE. FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3437 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES · SHEET 5 OF 6


VARIABLE SUPPLY
D
C
B
A
TP14
+12VADJ
+24V
R85
100
Q9
2N3904
+12VADJ
D8 F05
R86
4.99K
C57
4.7
R93
8.87K
R94
12.1K
+12V
R87
4.99K
R99
6.81K
8
6
7
U8B
5
R95
2.49K
R100
6.81K
VSINCAL
C7 F01
C55
4.7
R88
4.99K
C58
.1
R96
2K
R101
2K
R89
4.99K
3
1
U8A
MC34082P
2
4
R97
1K
C56
4.7
R90
4.99K
R91
4.99K
R98
12.1K
TP15
-12VADJ
R92
100
Q10
2N4122
-12VADJ
A8 F05
-24V
C59
4.7
VAMCAL
F01 C7
FB12
R110
3.32K
R113
3.57K
C109
2.2
CR21
1N5282
+5V
K1
HD1E-M-DC5V
AMSEL
F01 C5
MOD_IN
F01 C7
C111
100pF
R112T
10K-NOM
R350
TRIM
+12
2
3
4
-12V

NOTE UNLESS OTHERWISE SPECIFIED

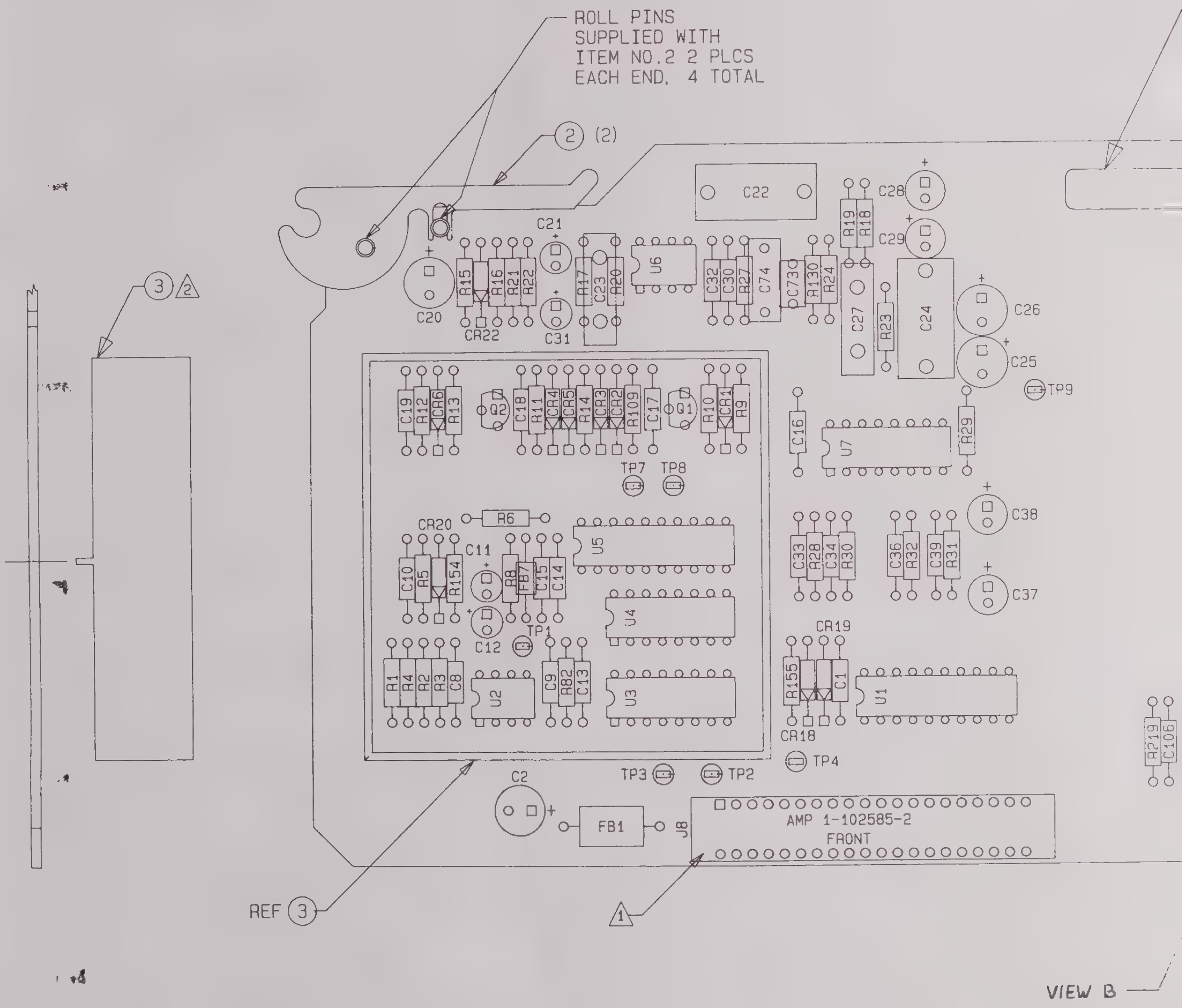
REV	ECO	BY	DATE	APP

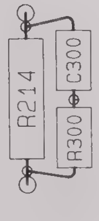

TP12
AMSIG
AMSIG
C7 F01
R221
100
+12V
1
V+
U13
HA5033
8
R222
7.15K
4
V−
5
−12V

1104-00-3437 B

CAD JOB # B063C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 7/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED JM	7/2/90	TITLE SCHEMATIC, PHASE LOCK LOOP
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3437 REV B
DO NOT SCALE DRAWING			SCALE NONE MODEL 90 SERIES SHEET 6 OF 6


ROLL PINS SUPPLIED WITH ITEM NO.2 2 PLCS EACH END, 4 TOTAL
2 (2)
3 2
C20
CR22
C21
C31
R15
R16
R21
R22
R17
C23
R20
U6
C22
C32
C30
R27
C74
C73
R130
R24
R19
R18
C28
C29
C27
R23
C24
C26
C25
TP9
C19
R12
CR6
R13
Q2
C18
R11
CR4
CR5
R14
CR3
CR2
R109
C17
Q1
R10
CR1
R9
C16
U7
R29
TP7
TP8
CR20
R6
C10
R5
R154
C11
R8
FB7
C15
C14
U5
C12
TP1
U4
C38
C37
C33
R28
C34
R30
C36
R32
C39
R31
CR19
R1
R4
R2
R3
C8
U2
C9
R82
C13
U3
R155
C1
U1
CR18
TP4
TP3
TP2
R219
C106
C2
FB1
J8
AMP 1-102585-2
FRONT
REF 3
1
VIEW B


R214
C300
R300

VIEW "A"

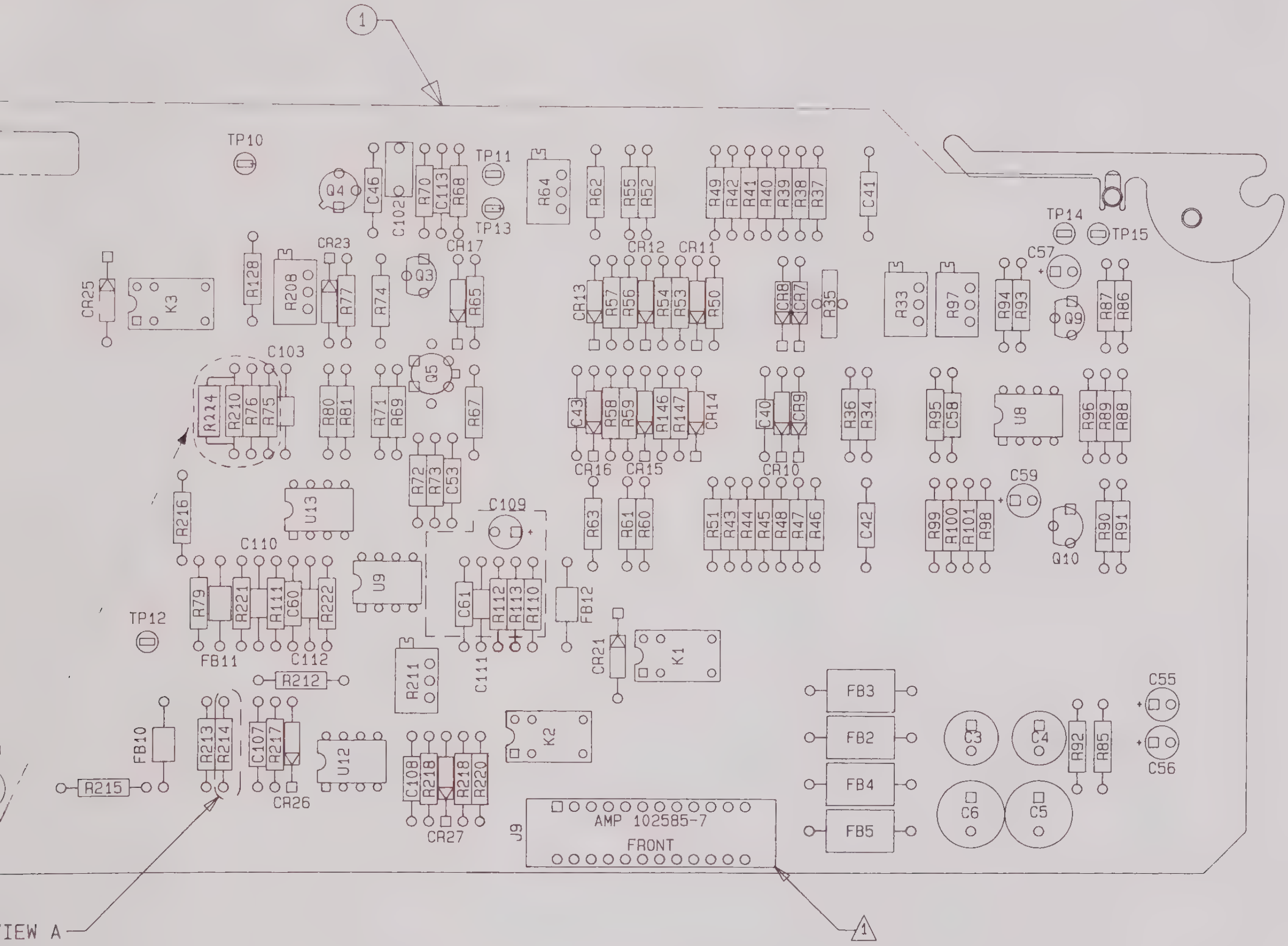
SCALE: NONE

6. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
5. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
4. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
3. SEE 1104-00-3341 FOR SCHEMATIC.
2. INSTALL CAN FLUSH TO COMPONENT SIDE OF P.C. BOARD. SOLDER TABS ON CIRCUIT SIDE.
1. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

NOTE UNLESS OTHERWISE SPECIFIED

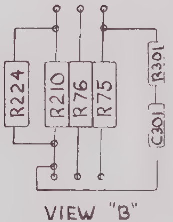
REV	ECO	BY	DATE	APP
A	ECO 90-584 -CLS I FROM: 1101-00-3341	KA	9/21/90	JM 10/9/90
B	ECO#91-121	KA	2/7/91	LJ

ACE ASSEMBLY I.D.
BEL IN THIS AREA



①
TP10
Q4
C46
C102
R70
C113
R68
TP11
TP13
R64
R62
R55
R52
R49
R42
R41
R40
R39
R38
R37
C41
TP14
TP15
C57
CR25
K3
R128
R208
CR23
R77
R74
Q3
CR17
R65
CR12
CR11
CR13
R57
R56
R54
R53
R50
CR8
CR7
R35
R33
R97
R94
R93
Q9
R87
R86
C103
R214
R210
R76
R75
R80
R81
R71
R69
Q5
R67
C43
R58
R59
R146
R147
CR14
C40
CR9
R36
R34
R95
C58
U8
R96
R89
R88
CR16
CR15
CR10
R216
U13
R72
R73
C53
C109
R63
R61
R60
R51
R43
R44
R45
R48
R47
R46
C42
R99
R100
R101
R98
C59
Q10
R90
R91
C110
R79
R221
R111
C60
R222
U9
C61
R112
R113
R110
FB12
TP12
FB11
C112
R212
R211
C111
CR21
K1
FB3
C55
FB10
R213
R214
C107
R217
U12
R215
CR26
C108
R218
R218
R220
K2
FB2
C3
C4
R92
R85
C56
FB4
J9
AMP 102585-7
FRONT
C6
C5
FB5
CR27
1

IEW A



R224
R210
R76
R75
R301
C301

VIEW "B"
SCALE: NONE

ACCEPTABLE VALUES FOR R112T	
R112T	
9.76K	
10K	
10.5K	

CAD JOB #: B063D

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

		DATE
DRAWN	Amy Talmadge	6/20/90
CHECKED	D.FISH	6/29/90
PROJ. ENGR.	D. E. FISH	6/29/90
RELEASE APPROV	JM	10/9/90

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PCA, PHASE
LOCK LOOP BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1101-00-3437	B

SCALE 2/1 MODEL 90 SERIES SHEET 1 OF 1

1101-00-3437 B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D PHASE LOCK LOOP	1101-00-3437	WVTK	1101-00-3437	1
NONE	SCHEMATIC, PHASE LOCK LOOP	1104-00-3437	WVTK	1104-00-3437	1
R8	RES,CFLM 4.7 OHM 5% 1/4W	5043CX4R700J	MEPCO	116.9471	1
CR26 CR27	SL ZR 6.2V 5% 400MW (1N753A)	1N753A	ROHM	131.9620	2
3	CAN,SYNTHESIZER	1400-02-3443	WVTK	1400-02-3443	1
C112 C300 C40	CAP,CER,10PF,100V,AXIAL	CAC02CDG100J100A	CORNG	1500-01-0006	3
C111	CAP,CER,100PF,100V,AXIAL	CAC02CDG101J100A	CORNG	1500-01-0106	1
C1 C10 C106 C107 C108 C13 C14 C15 C16 C17 C18 C19 C30 C32 C33 C34 C36 C39 C41 C42 C46 C53 C58 C60 C61 C8 C9	CAP,CER,MON,.1MF,50V,AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	27
C43	CAP,CER,15PF,100V,AXIAL	CAC02CDG150J100A	CORNG	1500-01-5006	1
C110	CAP,CER,150PF,100V,5%,AXIAL	CAC02CDG151J100A	CORNG	1500-01-5100	1
C102T	CAP CER MON 2.7PF 50V	CCD2R7DNPO	ARCO	1500-02-7505	1
C103T	CAP,CER,2.7PF,100V,AX	CAC02CDG2R7J100A	CORNG	1500-02-7906	1

WAVETEK PARTS LIST
TITLE PCA, PHASE LOCK LOOP
ASSEMBLY NO. 1100-00-3437
PAGE 1
REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	IAL				
C73	CAP,CER,470PF,1KV	DD-471	CRL	1500-04-7111	1
C37 C38	CAP,ELECT,10MF,20%,16V,END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	2
C5 C6	CAP,ELECT,100MF,35V RADIAL LEAD,SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	2
C2 C3 C4	CAP,ELECT,100MF,25V,RADIAL LEAD-SP SIZE	NRE101M25V6.3X11	NIC	1500-31-0122	3
C20 C25 C26	CAP,ELECT,220MF,20%,16V,RADIAL END MOUNT, 0.14 LEAD SPACE	16TWSS220M	RUBY	1500-32-2104	3
C11 C12 C21 C31 C55 C56 C57 C59	CAP,ELECT,4.7MF/50V RADIAL LEAD, SP .10	ECEA1HV4R7SC	PANAS	1500-34-7903	8
C23 C74	CAP,MYLAR,.01MF,100V	225P10391WD3	SPRAG	1500-41-0314	2
C22 C24	CAP,MYLAR,1MF,100V,RADIAL	PMT2R1.0K100	ITT	1500-41-0524	2
C27	CAP,MYLAR,.0047MF,100V,RADIAL	225P47291WD3	SPRAG	1500-44-7204	1
C109 C28 C29	CAP,TANT,2.2MF,25V	199D225X9025AA2	SPRAG	1500-72-2502	3
NONE	PCB,PHASE LOCK LOOP BD	1700-00-3341	WVTK	1700-00-3341	1

WAVETEK PARTS LIST
TITLE PCA, PHASE LOCK LOOP
ASSEMBLY NO. 1100-00-3437
PAGE 2
REV A

REFERENCE DESIGNATORS	PART DESCRIPTION
J9	CONN,HEADER,24 PIN,RECPT,2X12, .1 CTR, PCMT
J8	CONN,HEADER,40 PIN,RECPT,2X20,.1 C PCMT
TP11 TP4	TEST POINT,BLK,PC
TP1 TP10 TP12 TP13 TP14 TP15 TP2 TP3 TP7 TP8 TP9	TEST POINT,RED,PC
2	PC BD EJECTOR
FB1 FB2 FB3 FB4 FB5	BALUN CORE,FERRITE,680 O
FB10 FB11 FB12 FB7	BALUN CORE,FERRITE, OHMS
K1 K2 K3	RELAY,1 FORMC,5V,.312H,.296
R64	POT,SIDE TRIM,20T,100K
R208	POT,SIDE TRIM,20T,
R97	POT,SIDE TRIM,20T,
R211 R33	POT,SIDE TRIM,20T,

WAVETEK PARTS LIST
TITLE PCA, PHASE LOCK LOOP

REFERENCE DESIGNATORS	PART DESCRIPTION
R128 R215 R216 R221 R85 R92	RES,MF,1/8W,1%,100
R14 R20	RES,MF,1/8W,1%,1K
R112 R217 R218 R219 R37 R46	RES,MF,1/8W,1%,10K
R62 R63	RES,MF,1/8W,1%,100
R147 R212 R222 R27 R36 R53 R56 R59	RES,MF,1/8W,1%,10
R29	RES,MF,1/8W,1%,110
R220	RES,MF,1/8W,1%,121
R80 R81	RES,MF,1/8W,1%,1.2
R94 R98	RES,MF,1/8W,1%,12.
R76	RES,MF,1/8W,1%,140
R224 R40 R45 R79T	RES,MF,1/8W,1%,150
R49T R51T R6	RES,MF,1/8W,1%,1.5
R109 R65	RES,MF,1/8W,1%,15K
R154 R69 R71 R74	RES,MF,1/8W,1%,15
R15 R67	RES,MF,1/8W,1%,165
R2 R52 R60	RES,MF,1/8W,1%,200

WAVETEK PARTS LIST
TITLE PCA, PHASE LOCK LOOP

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
102585-7	AMP	2100-02-0255	1
-102585-2	AMP	2100-02-0256	1
TP-104-01-00	COMPO	2100-04-0054	2
TP-104-01-02	COMPO	2100-04-0055	11
37-2-C	BRIT	2800-07-0032	2
2943666671	FARIT	3100-00-0017	5
2743015111	FARIT	3100-00-0018	4
D1E-M-DC5V	AROMT	4500-00-0034	3
8XR100K	BECK	4609-90-0012	1
8XR500	BECK	4609-90-0014	1
8XR1K	BECK	4609-90-0015	1
8XR100	BECK	4609-90-0017	2

ASSEMBLY NO. 1100-00-3437 REV A

PAGE 3

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RN55D-1000F	TRW	4701-03-1000	6
RN55D-1001F	TRW	4701-03-1001	2
RN55D-1002F	TRW	4701-03-1002	6
RN55D-1003F	TRW	4701-03-1003	2
5043ED10R100F	MEPCO	4701-03-1009	8
N55D-1103F	TRW	4701-03-1103	1
N55D-1210F	TRW	4701-03-1210	1
N55D-1211F	TRW	4701-03-1211	2
N55D-1212F	TRW	4701-03-1212	2
N55D-1400F	TRW	4701-03-1400	1
N55D-1500F	TRW	4701-03-1500	4
N55D-1501F	TRW	4701-03-1501	3
N55D-1502F	TRW	4701-03-1502	2
N55D-15R0F	TRW	4701-03-1509	4
N55D-1650F	TRW	4701-03-1650	2
N55D-2000F	TRW	4701-03-2000	3

ASSEMBLY NO. 1100-00-3437 REV A

PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R101 R38 R47 R72 R73 R96	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	6
R34 R57 R58	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	3
R300	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	1
R28 R3 R30 R31 R32 R95	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	6
R146 R54	RES, MF, 1/8W, 1%, 24.9	RN55D-24R9F	TRW	4701-03-2499	2
R55 R61	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	2
R113	RES, MF, 1/8W, 1%, 2.94K	5033RD2941F	MEPCO	4701-03-2941	1
R1 R68 R70	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	3
R11 R39 R48	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	3
R223	RES, MF, 1/8W, 1%, 30.1	RN55D-30R1F	TRW	4701-03-3019	1
R110	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R155 R4 R42 R43 R75	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	5
R41 R44	RES, MF, 1/8W, 1%, 39.2	RN55D-39R2F	TRW	4701-03-3929	2
R77	RES, MF, 1/8W, 1%, 40.2	RN55D-40R2F	TRW	4701-03-4029	1
R213 R214	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	2
R82 R86 R87 R88 R89 R90 R91	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	7
R23 R24	RES, MF, 1/8W, 1%, 5.49K	RN55D-5491F	MEPCO	4701-03-5491	2

WAVETEK
PARTS LIST

TITLE
PCA, PHASE LOCK LOOP

ASSEMBLY NO. 1100-00-3437 REV A

PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R5	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	1
R100 R99	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	2
R111	RES, MF, 1/8W, 1%, 7.15K	RN55D-7151F	TRW	4701-03-7151	1
R21 R22	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	2
R10 R12 R13 R130 R16 R17 R18 R19 R9	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	9
R93	RES, MF, 1/8W, 1%, 8.87K	RN55D-8871F	TRW	4701-03-8871	1
CR20 CR22 CR23	DIODE, ZENOR, 5.1V, 500MW, GIB, IN751A	1N751A	FAIR	4801-01-0751	3
CR1 CR17 CR18 CR19 CR2 CR21 CR25 CR3 CR4 CR5 CR6	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	11
CR10 11 12 13 14 15 16 7 8 9	DIODE SET, 5082-2811 QTY: 10: 4809-02-2811	4898-00-0015	KLG	4898-00-0015	1
Q4	TRANS, SILICON, PLANAR, EPITAXIAL, NPN, TO-18	2N2369A	MOT	4901-02-3691	1
Q2	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	1
Q9	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	1
Q10	TRANS, GENERAL	PN4122	NSC	4901-04-1220	1

WAVETEK
PARTS LIST

TITLE
PCA, PHASE LOCK LOOP

ASSEMBLY NO. 1100-00-3437 REV A

PAGE 6

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
PHASE LOCK LOOP BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-3437	A

SCALE | MODEL 95 | SHEET 1 OF 2

115686

D

C

B

A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	PURPOSE, PNP, TO-92				
Q1 Q3	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	2
Q13	TRANS	VN10KM	INTSL	4902-00-0100	1
R35	THERMISTOR 18.6 OHMS +/-25% CUST COATED	155-180FAK-B01	FENWL	5300-00-0002	1
R210 R50	THERMISTER, 50 OHM, +-10%, @ 25 DEG C	1K-500-K	MCI	5300-00-0013	2
U12	WIDWBAND HIGH SLEW RATE OP AMP	CLC404AJP	COMLR	7000-04-0410	1
Q5	TRANS, MONO, DUAL, NPN	LS312-52	LINSY	7000-08-1200	1
U2	COMPARATOR, ULTRA FAST, 10NS	LT1016CN8	LINTE	7000-10-1600	1
U13	VIDEO BUFFER	HA3-5033-5	HARIS	7000-50-3300	1
U6	OP AMP, HI SLEW RTE, WIDEBND, JFET, STD	MC34081P	MOT	7003-40-8100	1
U9	OP AMP, HI SLEW RTE, WIDEBND, JFET, PRIM E	MC34081AP	MOT	7003-40-8101	1
U8	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	1

WAVETEK
PARTS LIST
TITLE
PCA, PHASE LOCK LOOP
ASSEMBLY NO. 1100-00-3437
PAGE 7
REV
A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U7	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	1
U3	MUX/SEL, DUAL 1 OF 4 DATA, 3/STATE	SN74ALS253N	TI	8007-42-5300	1
U4	COUNTER, DUAL 4B BCD, TTL	74LS390PC	FAIR	8007-43-9010	1
U1	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	1
U5	PAL, PROG USES 1 EA 8000-16-8000 FOR 1288 PHASE DET. V1.0	8600-00-0497	WVTK	8600-00-0497	1

WAVETEK
PARTS LIST
TITLE
PCA, PHASE LOCK LOOP
ASSEMBLY NO. 1100-00-3437
PAGE 8
REV
A

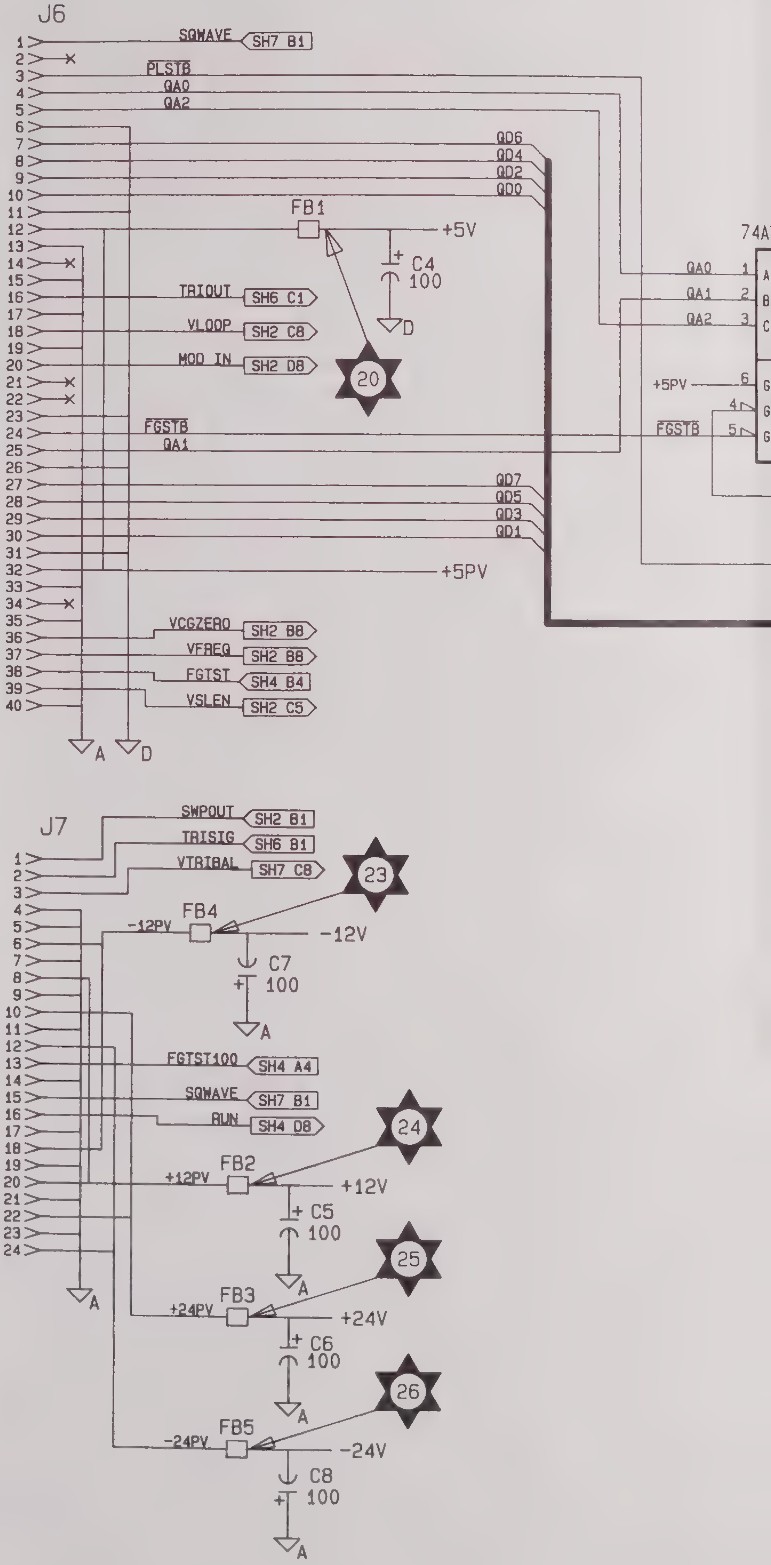
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

DRAWN
CHECKED
PROJ. ENGR.
RELEASE APPROV
DATE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
PHASE LOCK LOOP BOARD

SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-3437
REV A
SCALE
MODEL 95
SHEET 2 OF 2



8
7
6
5
D
C
B
A
J6
SQWAVE
SH7 B1
PLSTB
QA0
QA2
QD6
QD4
QD2
QD0
FB1
+5V
C4
100
D
TRIOUT
SH6 C1
VLOOP
SH2 C8
MOD IN
SH2 D8
20
FGSTB
QA1
QD7
QD5
QD3
QD1
+5PV
VCGZERO
SH2 B8
VFREQ
SH2 B8
FGTST
SH4 B4
VSLEN
SH2 C5
A
D
74A
QA0
QA1
QA2
+5PV
FGSTB
J7
SWPOUT
SH2 B1
TRISIG
SH6 B1
VTRIBAL
SH7 C8
23
FB4
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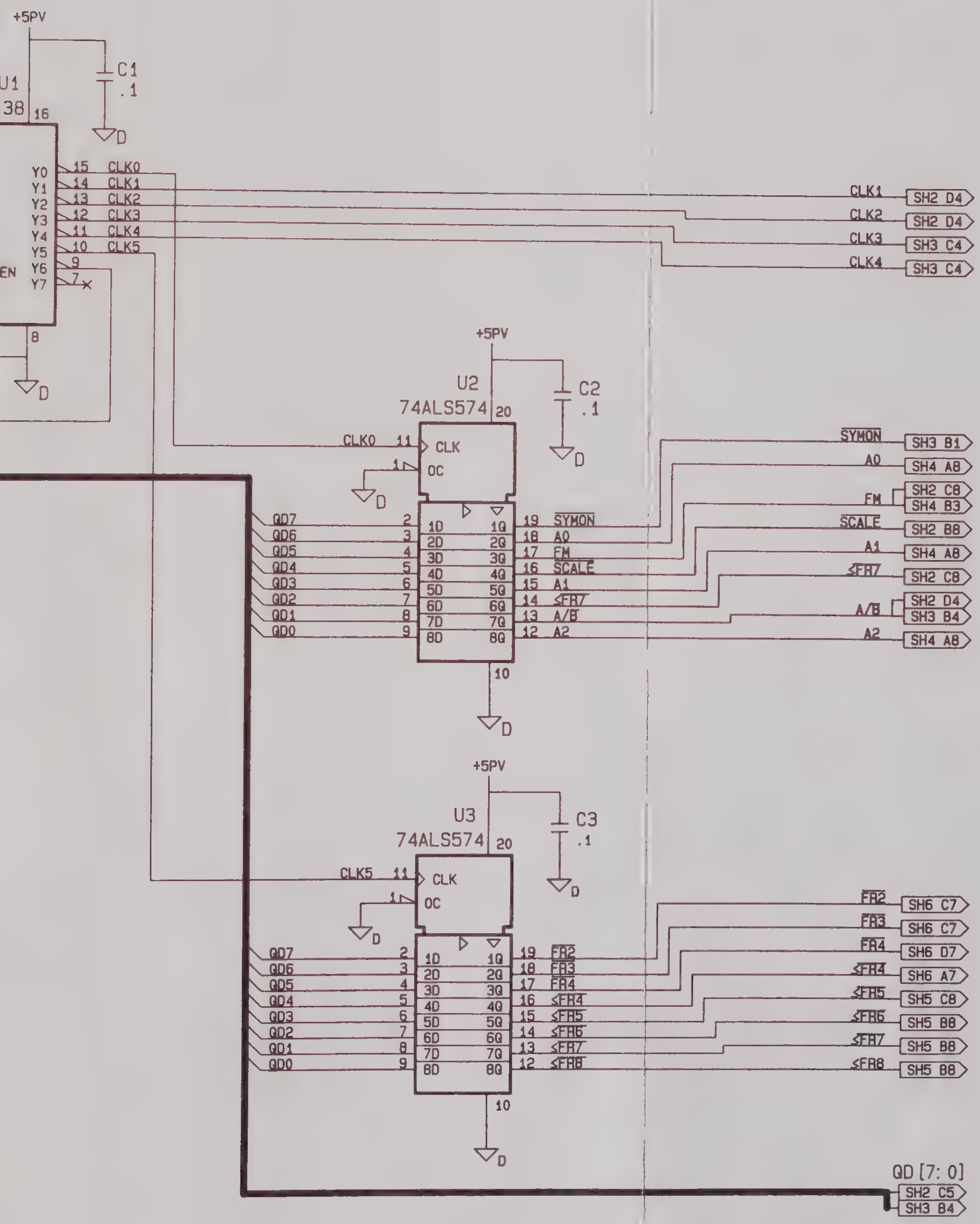
-12V
C7
100
FGTST100
SH4 A4
SQWAVE
SH7 B1
RUN
SH4 D8
24
FB2
+12PV
+12V
C5
100
25
FB3
+24PV
+24V
C6
100
26
FB5
-24PV
-24V
C8
100

5. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
4. ▽A = ANALOG GROUND SYMBOL.
3. ▽D = DIGITAL GROUND SYMBOL.
2. ALL CAPACITORS ARE IN MICROFARADS.
1. ALL RESISTORS ARE IN OHMS, 1/8W, 1%, MF.

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ERO # 90-491	AQ	6-29-90	
A				



+5PV
C1
.1
U1
38
16
Y0 15 CLK0
Y1 14 CLK1
Y2 13 CLK2
Y3 12 CLK3
Y4 11 CLK4
Y5 10 CLK5
EN Y6 9
Y7 7
8
D
CLK1 SH2 D4
CLK2 SH2 D4
CLK3 SH3 C4
CLK4 SH3 C4
+5PV
U2
74ALS574
20
C2
.1
CLK0 11 CLK
1 OC
QD7 2 1D 1Q 19 SYMON
QD6 3 2D 2Q 18 A0
QD5 4 3D 3Q 17 FM
QD4 5 4D 4Q 16 SCALE
QD3 6 5D 5Q 15 A1
QD2 7 6D 6Q 14 ≤FR7
QD1 8 7D 7Q 13 A/B
QD0 9 8D 8Q 12 A2
10
SYMON SH3 B1
A0 SH4 A8
FM SH2 C8 SH4 B3
SCALE SH2 B8
A1 SH4 A8
≤FR7 SH2 C8
A/B SH2 D4 SH3 B4
A2 SH4 A8
+5PV
U3
74ALS574
20
C3
.1
CLK5 11 CLK
1 OC
QD7 2 1D 1Q 19 FR2
QD6 3 2D 2Q 18 FR3
QD5 4 3D 3Q 17 FR4
QD4 5 4D 4Q 16 ≤FR4
QD3 6 5D 5Q 15 ≤FR5
QD2 7 6D 6Q 14 ≤FR6
QD1 8 7D 7Q 13 ≤FR7
QD0 9 8D 8Q 12 ≤FR8
10
FR2 SH6 C7
FR3 SH6 C7
FR4 SH6 D7
≤FR4 SH6 A7
≤FR5 SH5 C8
≤FR6 SH5 B8
≤FR7 SH5 B8
≤FR8 SH5 B8
QD [7: 0]
SH2 C5
SH3 B4
D

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN A. TALMADGE — DATE 5-8-90
CHECKED D. FISH — 6/29/90
PROJ. ENGR. D.E. Fisk — 6/29/90
RELEASE APPROV D.E. Fisk — 6/29/90

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE.
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

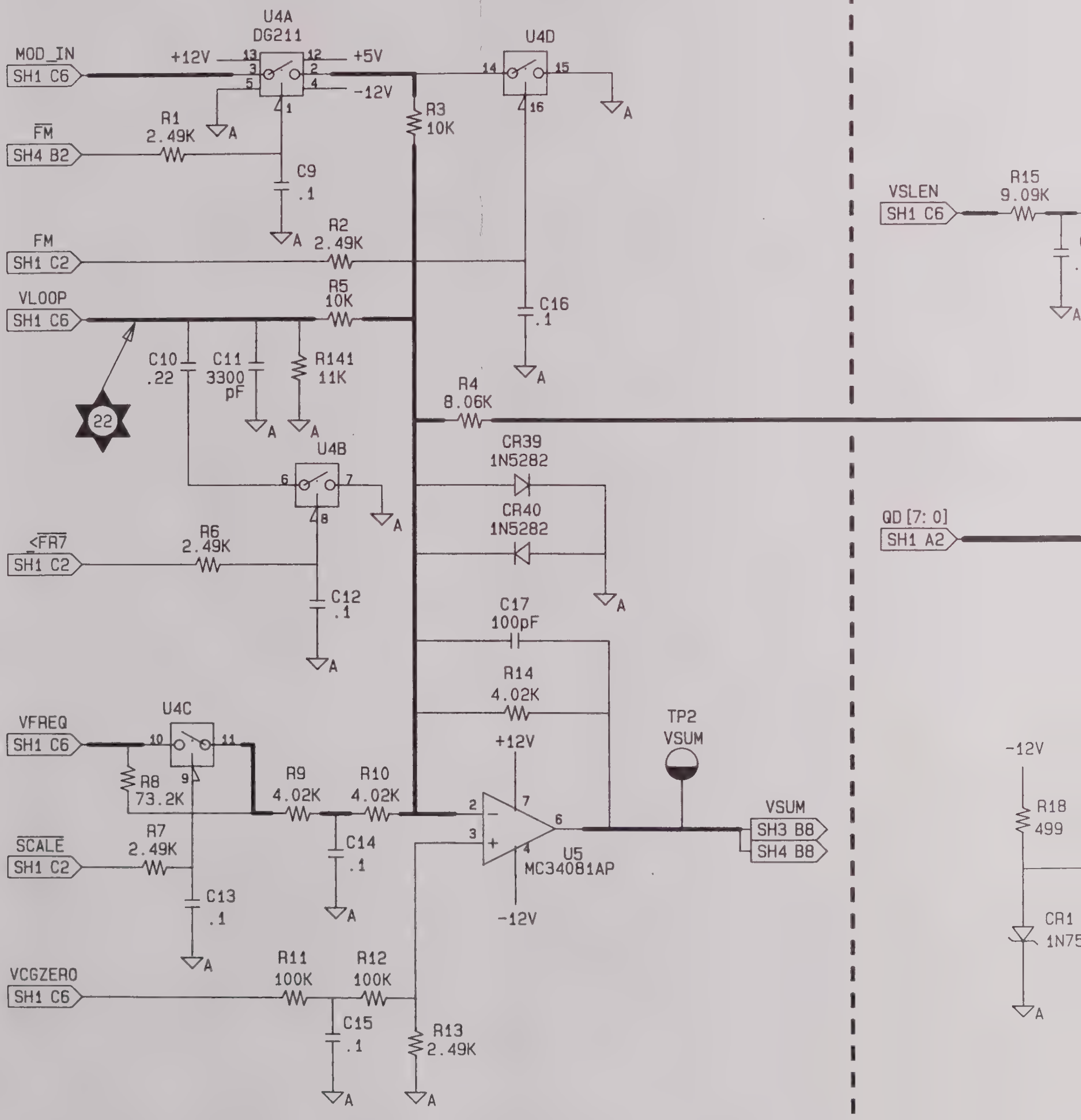
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
FUNCTION GENERATOR

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3342	A

SCALE NONE — MODEL 90 SERIES — SHEET 1 OF 7

VCG SUMMING AMPLIFIER



U4A
DG211
MOD_IN
SH1 C6
+12V
13
3
5
12
2
4
+5V
-12V
1
A
U4D
14
15
16
R1
2.49K
FM
SH4 B2
C9
.1
R3
10K
R2
2.49K
FM
SH1 C2
R5
10K
VLOOP
SH1 C6
C16
.1
C10
.22
C11
3300
pF
R141
11K
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R4
8.06K
U4B
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R6
2.49K
C12
.1
C17
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VFREQ
SH1 C6
10
11
9
R8
73.2K
R9
4.02K
R10
4.02K
TP2
VSUM
+12V
2
3
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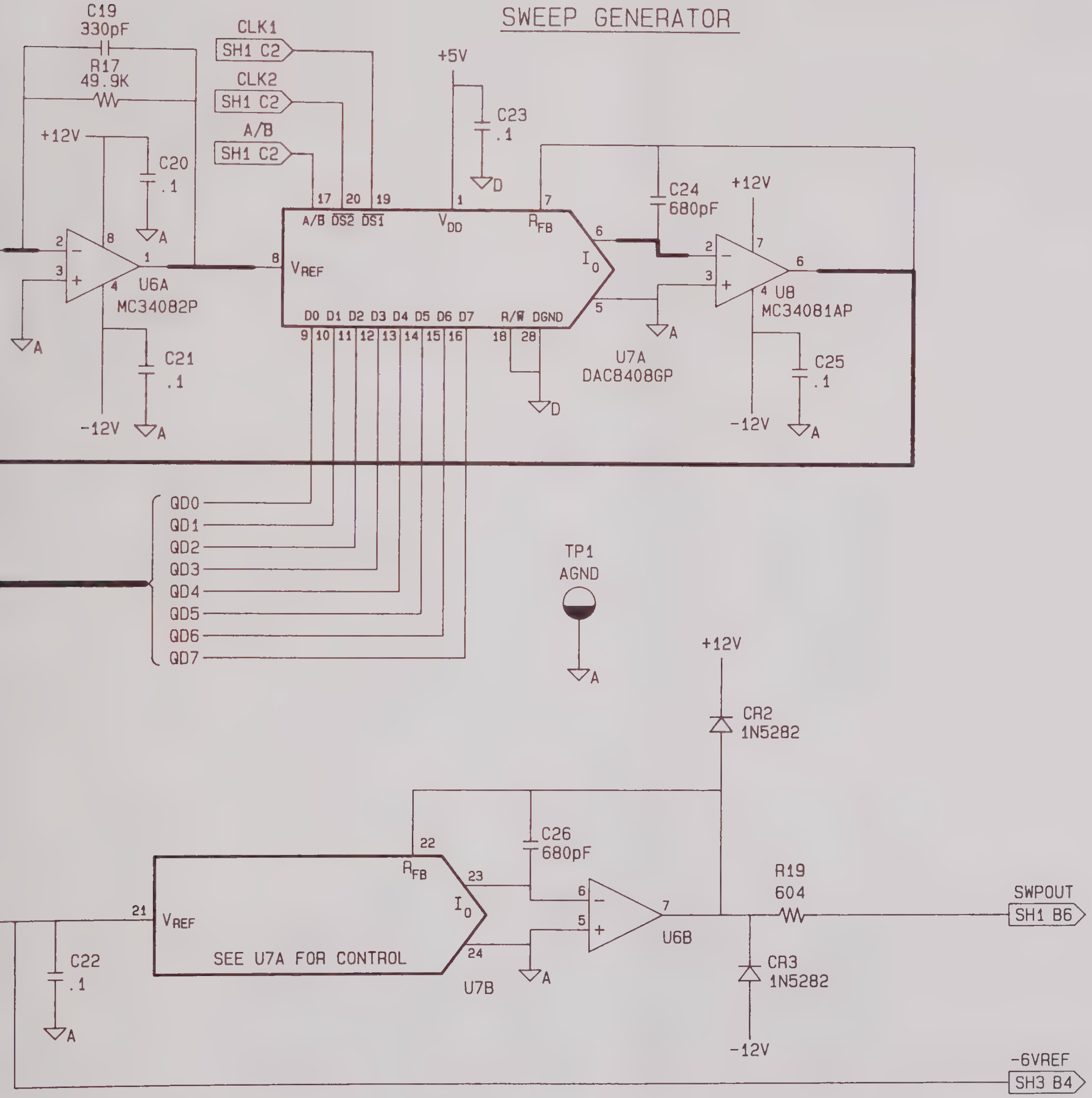
4
U5
MC34081AP
-12V
VSUM
SH3 B8
SH4 B8
SCALE
SH1 C2
R7
2.49K
C14
.1
C13
.1
VCGZERO
SH1 C6
R11
100K
R12
100K
C15
.1
R13
2.49K
VSLEN
SH1 C6
R15
9.09K
QD [7: 0]
SH1 A2
-12V
R18
499
CR1
1N75
A

NOTE UNLESS OTHERWISE SPECIFIED

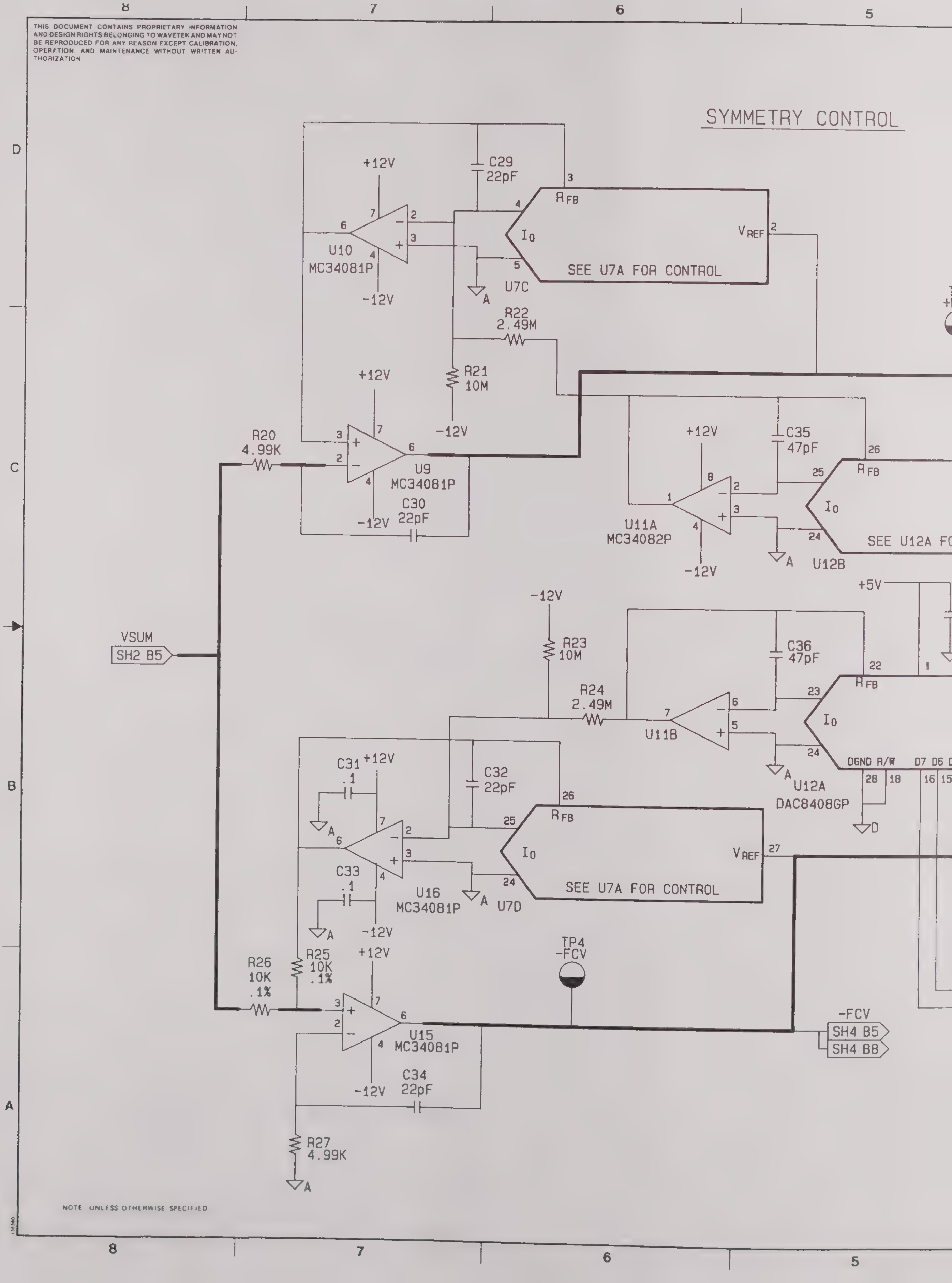
REV	ECO	BY	DATE	APP

SWEEP GENERATOR

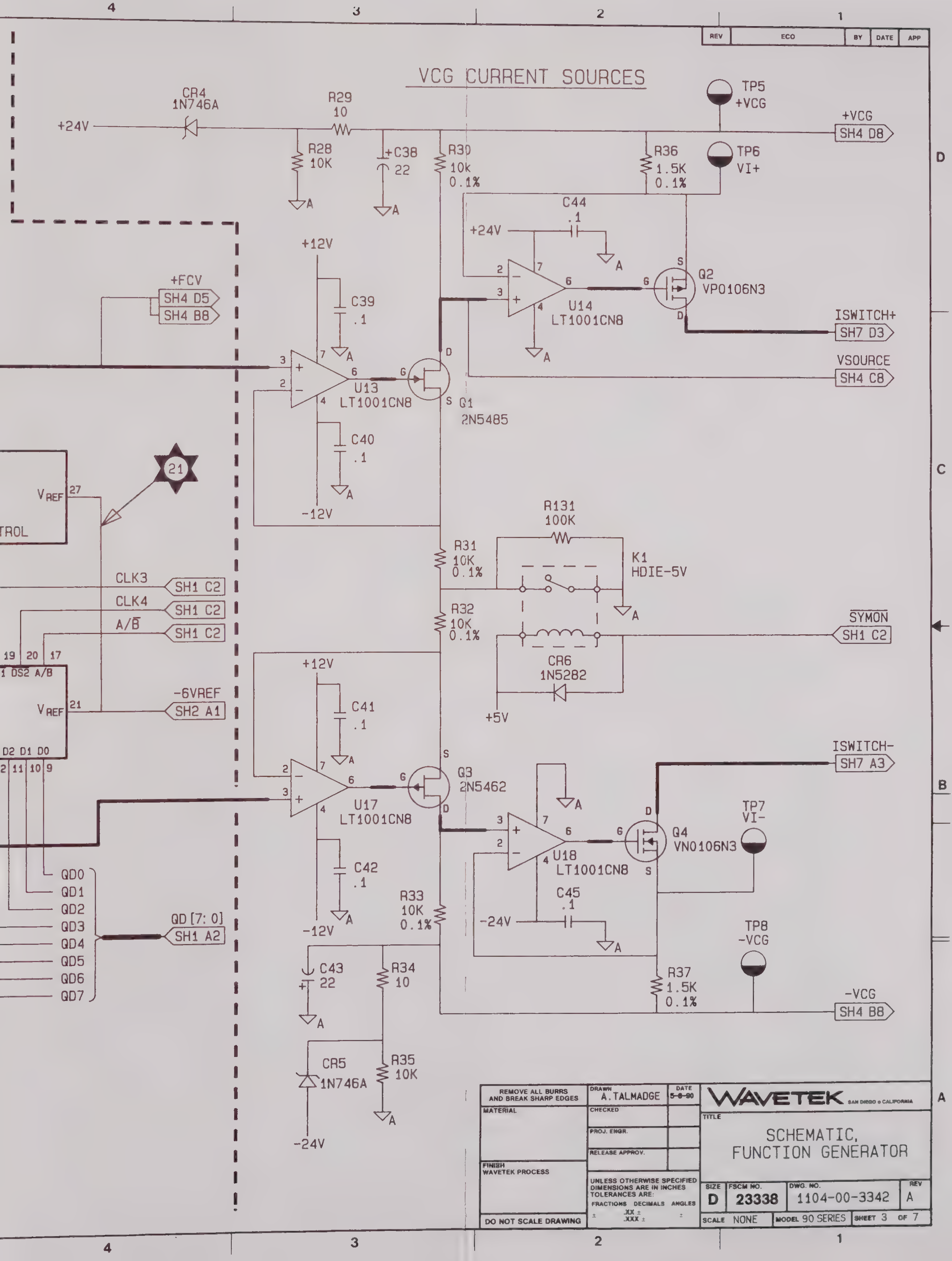

C19
330pF
R17
49.9K
CLK1
SH1 C2
CLK2
SH1 C2
A/B
SH1 C2
+5V
C23
.1
D
+12V
C20
.1
A
17 20 19 1 7
A/B DS2 DS1
VDD
RFB
C24
680pF
+12V
2 8 1
U6A
MC34082P
3 4
8
VREF
IO
6
2 7
3 4
U8
MC34081AP
6
5
A
D0 D1 D2 D3 D4 D5 D6 D7
R/W DGND
9 10 11 12 13 14 15 16 18 28
C21
.1
-12V
A
U7A
DAC8408GP
D
C25
.1
-12V
A
QD0
QD1
QD2
QD3
QD4
QD5
QD6
QD7
TP1
AGND
A
+12V
CR2
1N5282
22
C26
680pF
RFB
23
21
VREF
IO
6
5
7
U6B
R19
604
SWPOUT
SH1 B6
SEE U7A FOR CONTROL
24
U7B
A
C22
.1
A
CR3
1N5282
-12V
-6VREF
SH3 B4

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 5-8-90	**WAVETEK** SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE SCHEMATIC, FUNCTION GENERATOR
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3342 REV A
DO NOT SCALE DRAWING			SCALE NONE MODEL 90 SERIES SHEET 2 OF 7

SYMMETRY CONTROL


8
7
6
5
D
C
B
A
+12V
C29
22pF
3
RFB
4
2
7
6
3
Io
VREF
2
U10
MC34081P
4
5
SEE U7A FOR CONTROL
U7C
A
-12V
R22
2.49M
+12V
R21
10M
-12V
7
3
6
R20
4.99K
2
U9
MC34081P
4
C30
22pF
-12V
+12V
C35
47pF
26
25
RFB
8
2
Io
1
3
U11A
MC34082P
4
24
SEE U12A FO
A
U12B
-12V
+5V
-12V
VSUM
SH2 B5
R23
10M
C36
47pF
22
RFB
R24
2.49M
23
7
6
Io
5
U11B
24
DGND R/W
D7 D6
28
18
16
15
A
U12A
DAC8408GP
D
C31
.1
+12V
C32
22pF
26
RFB
25
7
2
A
6
Io
VREF
27
3
C33
.1
4
24
U16
MC34081P
SEE U7A FOR CONTROL
A
U7D
A
-12V
TP4
-FCV
R26
10K
.1%
R25
10K
.1%
+12V
3
7
6
2
U15
MC34081P
4
-FCV
SH4 B5
SH4 B8
C34
22pF
-12V
R27
4.99K
A
8
7
6
5

NOTE UNLESS OTHERWISE SPECIFIED


4
3
2
1
REV
ECO
BY
DATE
APP
D
C
B
A
VCG CURRENT SOURCES
CR4
1N746A
+24V
R29
10
R28
10K
+C38
22
R30
10k
0.1%
R36
1.5K
0.1%
TP5
+VCG
TP6
VI+
+VCG
SH4 D8
C44
.1
+24V
A
2
7
3
6
4
U14
LT1001CN8
S
6
D
Q2
VP0106N3
ISWITCH+
SH7 D3
VSOURCE
SH4 C8
+12V
C39
.1
+FCV
SH4 D5
SH4 B8
3
2
7
6
4
U13
LT1001CN8
G
D
S
Q1
2N5485
C40
.1
-12V
21
VREF
27
TROL
R131
100K
R31
10K
0.1%
K1
HDIE-5V
R32
10K
0.1%
SYMON
SH1 C2
CLK3
SH1 C2
CLK4
SH1 C2
A/B̅
SH1 C2
CR6
1N5282
+5V
19
20
17
1 DS2 A/B
VREF
21
-6VREF
SH2 A1
D2 D1 D0
2 11 10 9
+12V
C41
.1
2
3
7
6
4
U17
LT1001CN8
G
S
D
Q3
2N5462
ISWITCH-
SH7 A3
3
2
7
6
4
U18
LT1001CN8
G
D
S
Q4
VN0106N3
TP7
VI-
C42
.1
-12V
R33
10K
0.1%
C45
.1
-24V
TP8
-VCG
QD0
QD1
QD2
QD3
QD4
QD5
QD6
QD7
QD [7: 0]
SH1 A2
C43
22
R34
10
R37
1.5K
0.1%
-VCG
SH4 B8
CR5
1N746A
R35
10K
-24V
A

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN A. TALMADGE DATE 5-8-90

CHECKED

PROJ. ENGR.

RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

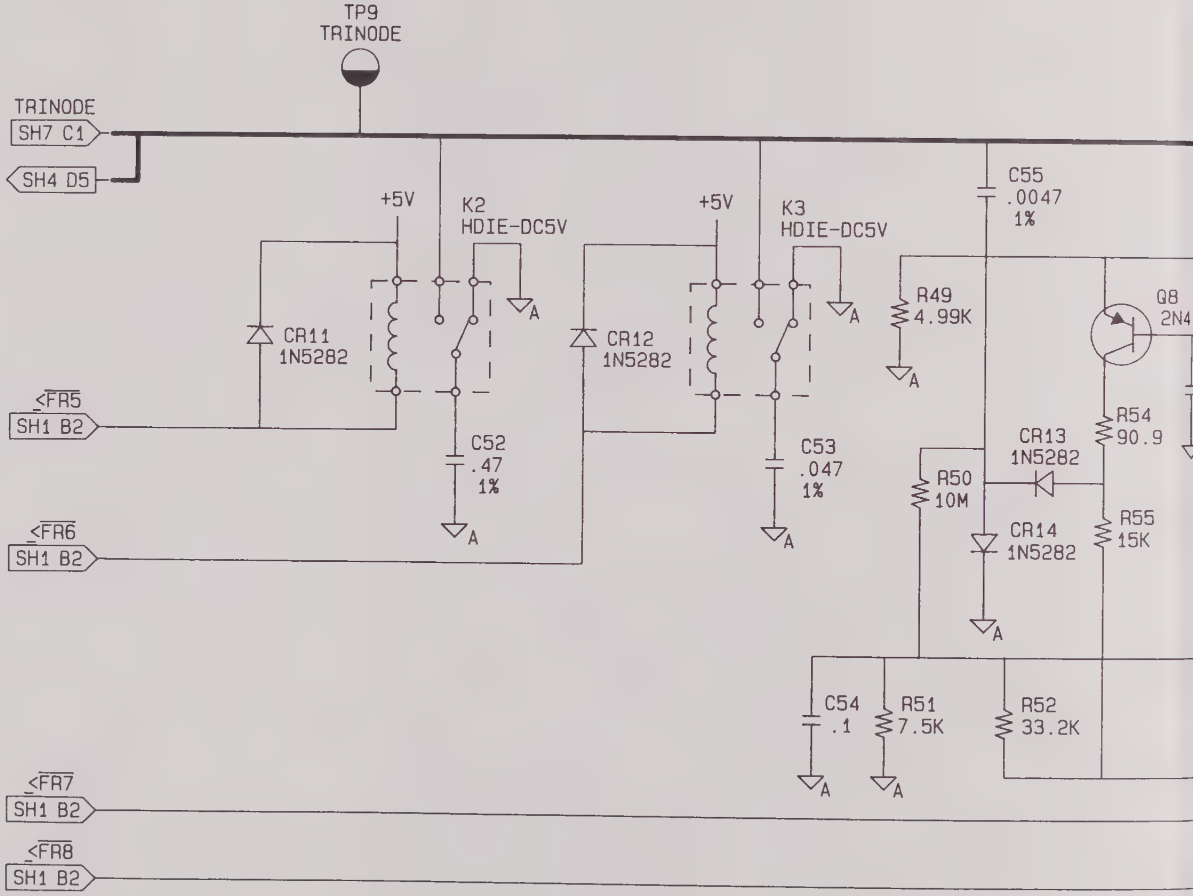
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
FUNCTION GENERATOR

SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3342 REV A

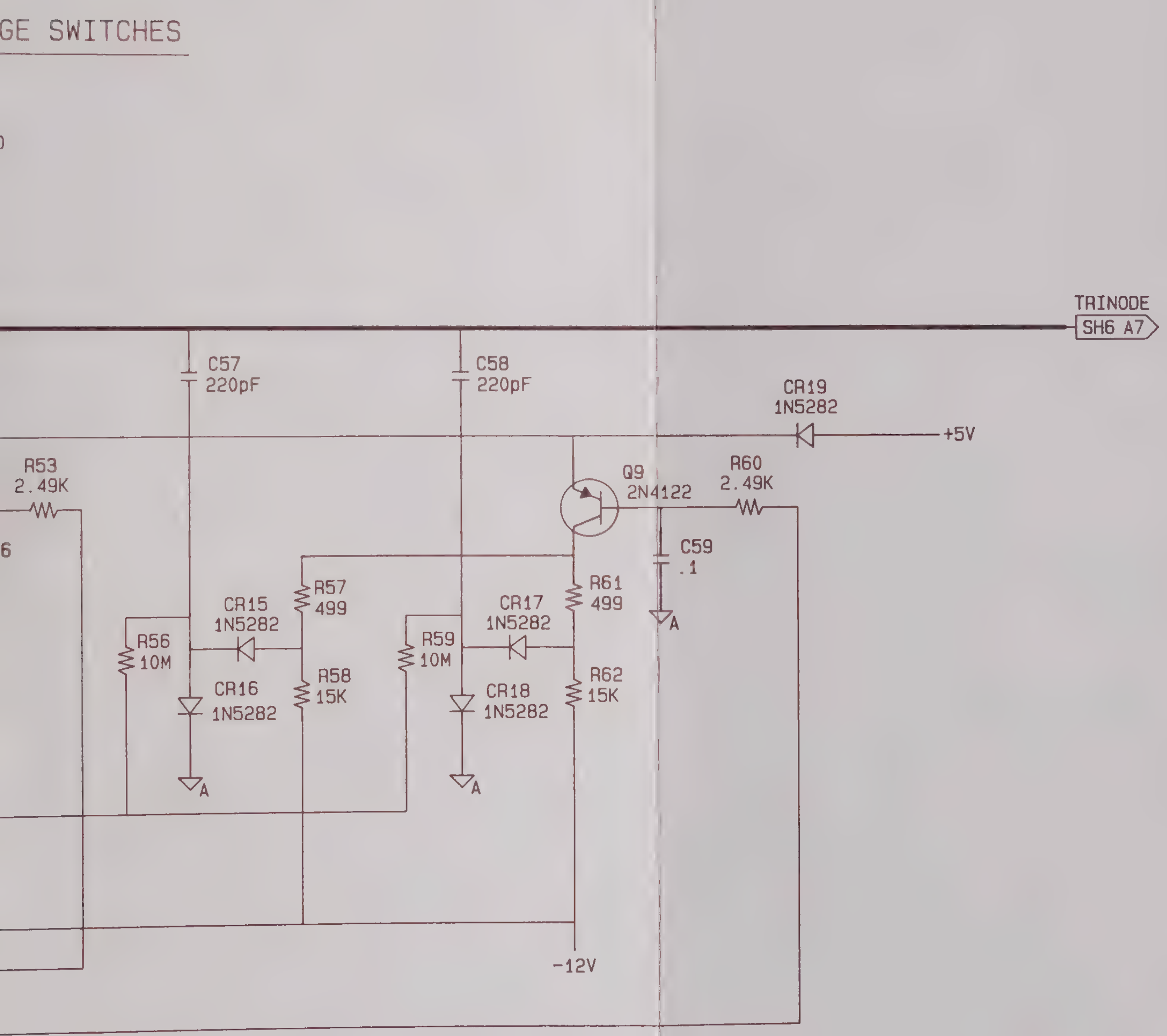
SCALE NONE MODEL 90 SERIES SHEET 3 OF 7

FREQUENCY


TP9
TRINODE
TRINODE
SH7 C1
SH4 D5
+5V
K2
HDIE-DC5V
CR11
1N5282
C52
.47
1%
+5V
K3
HDIE-DC5V
CR12
1N5282
C53
.047
1%
C55
.0047
1%
R49
4.99K
Q8
2N4
R54
90.9
CR13
1N5282
R50
10M
CR14
1N5282
R55
15K
C54
.1
R51
7.5K
R52
33.2K
A
_<FR5
SH1 B2
_<FR6
SH1 B2
_<FR7
SH1 B2
_<FR8
SH1 B2

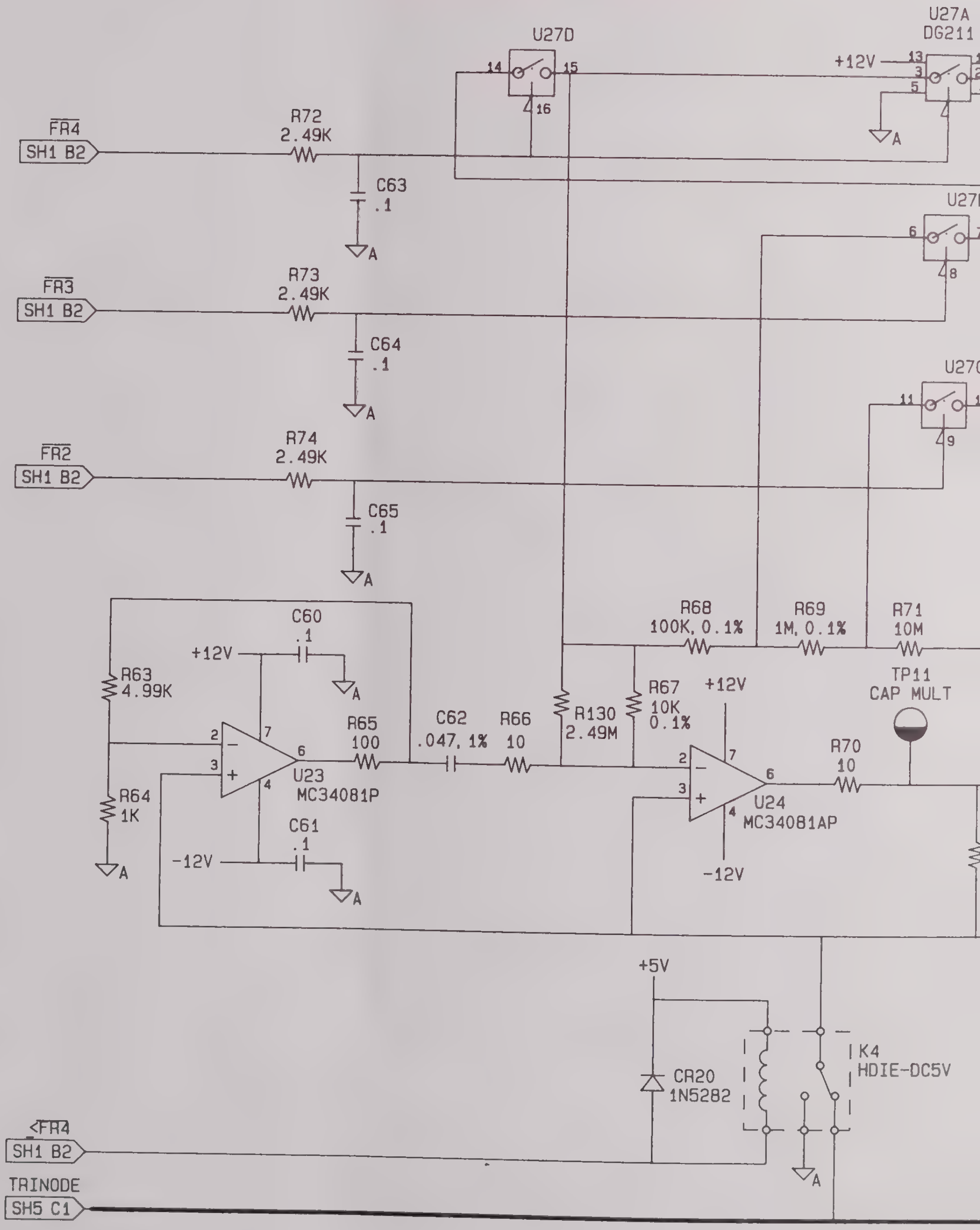
NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


GE SWITCHES
TRINODE
SH6 A7
C57
220pF
C58
220pF
CR19
1N5282
+5V
R53
2.49K
Q9
2N4122
R60
2.49K
C59
.1
A
R57
499
R61
499
CR15
1N5282
CR17
1N5282
R56
10M
R59
10M
CR16
1N5282
R58
15K
CR18
1N5282
R62
15K
A
A
-12V

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 5-8-90	**WAVETEK** SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE SCHEMATIC, FUNCTION GENERATOR
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3342 · REV A
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES · SHEET 5 OF 7

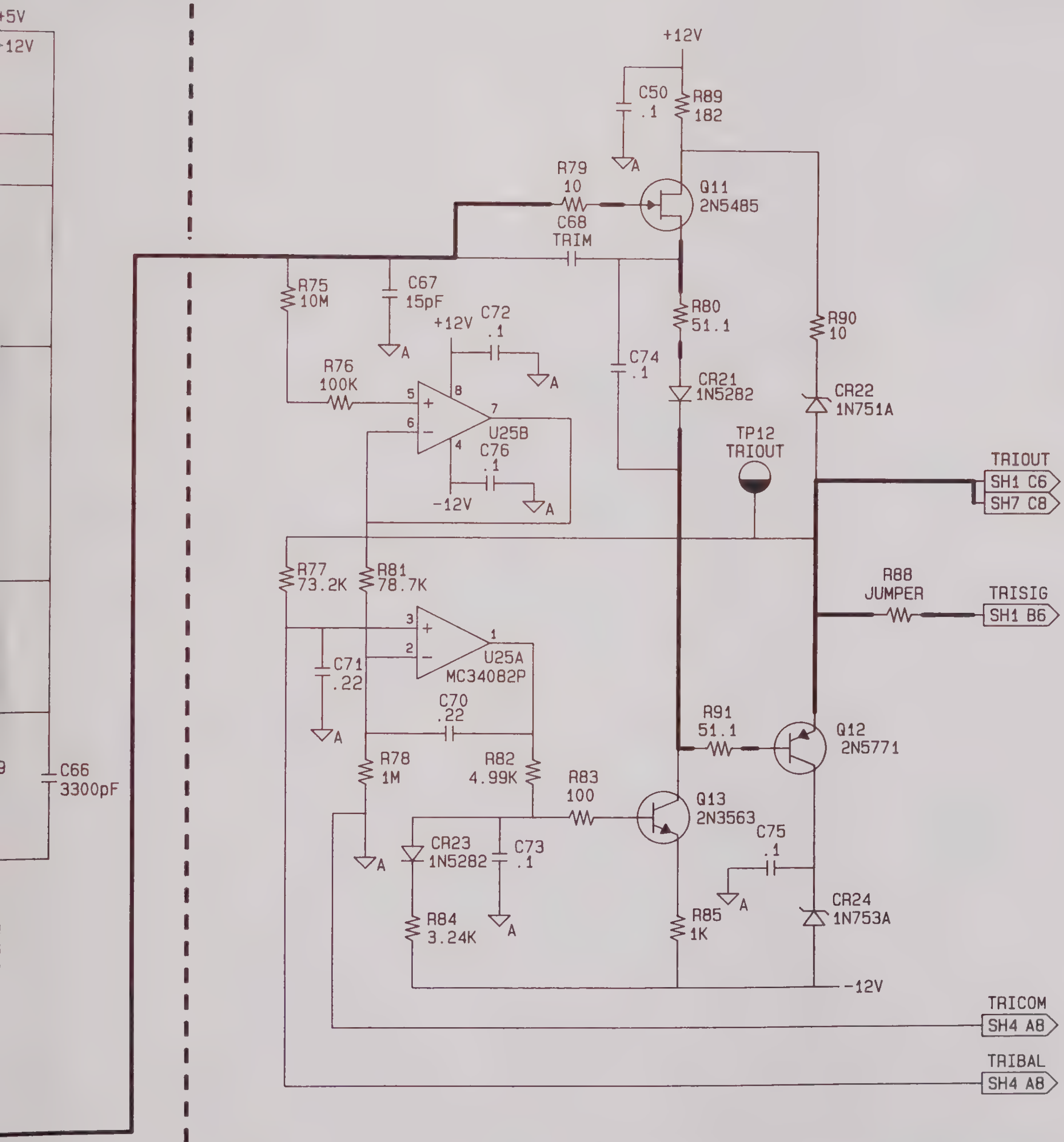
CAPACITANCE MULTIPLIER


U27D
14
15
16
U27A
DG211
+12V
13
3
5
A
FR4
SH1 B2
R72
2.49K
C63
.1
A
U27
6
8
FR3
SH1 B2
R73
2.49K
C64
.1
A
U27C
11
9
FR2
SH1 B2
R74
2.49K
C65
.1
A
C60
.1
+12V
A
R63
4.99K
R64
1K
A
2
3
7
6
4
U23
MC34081P
R65
100
C62
.047, 1%
R66
10
-12V
C61
.1
A
R130
2.49M
R67
10K
0.1%
R68
100K, 0.1%
R69
1M, 0.1%
R71
10M
TP11
CAP MULT
+12V
2
3
7
6
4
U24
MC34081AP
-12V
R70
10
+5V
CR20
1N5282
K4
HDIE-DC5V
A
FR4
SH1 B2
TRINODE
SH5 C1

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

TRIANGLE BUFFER


+5V
+12V
C66
3300pF
+12V
C50
.1
R89
182
A
R79
10
Q11
2N5485
C68
TRIM
R75
10M
C67
15pF
A
+12V
C72
.1
A
R80
51.1
R90
10
R76
100K
5
8
+
-
6
7
U25B
4
C76
.1
-12V
A
C74
.1
CR21
1N5282
CR22
1N751A
TP12
TRIOUT
TRIOUT
SH1 C6
SH7 C8
R77
73.2K
R81
78.7K
R88
JUMPER
TRISIG
SH1 B6
3
2
1
U25A
MC34082P
C71
.22
A
C70
.22
R91
51.1
Q12
2N5771
R78
1M
R82
4.99K
R83
100
Q13
2N3563
C75
.1
A
CR23
1N5282
C73
.1
A
R84
3.24K
A
R85
1K
CR24
1N753A
-12V
TRICOM
SH4 A8
TRIBAL
SH4 A8

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

DRAWN A. TALMADGE DATE 5-6-90
CHECKED
PROJ. ENGR.
RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

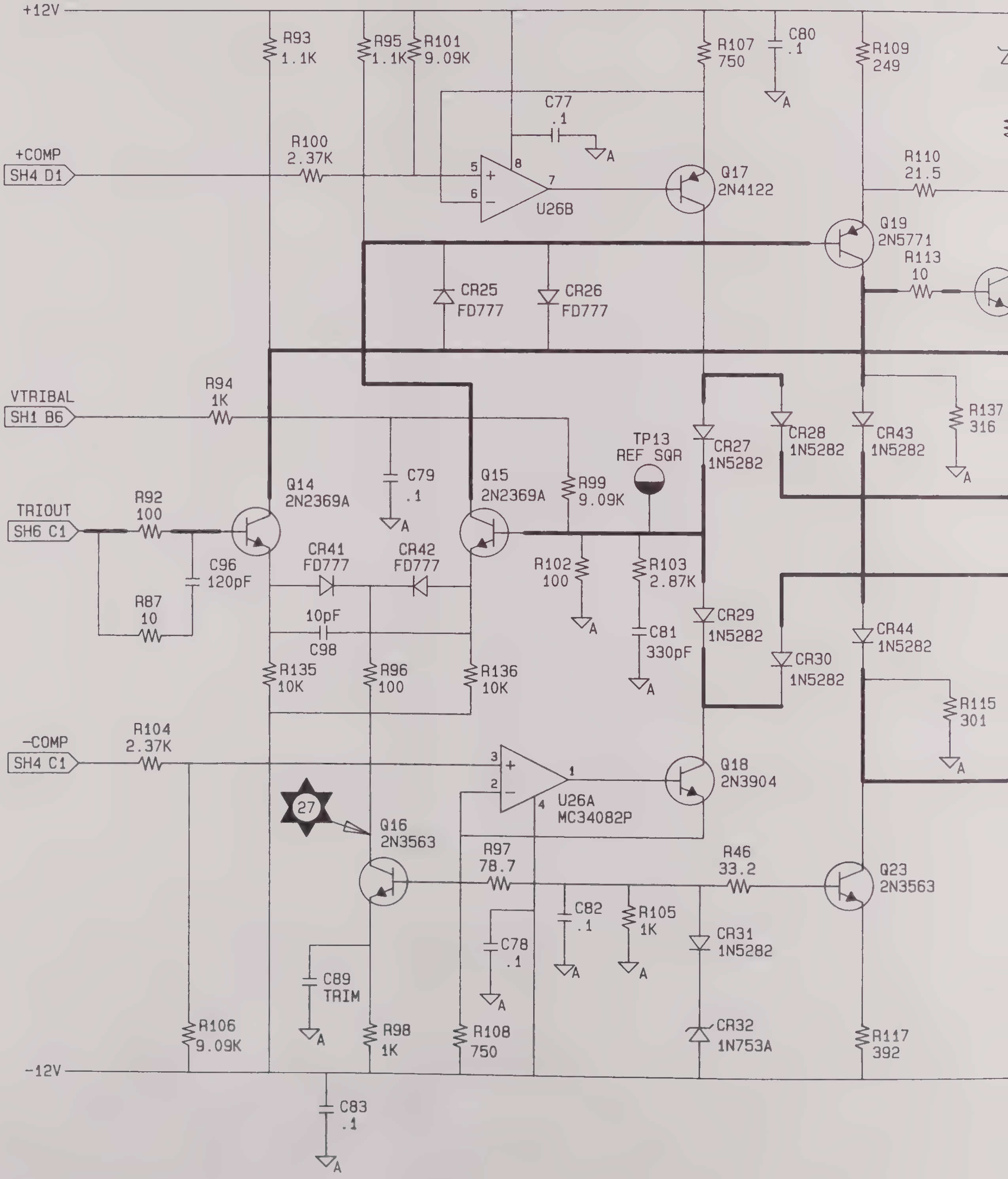
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
FUNCTION GENERATOR

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3342	A

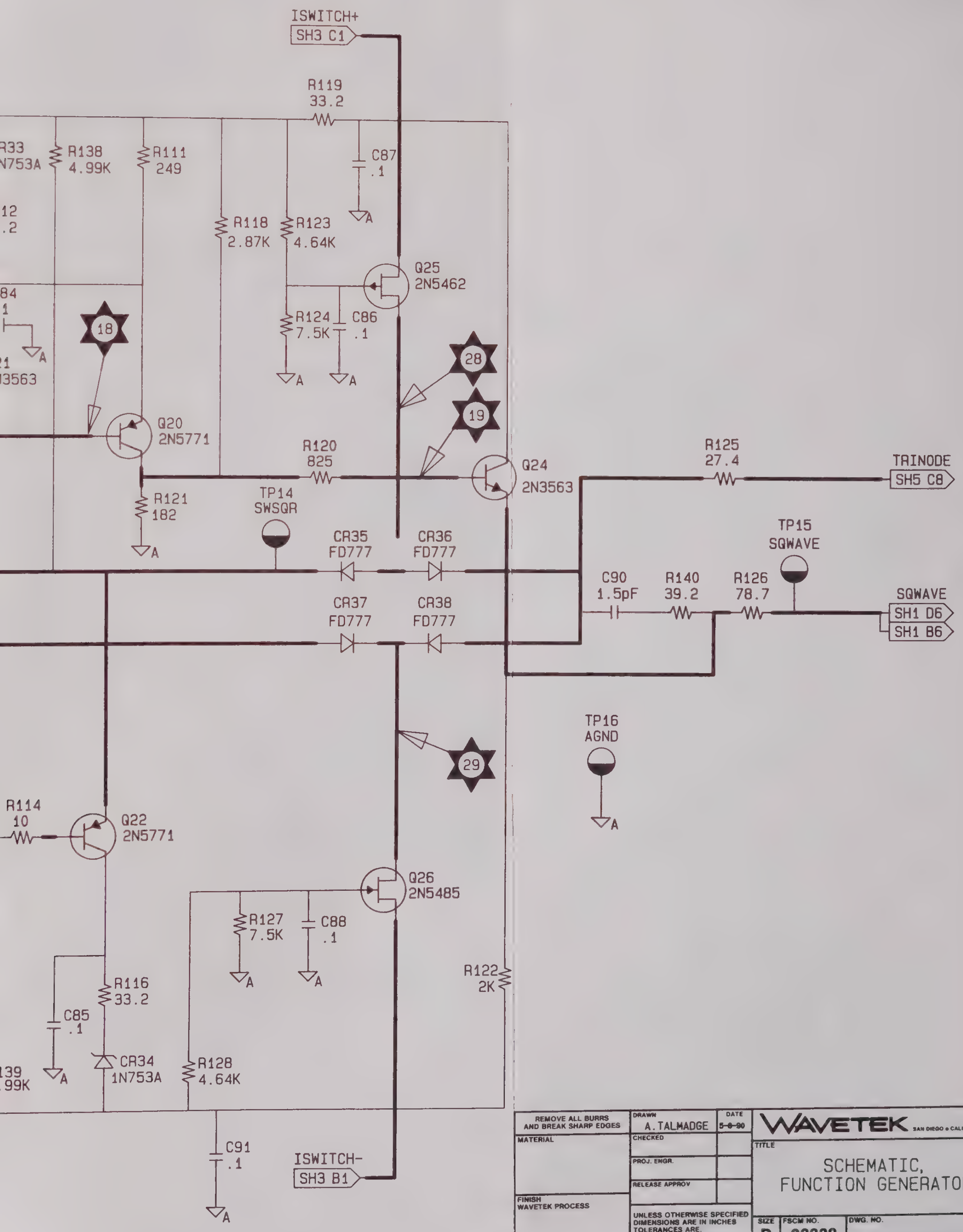
SCALE NONE MODEL 90 SERIES SHEET 6 OF 7

COMPARATOR


+12V
R93 1.1K
R95 1.1K
R101 9.09K
R107 750
C80 .1
R109 249
C77 .1
+COMP SH4 D1
R100 2.37K
U26B
Q17 2N4122
R110 21.5
Q19 2N5771
R113 10
CR25 FD777
CR26 FD777
VTRIBAL SH1 B6
R94 1K
CR27 1N5282
CR28 1N5282
CR43 1N5282
R137 316
TP13 REF SQR
C79 .1
Q14 2N2369A
Q15 2N2369A
R99 9.09K
TRIOUT SH6 C1
R92 100
C96 120pF
R87 10
CR41 FD777
CR42 FD777
R102 100
R103 2.87K
CR29 1N5282
CR30 1N5282
CR44 1N5282
10pF C98
C81 330pF
R135 10K
R96 100
R136 10K
R115 301
-COMP SH4 C1
R104 2.37K
U26A MC34082P
Q18 2N3904
27
Q16 2N3563
R97 78.7
R46 33.2
Q23 2N3563
C82 .1
R105 1K
CR31 1N5282
C78 .1
C89 TRIM
R106 9.09K
R98 1K
R108 750
CR32 1N753A
R117 392
-12V
C83 .1
A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


ISWITCH+
SH3 C1
R119
33.2
C87
.1
R33
N753A
R138
4.99K
R111
249
12
.2
R118
2.87K
R123
4.64K
Q25
2N5462
84
1
R124
7.5K
C86
.1
18
28
21
3563
19
Q20
2N5771
R120
825
Q24
2N3563
R125
27.4
TRINODE
SH5 C8
R121
182
TP14
SWSQR
CR35
FD777
CR36
FD777
TP15
SQWAVE
C90
1.5pF
R140
39.2
R126
78.7
SQWAVE
SH1 D6
SH1 B6
CR37
FD777
CR38
FD777
TP16
AGND
29
R114
10
Q22
2N5771
Q26
2N5485
R127
7.5K
C88
.1
R122
2K
R116
33.2
C85
.1
139
99K
CR34
1N753A
R128
4.64K
C91
.1
ISWITCH-
SH3 B1
A

REMOVE ALL BURRS
AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN A. TALMADGE
DATE 5-8-90
CHECKED
PROJ. ENGR.
RELEASE APPROV

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE.

FRACTIONS	DECIMALS	ANGLES
±	.XX ± .XXX ±	±

WAVETEK SAN DIEGO • CALIFORNIA

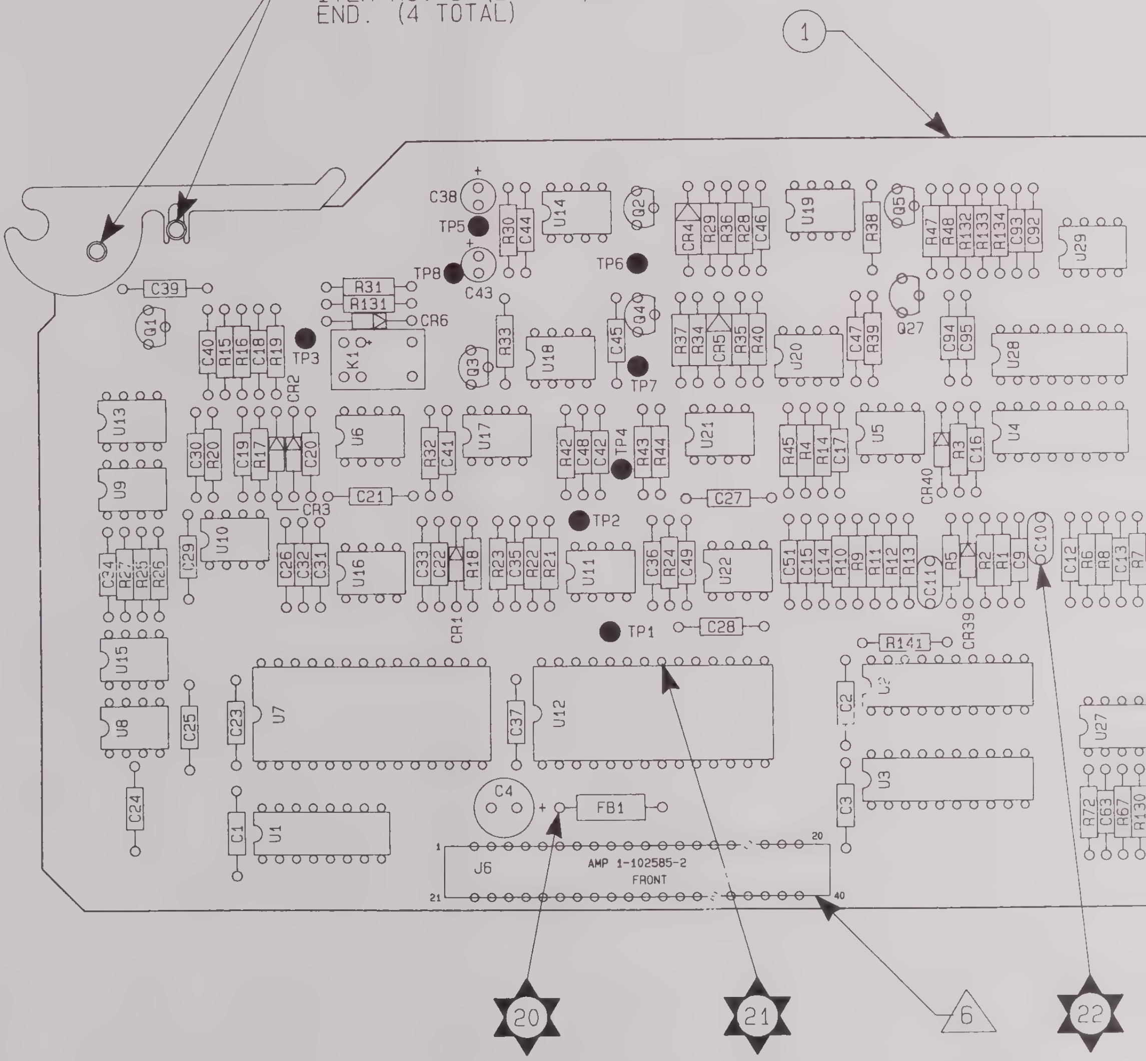
TITLE

SCHEMATIC,
FUNCTION GENERATOR

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3342	A

SCALE NONE
MODEL 90 SERIES
SHEET 7 OF 7

ROLL PINS SUPPLIED WITH ITEM NO. 2 (2 PLCS) EACH END. (4 TOTAL)


8
7
6
5
D
C
B
A
1
C38
TP5
TP8
C43
R30
C44
U14
Q2
TP6
CR4
R29
R36
R28
C46
U19
R38
Q5
R47
R48
R132
R133
R134
C93
C92
U29
C39
R31
R131
CR6
Q1
C40
R15
R16
C18
R19
TP3
K1
CR2
Q3
R33
U18
C45
Q4
TP7
R37
R34
CR5
R35
R40
U20
C47
R39
Q27
C94
C95
U28
U13
C30
R20
C19
R17
C20
U6
R32
C41
U17
R42
C48
C42
TP4
R43
R44
U21
R45
R4
R14
C17
U5
CR40
R3
C16
U4
U9
C21
CR3
C27
C29
U10
C26
C32
C31
U16
C33
C22
R18
CR1
R23
C35
R22
R21
TP2
U11
C36
R24
C49
U22
C51
C15
C14
R10
R9
R11
R12
R13
C11
CR39
R5
R2
R1
C9
C10
C12
R6
R8
C13
R7
C34
R27
R25
R26
TP1
C28
R141
U15
U8
C25
C23
U7
C37
U12
C2
U2
U27
C24
C1
U1
C4
FB1
C3
U3
R72
C63
R67
R130
1
20
J6
AMP 1-102585-2
FRONT
21
40
20
21
6
22

7. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.

△6 MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

5. * = TRIM.

4. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.

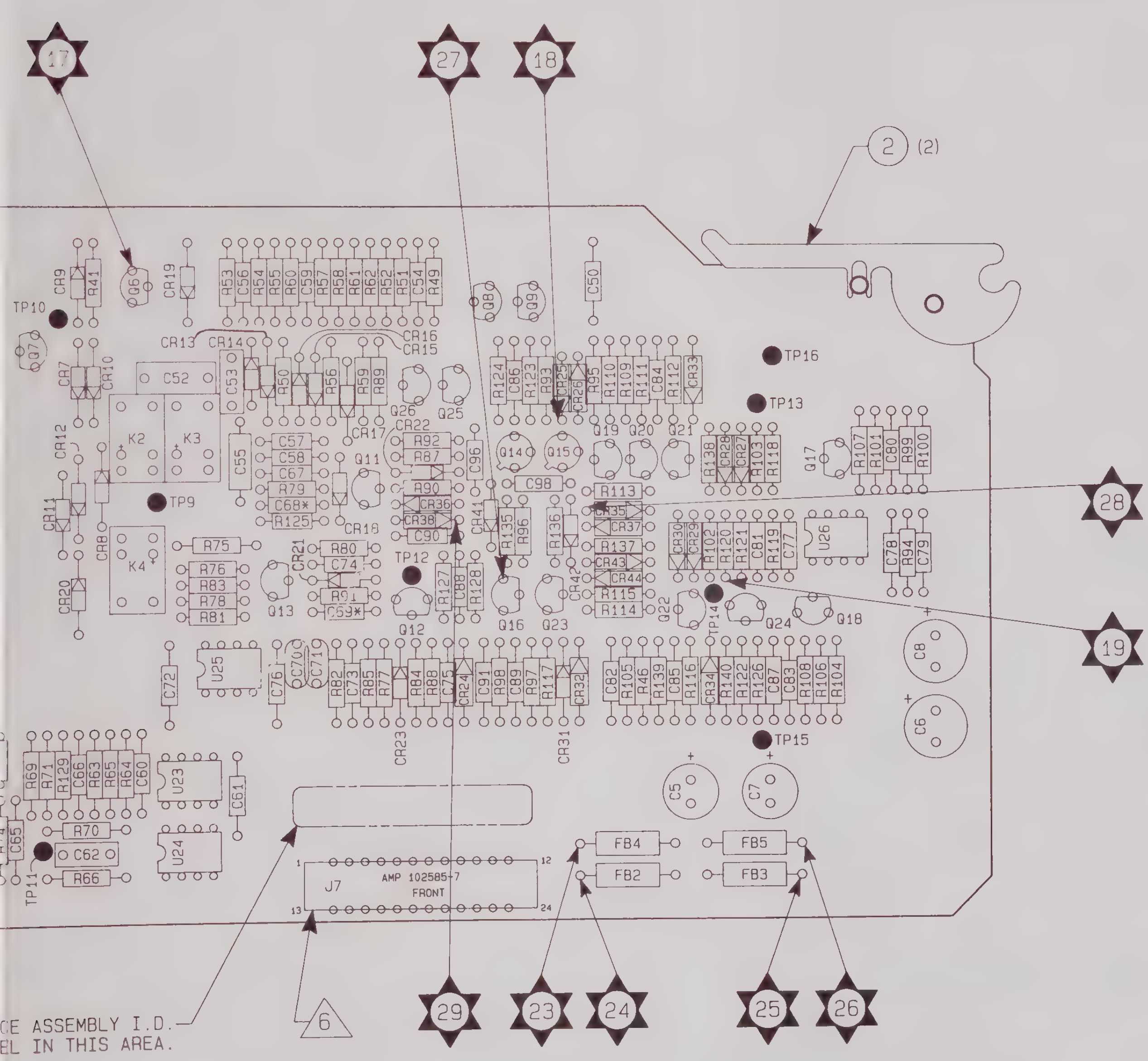
3. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

1. SEE 1104-00-3342 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ERO NO 50-441	AD	4/29/90	DEF
B	ECO No. 90-537	JT	8/30/90	MS



17
27
18
2 (2)
28
19
29
23
24
25
26
6
TP10
TP9
TP11
TP12
TP13
TP14
TP15
TP16
K2
K3
K4
Q6
Q7
Q8
Q9
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
U23
U24
U25
U26
C5
C6
C7
C8
C50
C52
C53
C55
C61
C62
C72
C76
R41
R70
R66
R75
R76
R83
R78
R81
R80
C74
R91
C69*
C98
R113
R137
R115
R114
CR35
CR36
CR37
CR38
CR43
CR44
CR9
CR10
CR12
CR13
CR14
CR15
CR16
CR17
CR18
CR19
CR20
CR22
CR23
CR31
FB2
FB3
FB4
FB5
J7
AMP 102585-7
FRONT
1
12
13
24

CE ASSEMBLY I.D.
EL IN THIS AREA.

CAD JOB #: B065C

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

		DATE
DRAWN	Amy Talmadge	6/20/90
CHECKED	D. Fish	4/29/90
PROJ. ENGR.	D. Fish	4/29/90
RELEASE APPROV.	D. Fish	6/29/90

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PCA, FUNCTION
GENERATOR BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1101-00-3342	B

SCALE 2/1 MODEL 90 SERIES SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONA	A/D, PCA, FUNCTION GENERATOR	1101-00-3342	WVTK	1101-00-3342	1
NONE	S/D, PCA, FUNCTION GENERATOR	1104-00-3342	WVTK	1104-00-3342	1
CR1 CR24 CR32 CR33 CR34	SL ZR 6.2V 5% 400MW (1N753A)	1N753A	ROHM	131.9620	5
C98	CAP, CER, 10PF, 100V, AXIAL	CAC02C0G100J100A	CORNG	1500-01-0006	1
C17	CAP, CER, 100PF, 100V, AXIAL	CAC02C0G101J100A	CORNG	1500-01-0106	1
C1 C12 C13 C14 C15 C16 C18 C2 C20 C21 C22 C23 C25 C27 C28 C3 C31 C33 C37 C39 C40 C41 C42 C44 C45 C46 C47 C48 C50 C54 C56 C59 C60 C61 C63 C64 C65 C72 C73 C74 C75 C76 C77 C78 C79 C80 C82 C83 C84 C85 C86 C87 C88 C9 C91 C92 C93 C94 C95	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	59
C96	CAP, CER, 120PF, 100V, 5%, AXIAL	CAC02C0G121J100A	CORNG	1500-01-2106	1
C67	CAP, CER, 15PF, 100V, AXIAL	CAC02C0G150J100A	CORNG	1500-01-5006	1
C90	CAP, CER, 1.5PF, 200V, AXIAL	SA102A1R5DAA	AVX	1500-01-5906	1

WAVETEK
PARTS LIST
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PCA, FUNCTION GENERATOR
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REV
D

REFERENCE DESIGNATORS	PART DESCRIPTION
C52	CAP, MYLR, .47MF, 50V
NONE	PCB, FUNCTION GENERATOR BD
J7	CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT
J6	CONN, HEADER, 40 PIN, RECPT, 2X20, .1 PCMT
TP1 TP10 TP16	TEST POINT, BLK, PC
TP11 TP12 TP13 TP14 TP15 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9	TEST POINT, RED, PC
NONE	PC BD EJECTOR
FB1 FB2 FB3 FB4 FB5	BALUN CORE, FERRITE, 680
K1 K2 K3 K4	RELAY, 1 FORMC, 5V, .312H, .29
R25 R26 R30 R31 R32 R33 R67	RES, MF, 1/8W, .1%, 10
R68	RES, MF, 1/8W, .1%, 10
R69	RES, MFLM, 1/8W, 0.1%

WAVETEK
PARTS LIST
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PCA, FUNCTION GENERATOR

C

B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C29 C30 C32 C34	CAP, CER, 22PF, 100V, AXIAL	CAC02C0G220J100A	CORNG	1500-02-2006	4
C57 C58	CAP, CER, 220PF, 100V, AXIAL	CAC02C0G221J100A	CORNG	1500-02-2106	2
C10 C70 C71	CAP, CER, .22MF, 25V	CW30C224K	CRL	1500-02-2409	3
C19 C81	CAP, CER, 330PF, 100V, AXIAL	CAC02C0G331J100A	CORNG	1500-03-3106	2
C11 C66	CAP, CER, 3300PF, 100V, 20%, AXIAL	CAC02X7R332M100A	CORNG	1500-03-3206	2
C35 C36 C49 C51	CAP, CER, 47PF, 100V, AXIAL	CAC02C0G470J100A	CORNG	1500-04-7006	4
C55	CAP, CER, 4700PF, 50V, 2%	592CC0G472G050E	SPRAG	1500-04-7213	1
C24 C26	CAP, CER, 680PF, 100V, AXIAL	CAC02C0G681J100A	CORNG	1500-06-8106	2
C6 C8	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	2
C4 C5 C7	CAP, ELECT, 100MF, 25V, RADIAL LEAD-SP SIZE	NRE101M25V6.3X11	NIC	1500-31-0122	3
C38 C43	CAP, ELECT, 22MF, 25V, RADIAL	SRA25VB22RM6X7LL	UNCON	1500-32-2002	2
C53 C62	CAP, MYLR, .047MF, 50V	C5R473F	ELPAC	1500-44-7303	2

WAVETEK
PARTS LIST
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PAGE 2
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D

REFERENCE DESIGNATORS	PART DESCRIPTION
	OM
R36 R37	RES, MF, 1/8W, .1%, 1.
R102 R65 R83 R92 R96	RES, MF, 1/8W, 1%, 100
R105 R64 R85 R94 R98	RES, MF, 1/8W, 1%, 1K
R135 R136 R28 R3 R35 R38 R39 R41 R47 R5	RES, MF, 1/8W, 1%, 10K
R11 R12 R131 R48 R76	RES, MF, 1/8W, 1%, 100
R78	RES, MF, 1/8W, 1%, 1M
R21 R23 R50 R56 R59 R71 R75	RES, MF, 1/4W, 10M, 1%
R113 R114 R29 R34 R66 R70 R79 R87 R90	RES, MF, 1/8W, 1%, 10
R93 R95	RES, MF, 1/8W, 1%, 1.1
R141	RES, MF, 1/8W, 1%, 11K
R55 R58 R62	RES, MF, 1/8W, 1%, 15K
R121 R89	RES, MF, 1/8W, 1%, 182
R122	RES, MF, 1/8W, 1%, 2K
R42 R44	RES, MF, 1/8W, 1%, 20K
R110	RES, MF, 1/8W, 1%, 21

WAVETEK
PARTS LIST
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PCA, FUNCTION GENERATOR

A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

IG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R474F	ELPAC	1500-44-7403	1
00-00-3342	WVTK	1700-00-3342	1
2585-7	AMP	2100-02-0255	1
102585-2	AMP	2100-02-0256	1
-104-01-00	COMPO	2100-04-0054	3
-104-01-02	COMPO	2100-04-0055	13
-2-C	BRIT	2800-07-0032	2
3666671	FARIT	3100-00-0017	5
E-M-DC5V	AROMT	4500-00-0034	4
5E-1002B	MEPCO	4701-02-1002	7
5E-1003B	MEPCO	4701-02-1003	1
-55-1004BT-9	DALE	4701-02-1004	1

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O-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
5E-1501B	CORNG	4701-02-1501	2
5D-1000F	TRW	4701-03-1000	5
5D-1001F	TRW	4701-03-1001	5
5D-1002F	TRW	4701-03-1002	10
5D-1003F	TRW	4701-03-1003	5
5D-1004F	TRW	4701-03-1004	1
3YD10M000F	MEPCO	4701-03-1005	7
3ED10R100F	MEPCO	4701-03-1009	9
D-1101F	TRW	4701-03-1101	2
D-1102F	TRW	4701-03-1102	1
D-1502F	TRW	4701-03-1502	3
D-1820F	TRW	4701-03-1820	2
D-2001F	TRW	4701-03-2001	1
D-2002F	TRW	4701-03-2002	2
D-21R5F	TRW	4701-03-2159	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R109 R111	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	2
R1 R13 R2 R53 R6 R60 R7 R72 R73 R74	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	10
R130 R22 R24	RES, MFLM, 1/8W, 2.49M, 1%	CMF-552494F T-8	DALE	4701-03-2494	3
R125	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	1
R103 R118	RES, MF, 1/8W, 1%, 2.87K	RN55D-2871F	TRW	4701-03-2871	2
R115	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	1
R43 R45	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	2
R137	RES, MF, 1/8W, 1%, 316	RN55D-3160F	TRW	4701-03-3160	1
R84	RES, MF, 1/8W, 1%, 3.24K	RN55D-3241F	TRW	4701-03-3241	1
R100 R104	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	2
R52	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	1
R112 R116 R119 R46	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	4
R117	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R140	RES, MF, 1/8W, 1%, 39.2	RN55D-39R2F	TRW	4701-03-3929	1
R10 R14 R9	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	3

WAVETEK
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R123 R128	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	2
R129 R18 R57 R61	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	4
R134 R138 R139 R20 R27 R49 R63 R82	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	8
R132 R17	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	2
R133	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	1
R80 R91	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	2
R19	RES, MF, 1/8W, 1%, 604	RN55D-6040F	TRW	4701-03-6040	1
R107 R108	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	2
R40	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	1
R124 R127 R16 R51	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	4
R81	RES, MF, 1/8W, 1%, 78.7K	RN55D-7872F	TRW	4701-03-7872	1
R126 R97	RES, MF, 1/8W, 1%, 78.7	RN55D-78R7F	TRW	4701-03-7879	2
R101 R106 R4	RES, MF, 1/8W, 1%, 8.06K	RN55D-8061F	TRW	4701-03-8061	3
R120	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	1
R15 R99	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	2
R54	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	1

WAVETEK
PARTS LIST

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PCA, FUNCTION GENERATOR

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REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE
	PROJ. ENGR.		PARTS LIST
	RELEASE APPROV.		FUNCTION GENERATOR
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3342 · REV D
DO NOT SCALE DRAWING			SCALE · MODEL 95 · SHEET 1 OF 2

D

REFERENCE DESIGNATORS	PART DESCRIPTION
R88	RES, 0 OHM JUMPER
R77 R8	RES, MFLM, 1/8W, 1%, 73.2 K
CR4 CR5	DIODE, ZENER, 3.3V, 5% TOL, 500MW, G/B, IN746A
CR22	DIODE, ZENOR, 5.1V, 500MW, GIB, IN751A
CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR2 CR20 CR21 CR23 CR27 CR28 CR29 CR3 CR30 CR31 CR39 CR40 CR43 CR44 CR6 CR9	DIODE, HIGH CONDUCTANCE, ULTRA FAST
CR25 CR26 CR35 CR36 CR37 CR38 CR7 CR8	DIODE, ULTRA FAST
CR41 CR42	DIODE, SET, 2-FD-777 QTY: 2: 4807-02-0777
Q14 Q15	TRANS, SILICON, PLANAR, EPITAXIAL, NPN, TO-18
Q13 Q16 Q21 Q23 Q24	TRANS, NPN, TO-92
Q18 Q27 Q6	TRANS 2N3904 NPN GENERAL PURPOSE TO-92
Q17 Q8 Q9	TRANS, GENERAL

WAVETEK
PARTS LIST

TITLE
PCA, FUNCTION GENERATOR

C

B

A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

FGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
90	ROHM	4799-00-0087	1
7322F	MEPCO	4799-00-0234	2
	FAIR	4801-01-0746	2
	FAIR	4801-01-0751	1
	FAIR	4801-01-5282	26
	T/CSF	4807-02-0777	8
0-0003	KLG	4898-00-0003	1
A	MOT	4901-02-3691	2
	FAIR	4901-03-5630	5
	FAIR	4901-03-9040	3
	NSC	4901-04-1220	3

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	PURPOSE, PNP, TO-92				
Q25 Q3	TRANS, P-CHANNEL JFETS	2N5462	MOT	4901-05-4620	2
Q1 Q11 Q26	TRANS, N-CHANNEL JFETS	2N5485	MOT	4901-05-4850	3
Q12 Q19 Q20 Q22	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	4
Q4 Q7	TRANS, FET N CHANNEL	VN0106N3	SUPER	4902-01-0600	2
Q2 Q5	TRANS, FET P CHANNEL	VP0106N3	SUPER	4902-01-0601	2
U28	MUX, CMOS, D 4C, 8 CHAN/DUAL 4 CHAN ANAL	DG508ACJ	SLCON	7000-05-0800	1
U13 U14 U17 U18	OP AMP, LOW DRIFT, LOW OFFSET	LT1001CN8	LINTE	7000-10-0180	4
U12 U7	DAC, QUAD 8 BIT, MULT W/MEM, CMOS	DAC8408GP	PMI	7000-84-0800	2
U10 U15 U16 U19 U20 U23 U9	OP AMP, HI SLEW RTE, WIDEBND, JFET, STD	MC34081P	MOT	7003-40-8100	7
U24 U5 U8	OP AMP, HI SLEW RTE, WIDEBND, JFET, PRIME	MC34081AP	MOT	7003-40-8101	3
U11 U21 U22 U25 U26 U29 U6	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	7

WAVETEK
PARTS LIST
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U27 U4	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	2
U1	DECODER/DEMUX, 3 TO 8 LINE	SN74ALS138N	TI	8007-41-3800	1
U2 U3	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	2

WAVETEK
PARTS LIST
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PCA, FUNCTION GENERATOR
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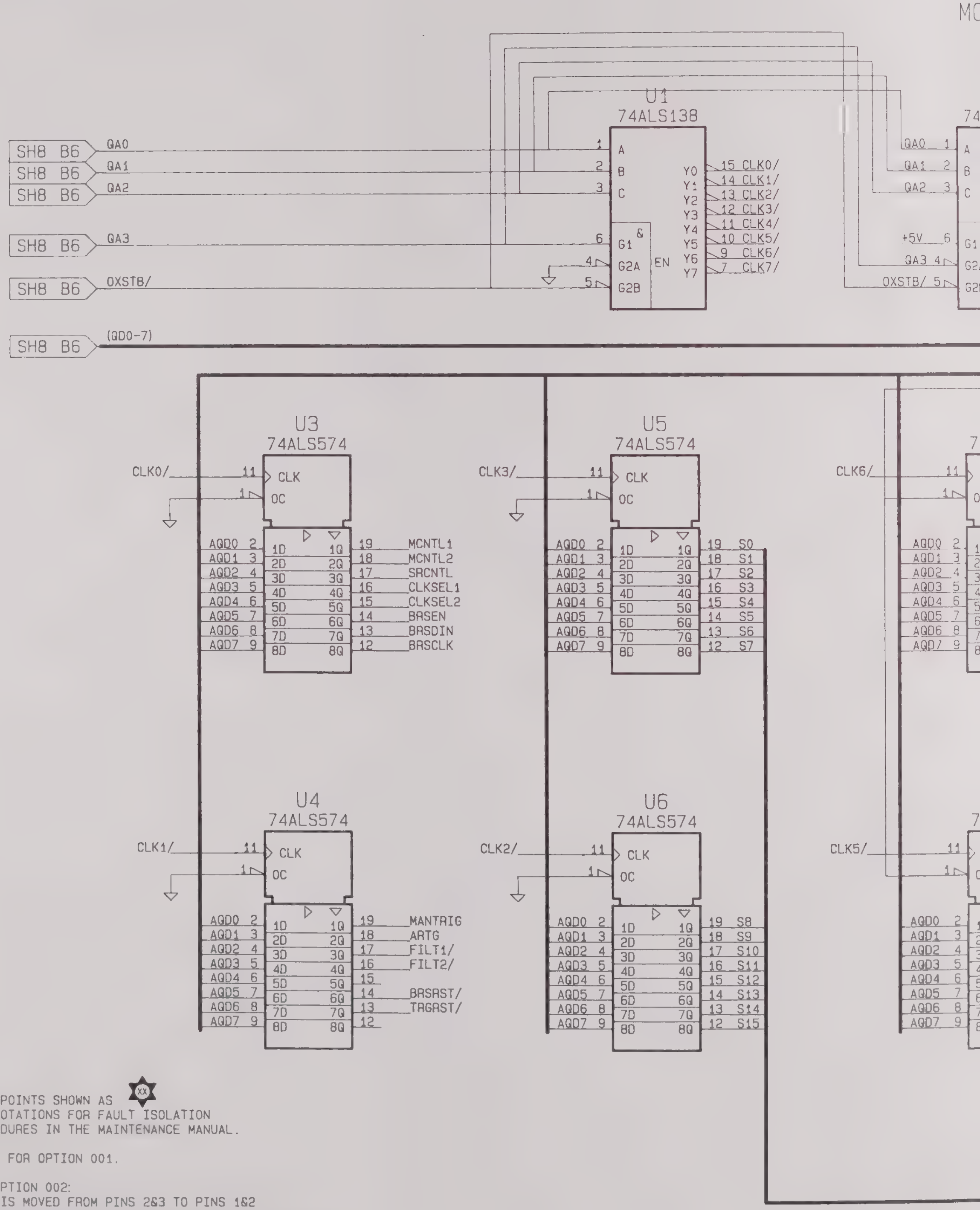
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	CHECKED		TITLE PARTS LIST FUNCTION GENERATOR	
	PROJ. ENGR.			
	RELEASE APPROV.			
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES . .XX ± ± XXX ±		SIZE D · FSCM NO. 23338 · DWG NO. 1100-00-3342	REV D
DO NOT SCALE DRAWING			SCALE · MODEL 95 · SHEET 2 OF 2	



MC
U1
74ALS138
SH8 B6 QA0
SH8 B6 QA1
SH8 B6 QA2
SH8 B6 QA3
SH8 B6 OXSTB/
SH8 B6 (QD0-7)
A B C G1 G2A G2B & EN
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
15 CLK0/
14 CLK1/
13 CLK2/
12 CLK3/
11 CLK4/
10 CLK5/
9 CLK6/
7 CLK7/
74
QA0 1 A
QA1 2 B
QA2 3 C
+5V 6 G1
QA3 4 G2
OXSTB/ 5 G2
U3
74ALS574
CLK0/
CLK OC
AQD0 2 1D 1Q 19 MCNTL1
AQD1 3 2D 2Q 18 MCNTL2
AQD2 4 3D 3Q 17 SRCNTL
AQD3 5 4D 4Q 16 CLKSEL1
AQD4 6 5D 5Q 15 CLKSEL2
AQD5 7 6D 6Q 14 BRSEN
AQD6 8 7D 7Q 13 BRSDIN
AQD7 9 8D 8Q 12 BRSCLK
U5
74ALS574
CLK3/
19 S0
18 S1
17 S2
16 S3
15 S4
14 S5
13 S6
12 S7
CLK6/
U4
74ALS574
CLK1/
19 MANTRIG
18 ARTG
17 FILT1/
16 FILT2/
15
14 BRSRST/
13 TRGRST/
12
U6
74ALS574
CLK2/
19 S8
18 S9
17 S10
16 S11
15 S12
14 S13
13 S14
12 S15
CLK5/

6. TEST POINTS SHOWN AS ✡ ARE NOTATIONS FOR FAULT ISOLATION PROCEDURES IN THE MAINTENANCE MANUAL.

5. ADDED FOR OPTION 001.

4. FOR OPTION 002:
JMP1 IS MOVED FROM PINS 2&3 TO PINS 1&2
U16, U18 ARE CHANGED FROM 8KX8 SRAM TO 32KX8 SRAM
U17, U19 ARE CHANGED FROM 32KX8 SRAM TO 128KX8 SRAM
Q11, CR10, BT2, R64 ARE ADDED
JMP2 IS REMOVED

3. RESISTORS VALUED IN OHMS, 1/8W.

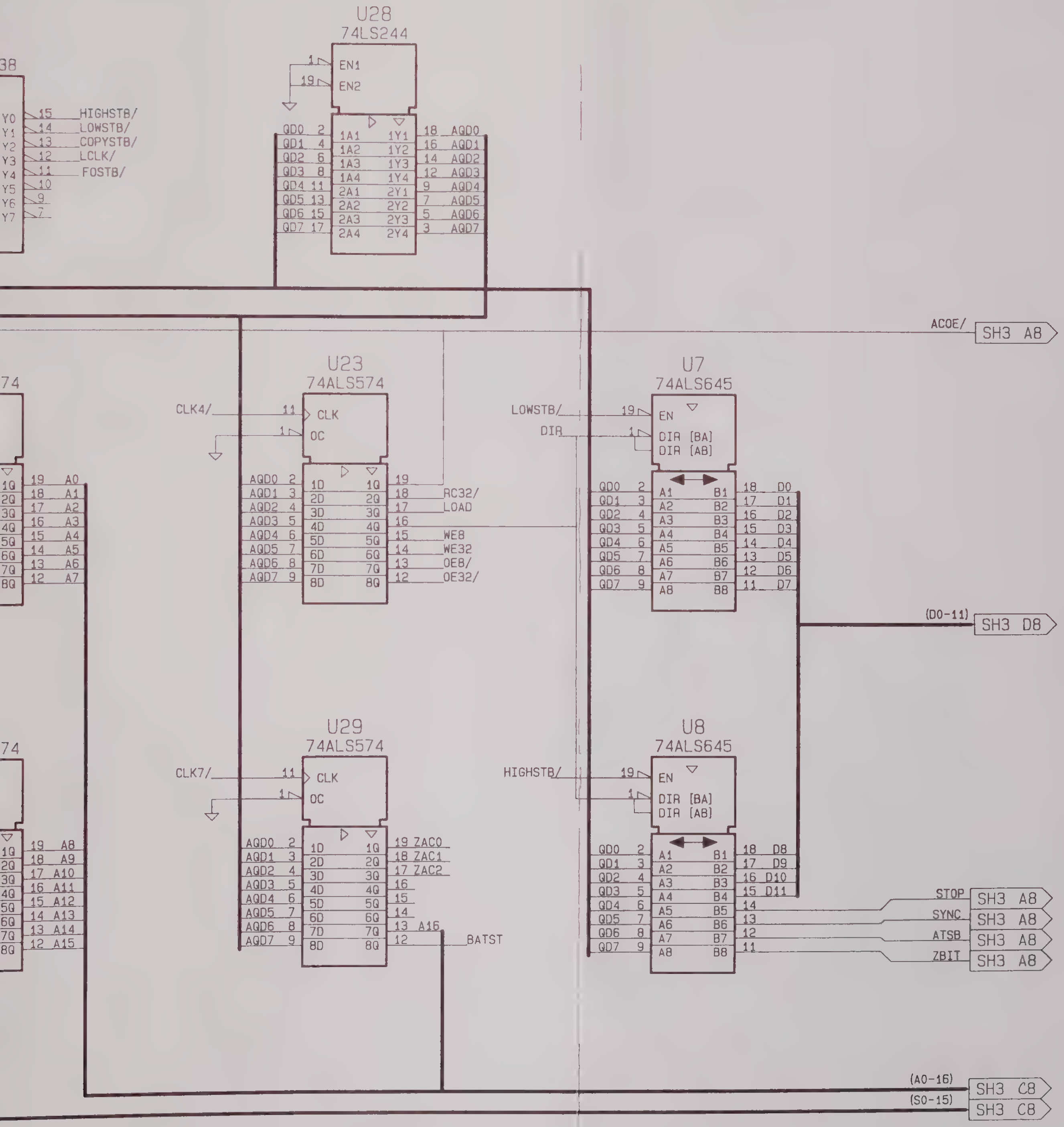
2. CAPACITORS VALUED IN MICROFARADS (uF).

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0599.

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ECO# 90-441		6/29/90	GF

AND ARB CONTROL I/O

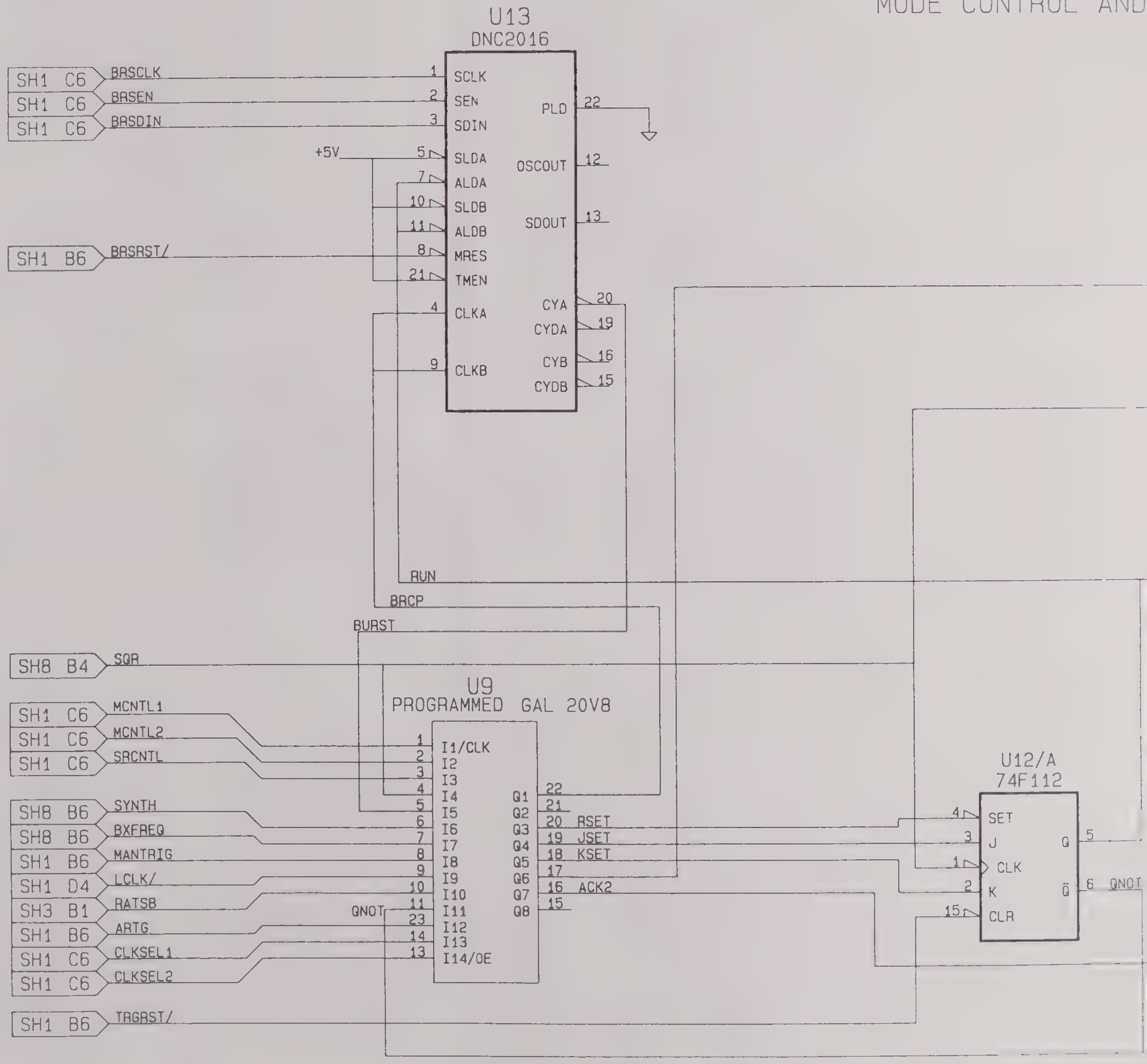


38
Y0 15 HIGHSTB/
Y1 14 LOWSTB/
Y2 13 COPYSTB/
Y3 12 LCLK/
Y4 11 FOSTB/
Y5 10
Y6 9
Y7 7
U28
74LS244
EN1
EN2
QD0 QD1 QD2 QD3 QD4 QD5 QD6 QD7
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4
1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4
AQD0 AQD1 AQD2 AQD3 AQD4 AQD5 AQD6 AQD7
ACOE/
SH3 A8
74
1Q 19 A0
2Q 18 A1
3Q 17 A2
4Q 16 A3
5Q 15 A4
6Q 14 A5
7Q 13 A6
8Q 12 A7
U23
74ALS574
CLK4/
CLK
OC
1D 2D 3D 4D 5D 6D 7D 8D
19 1Q
18 2Q RC32/
17 3Q LOAD
16 4Q
15 5Q WE8
14 6Q WE32
13 7Q OE8/
12 8Q OE32/
U7
74ALS645
LOWSTB/
DIR
EN
DIR [BA]
DIR [AB]
A1 A2 A3 A4 A5 A6 A7 A8
B1 D0
B2 D1
B3 D2
B4 D3
B5 D4
B6 D5
B7 D6
B8 D7
(D0-11)
SH3 D8
74
1Q 19 A8
2Q 18 A9
3Q 17 A10
4Q 16 A11
5Q 15 A12
6Q 14 A13
7Q 13 A14
8Q 12 A15
U29
74ALS574
CLK7/
CLK
OC
19 ZAC0
18 ZAC1
17 ZAC2
13 A16
12 BATST
U8
74ALS645
HIGHSTB/
EN
DIR [BA]
DIR [AB]
B1 D8
B2 D9
B3 D10
B4 D11
STOP SH3 A8
SYNC SH3 A8
ATSB SH3 A8
ZBIT SH3 A8
(A0-16) SH3 C8
(S0-15) SH3 C8

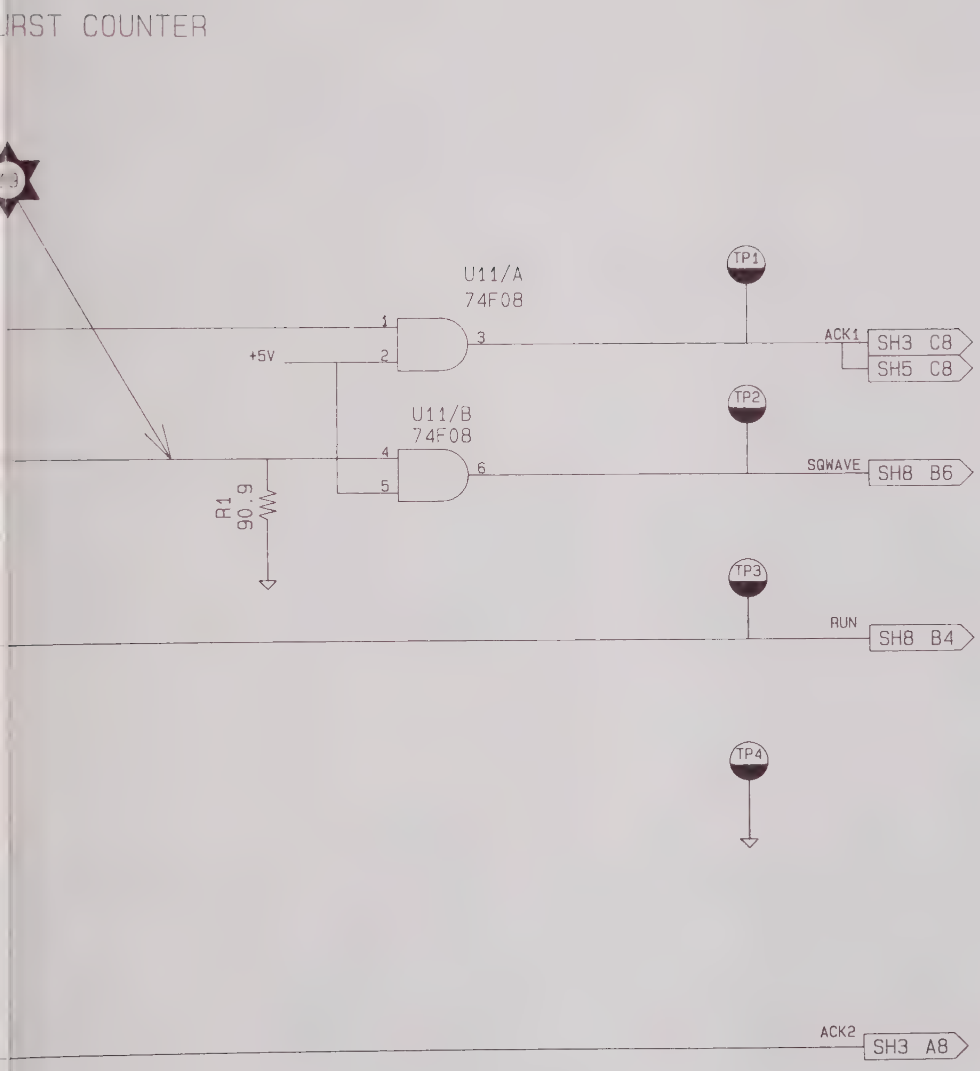
CAD JOB #: B051C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BO FIFER	DATE 6/27/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED D. FISH	6/29/90	TITLE SCHEMATIC, ARB, BOARD
	PROJ. ENGR.	6/29/90	
FINISH WAVETEK PROCESS	RELEASE APPROV	6/29/90	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3327 REV A
DO NOT SCALE DRAWING			SCALE N/A MODEL 90/95 SHEET 1 OF 8

MODE CONTROL AND


U13
DNC2016
SH1 C6
BRSCLK
SH1 C6
BRSEN
SH1 C6
BRSDIN
+5V
SH1 B6
BRSRST/
1 SCLK
2 SEN
3 SDIN
5 SLDA
7 ALDA
10 SLDB
11 ALDB
8 MRES
21 TMEN
4 CLKA
9 CLKB
PLD 22
OSCOUT 12
SDOUT 13
CYA 20
CYDA 19
CYB 16
CYDB 15
RUN
BRCP
BURST
SH8 B4
SQR
U9
PROGRAMMED GAL 20V8
SH1 C6
MCNTL1
SH1 C6
MCNTL2
SH1 C6
SRCNTL
SH8 B6
SYNTH
SH8 B6
BXFREQ
SH1 B6
MANTRIG
SH1 D4
LCLK/
SH3 B1
RATSB
SH1 B6
ARTG
SH1 C6
CLKSEL1
SH1 C6
CLKSEL2
SH1 B6
TRGRST/
QNOT
1 I1/CLK
2 I2
3 I3
4 I4
5 I5
6 I6
7 I7
8 I8
9 I9
10 I10
11 I11
23 I12
14 I13
13 I14/OE
Q1 22
Q2 21
Q3 20 RSET
Q4 19 JSET
Q5 18 KSET
Q6 17
Q7 16 ACK2
Q8 15
U12/A
74F112
4 SET
3 J
1 CLK
2 K
15 CLR
Q 5
Q̄ 6 QNOT

NOTE UNLESS OTHERWISE SPECIFIED

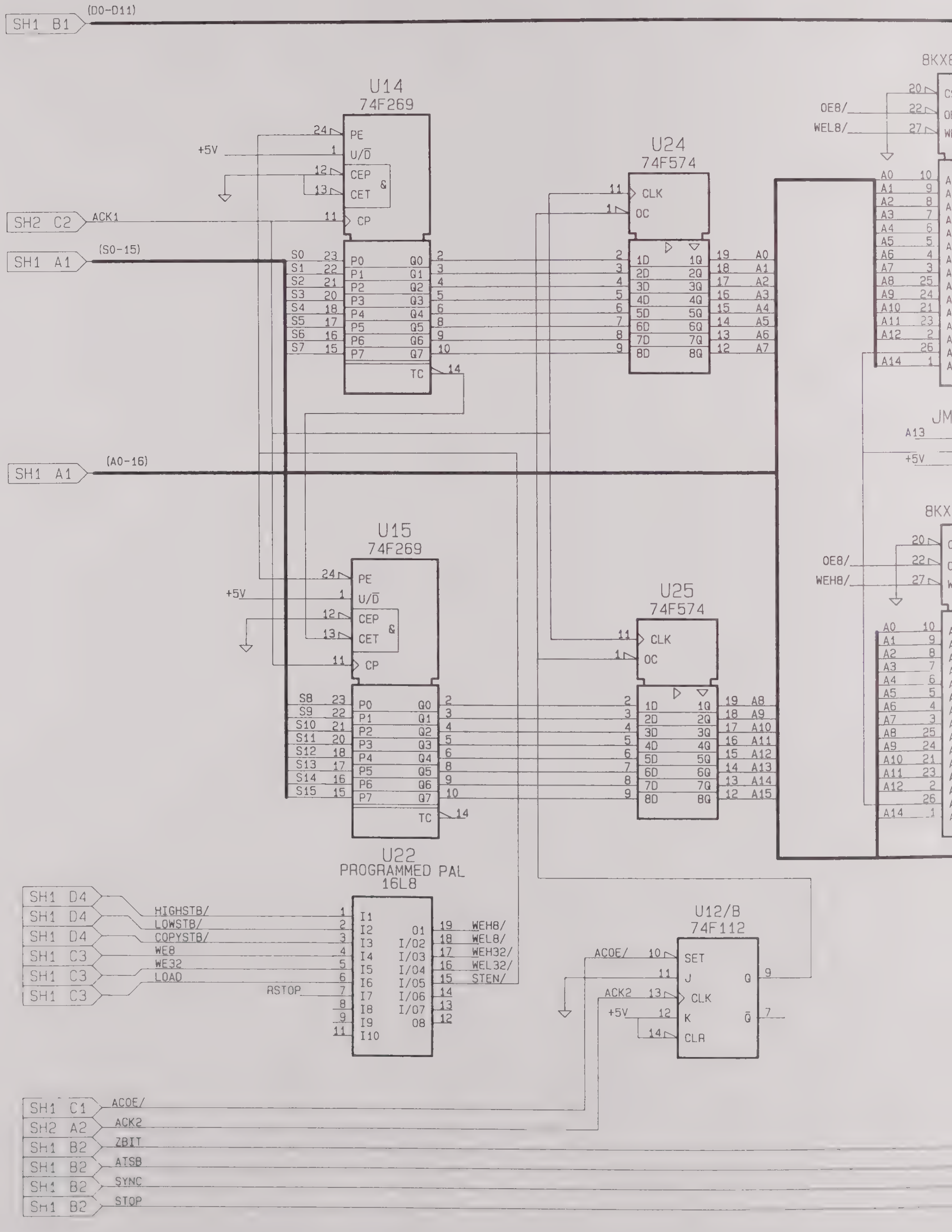

RST COUNTER
U11/A
74F08
1
2
3
+5V
TP1
ACK1
SH3 C8
SH5 C8
U11/B
74F08
4
5
6
TP2
SQWAVE
SH8 B6
R1
90.9
TP3
RUN
SH8 B4
TP4
ACK2
SH3 A8

REV	ECO	BY	DATE	APP

CAD JOB #: B051C

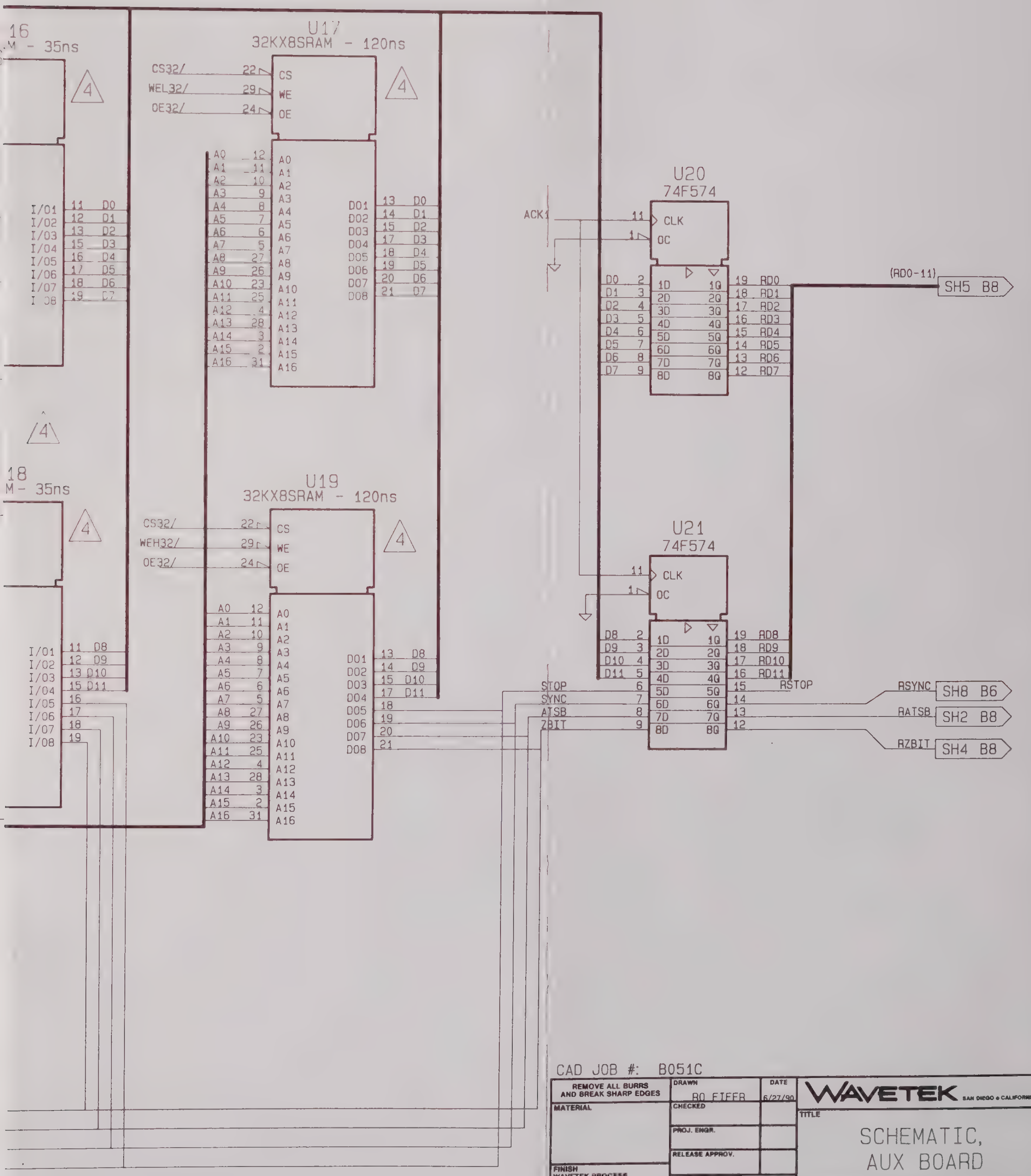
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BO FIFER	DATE 6/27/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE SCHEMATIC, ARB BOARD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO 23338 · DWG. NO. 1104-00-3327 · REV A
DO NOT SCALE DRAWING			SCALE · MODEL 90,75 · SHEET 2 OF 5

ARBRITRARY WAVEFORM ADDRESS AN


SH1 B1
(D0-D11)
SH2 C2
ACK1
SH1 A1
(S0-15)
SH1 A1
(A0-16)
U14
74F269
U15
74F269
PE
U/D
CEP
CET
CP
+5V
P0 P1 P2 P3 P4 P5 P6 P7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
TC
S0 S1 S2 S3 S4 S5 S6 S7
S8 S9 S10 S11 S12 S13 S14 S15
U24
74F574
U25
74F574
CLK
OC
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
A0 A1 A2 A3 A4 A5 A6 A7
A8 A9 A10 A11 A12 A13 A14 A15
8KX8
OE8/
WEL8/
WEH8/
A13
+5V
JM
U22
PROGRAMMED PAL
16L8
SH1 D4
SH1 D4
SH1 D4
SH1 C3
SH1 C3
SH1 C3
HIGHSTB/
LOWSTB/
COPYSTB/
WE8
WE32
LOAD
RSTOP
I1 I2 I3 I4 I5 I6 I7 I8 I9 I10
O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 O8
WEH8/
WEL8/
WEH32/
WEL32/
STEN/
U12/B
74F112
ACOE/
ACK2
SET
J
CLK
K
CLR
Q
Q̄
SH1 C1
SH2 A2
SH1 B2
SH1 B2
SH1 B2
SH1 B2
ACOE/
ACK2
ZBIT
ATSB
SYNC
STOP

NOTE UNLESS OTHERWISE SPECIFIED

DATA GENERATOR

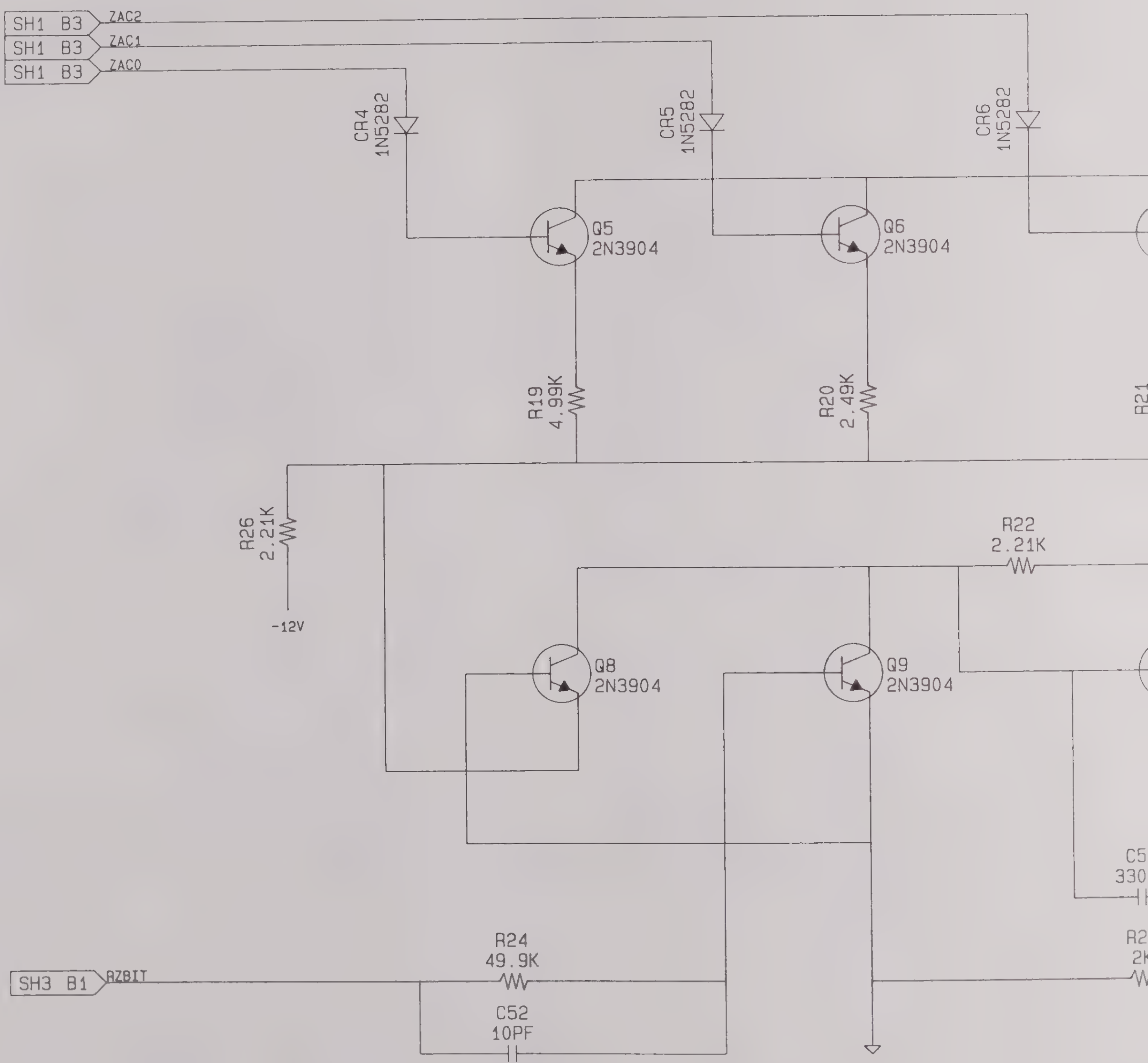

16
M - 35ns
18
M - 35ns
U17
32KX8SRAM - 120ns
U19
32KX8SRAM - 120ns
CS32/
WEL32/
WEH32/
OE32/
CS
WE
OE
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16
I/01 I/02 I/03 I/04 I/05 I/06 I/07 I/08
D01 D02 D03 D04 D05 D06 D07 D08
D0 D1 D2 D3 D4 D5 D6 D7
D8 D9 D10 D11
U20
74F574
U21
74F574
ACK1
CLK
OC
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
RD0 RD1 RD2 RD3 RD4 RD5 RD6 RD7
RD8 RD9 RD10 RD11
(RD0-11)
SH5 B8
STOP
SYNC
ATSB
ZBIT
RSTOP
RSYNC
SH8 B6
RATSB
SH2 B8
RZBIT
SH4 B8
4

CAD JOB #: B051C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BO FIFER	DATE 6/27/90	**WAVETEK** SAN DIEGO • CALIFORNIA	
MATERIAL	CHECKED		TITLE SCHEMATIC, AUX BOARD	
	PROJ. ENGR.			
	RELEASE APPROV.			
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3327 · REV A	
DO NOT SCALE DRAWING			SCALE · MODEL 90/95 · SHEET 3 OF 8	

REV	ECO	BY	DATE	APP

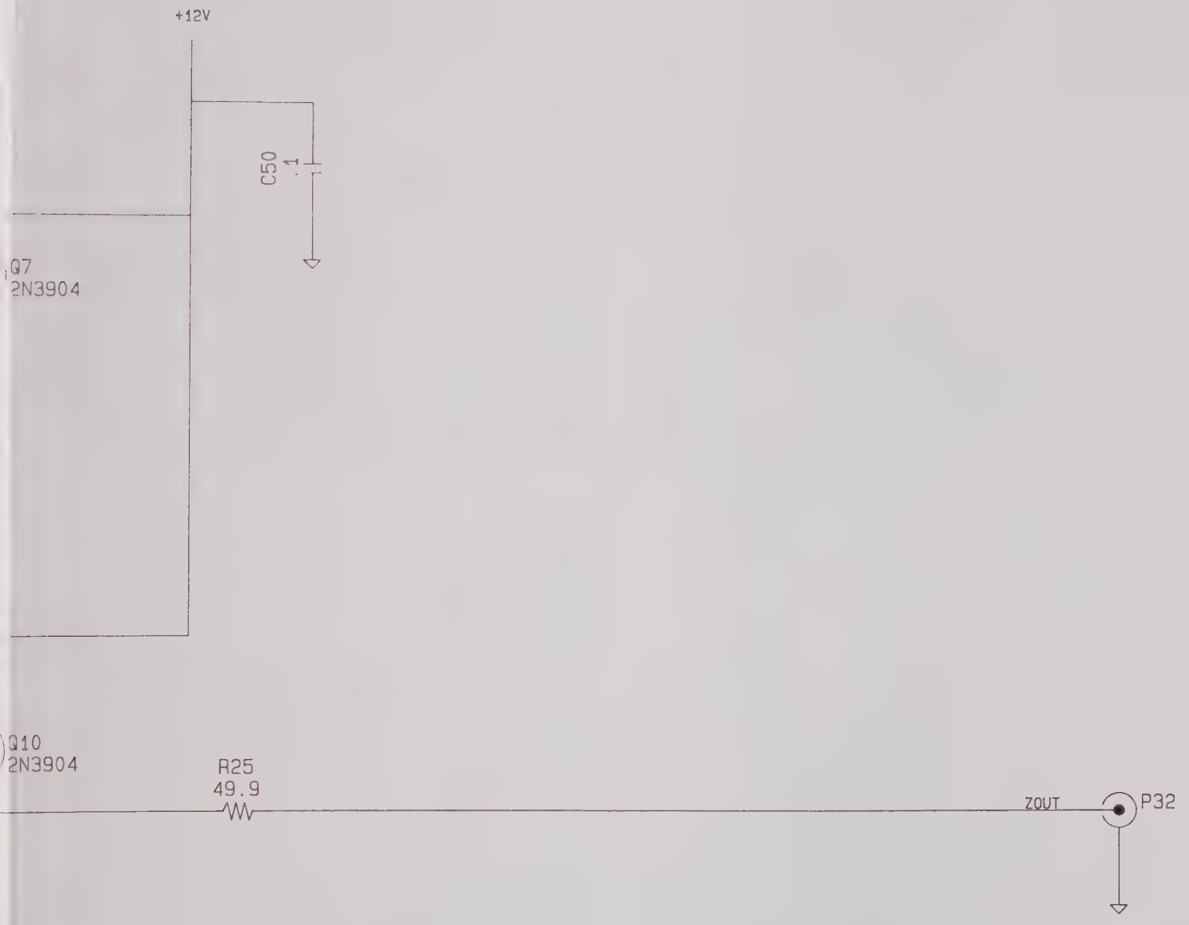
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION


SH1 B3
ZAC2
SH1 B3
ZAC1
SH1 B3
ZAC0
CR4
1N5282
CR5
1N5282
CR6
1N5282
Q5
2N3904
Q6
2N3904
R19
4.99K
R20
2.49K
R21
R26
2.21K
-12V
R22
2.21K
Q8
2N3904
Q9
2N3904
C5
330
R2
2K
SH3 B1
RZBIT
R24
49.9K
C52
10PF

Z AXIS DR

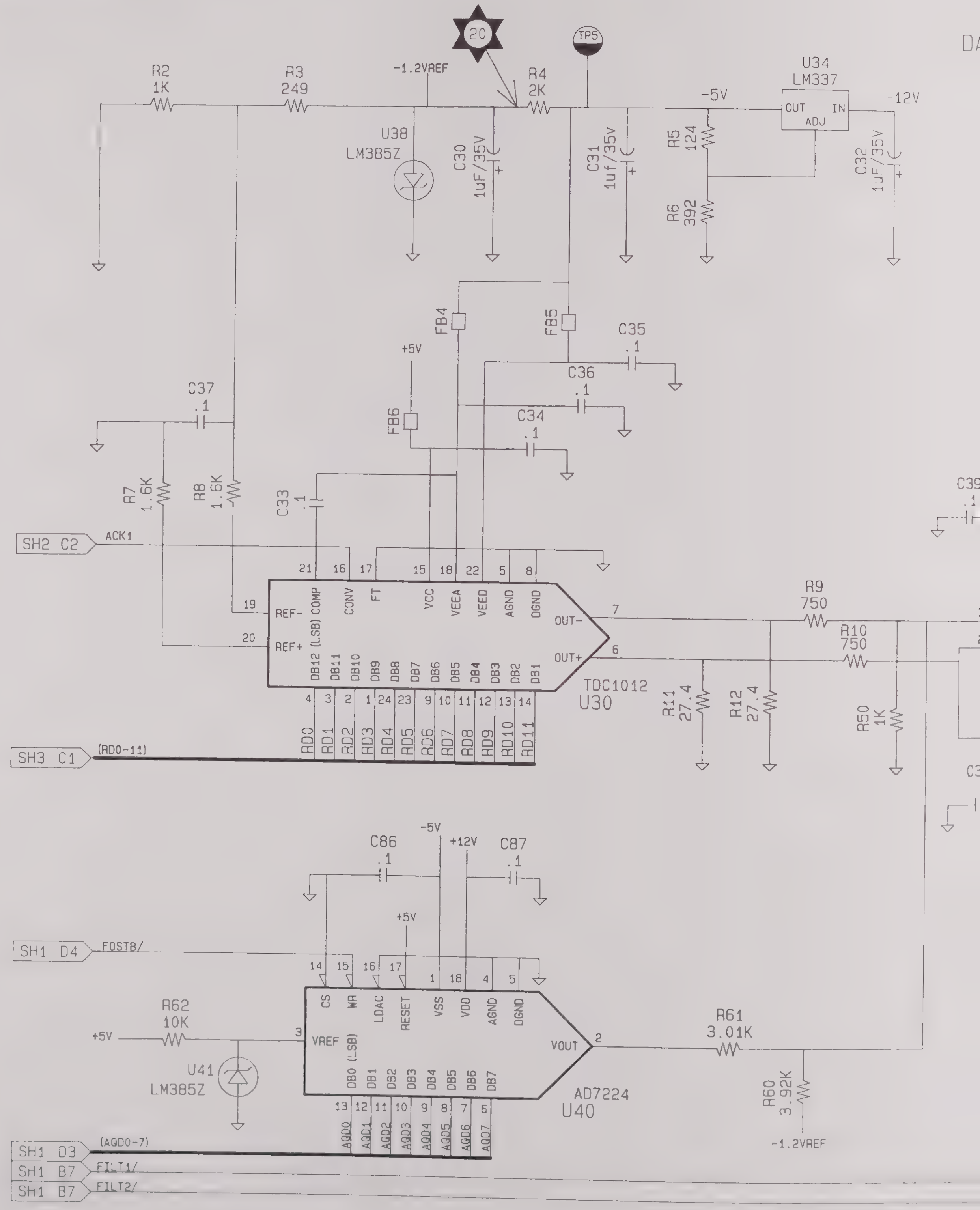
NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


+12V
C50
.1
Q7
2N3904
Q10
2N3904
R25
49.9
ZOUT
P32
R

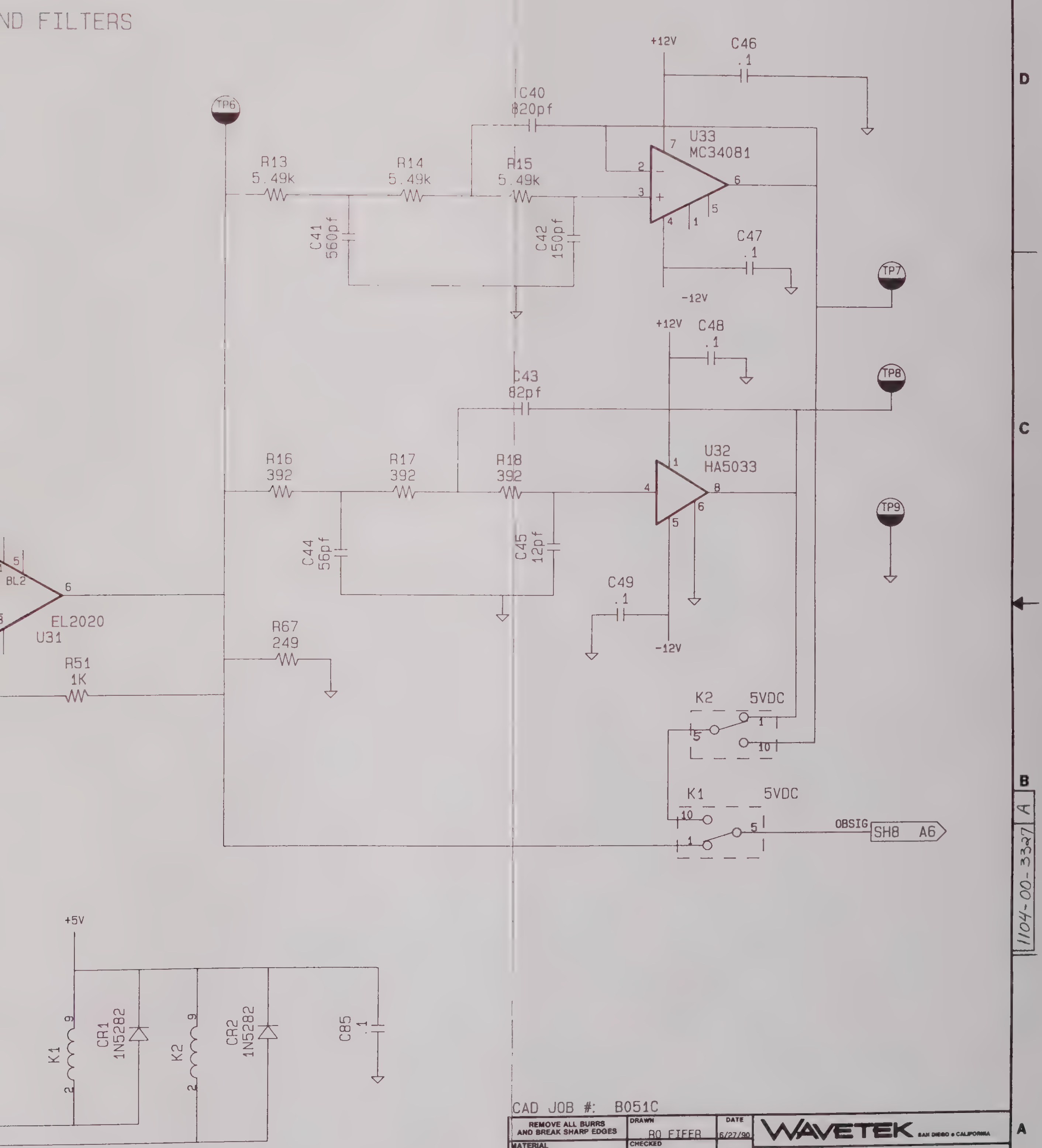
CAD JOB #: B051C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BO FIFER	DATE 6/27/90	**WAVETEK** SAN DIEGO • CALIFORNIA	
MATERIAL	CHECKED		TITLE SCHEMATIC, ARB BOARD	
	PROJ. ENGR.			
	RELEASE APPROV.			
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3327	REV A
DO NOT SCALE DRAWING			SCALE · MODEL 90 · SHEET 4 OF 9	


8
7
6
5
D
C
B
A
20
TP5
DA
R2
1K
R3
249
-1.2VREF
R4
2K
-5V
U34
LM337
OUT
IN
ADJ
-12V
U38
LM385Z
C30
1uF/35V
C31
1uf/35v
R5
124
R6
392
C32
1uF/35V
FB4
FB5
C35
.1
+5V
C36
.1
C34
.1
FB6
C37
.1
R7
1.6K
R8
1.6K
C33
.1
C39
.1
SH2 C2
ACK1
21 16 17 15 18 22 5 8
19
20
REF-
REF+
DB12 (LSB) COMP
CONV
FT
VCC
VEEA
VEED
AGND
DGND
OUT-
OUT+
7
6
DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1
TDC1012
U30
4 3 2 1 24 23 9 10 11 12 13 14
RD0 RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8 RD9 RD10 RD11
SH3 C1
(RD0-11)
R9
750
R10
750
R11
27.4
R12
27.4
R50
1K
C3
-5V
+12V
C86
.1
C87
.1
+5V
SH1 D4
FOSTB/
14 15 16 17 1 18 4 5
CS
WR
LDAC
RESET
VSS
VDD
AGND
DGND
R62
10K
+5V
3
VREF
(LSB)
VOUT
2
U41
LM385Z
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
13 12 11 10 9 8 7 6
AQD0 AQD1 AQD2 AQD3 AQD4 AQD5 AQD6 AQD7
AD7224
U40
R61
3.01K
R60
3.92K
-1.2VREF
SH1 D3
(AQD0-7)
SH1 B7
FILT1/
SH1 B7
FILT2/

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP



ND FILTERS
TP6
R13 5.49k
R14 5.49k
R15 5.49k
C40 820pf
C41 560pf
C42 150pf
+12V
C46 .1
U33 MC34081
7
2
3
6
4
1
5
C47 .1
-12V
TP7
+12V
C48 .1
C43 82pf
TP8
R16 392
R17 392
R18 392
C44 56pf
C45 12pf
U32 HA5033
1
4
8
6
5
TP9
C49 .1
-12V
BL2
5
6
EL2020
U31
R67 249
R51 1K
K2
5VDC
5
1
10
K1
5VDC
10
1
5
OBSIG
SH8 A6
+5V
K1
9
2
CR1 1N5282
K2
9
2
CR2 1N5282
C85 .1

CAD JOB #: B051C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BO FIFER	DATE 6/27/90
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO • CALIFORNIA

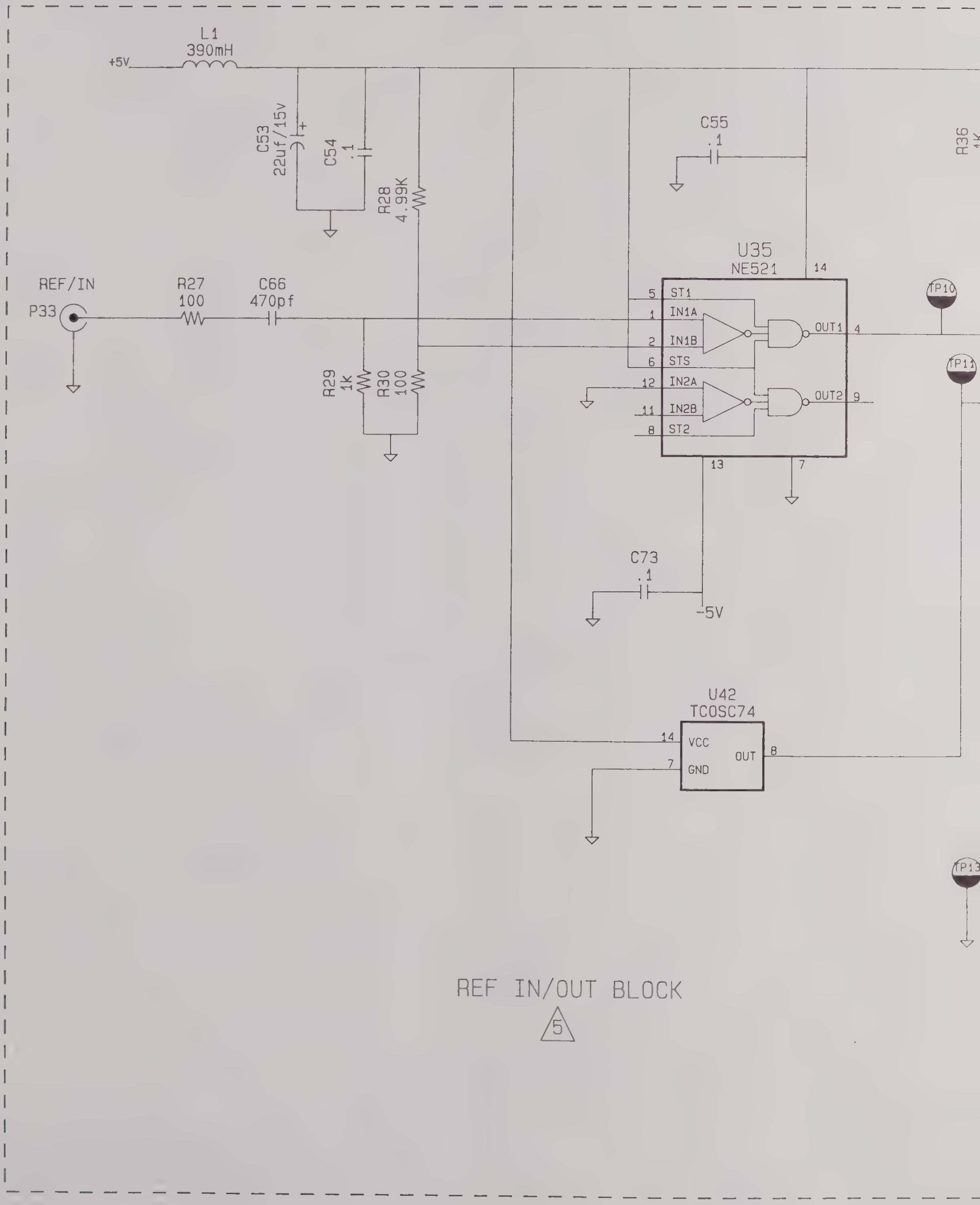
TITLE

SCHEMATIC,
ARB BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3327	A

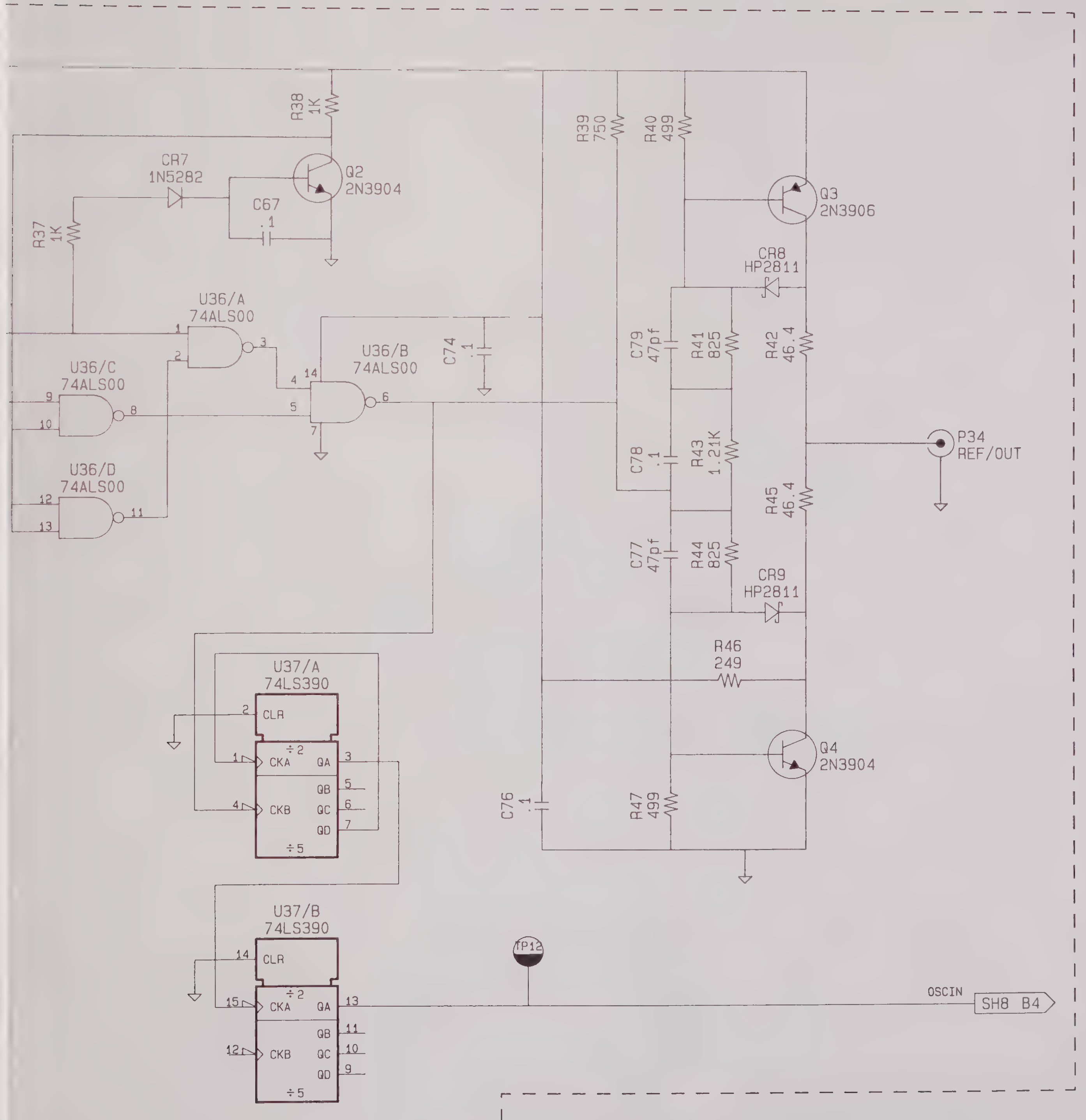
SCALE MODEL 90/95 SHEET 5 OF 8

1104-00-3327 A


L1
390mH
+5V
C53
22uf/15v
C54
.1
R28
4.99K
C55
.1
R36
U35
NE521
14
REF/IN
P33
R27
100
C66
470pf
5 ST1
1 IN1A
2 IN1B
6 STS
12 IN2A
11 IN2B
8 ST2
OUT1 4
OUT2 9
13
7
TP10
TP11
R29
1k
R30
100
C73
.1
-5V
U42
TCOSC74
14 VCC
7 GND
OUT 8
TP13
REF IN/OUT BLOCK
5

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


R38
1K
CR7
1N5282
Q2
2N3904
C67
.1
R37
1K
R39
750
R40
499
Q3
2N3906
CR8
HP2811
U36/A
74ALS00
U36/B
74ALS00
C74
.1
U36/C
74ALS00
U36/D
74ALS00
C79
47pf
R41
825
R42
46.4
C78
.1
R43
1.21K
P34
REF/OUT
R45
46.4
C77
47pf
R44
825
CR9
HP2811
R46
249
U37/A
74LS390
CLR
÷2
CKA
QA
QB
CKB
QC
QD
÷5
Q4
2N3904
C76
.1
R47
499
U37/B
74LS390
TP12
OSCIN
SH8 B4

CAD JOB #: B051C

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

		DATE
DRAWN	BO FIFER	6/27/90
CHECKED		
PROJ. ENGR.		
RELEASE APPROV.		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

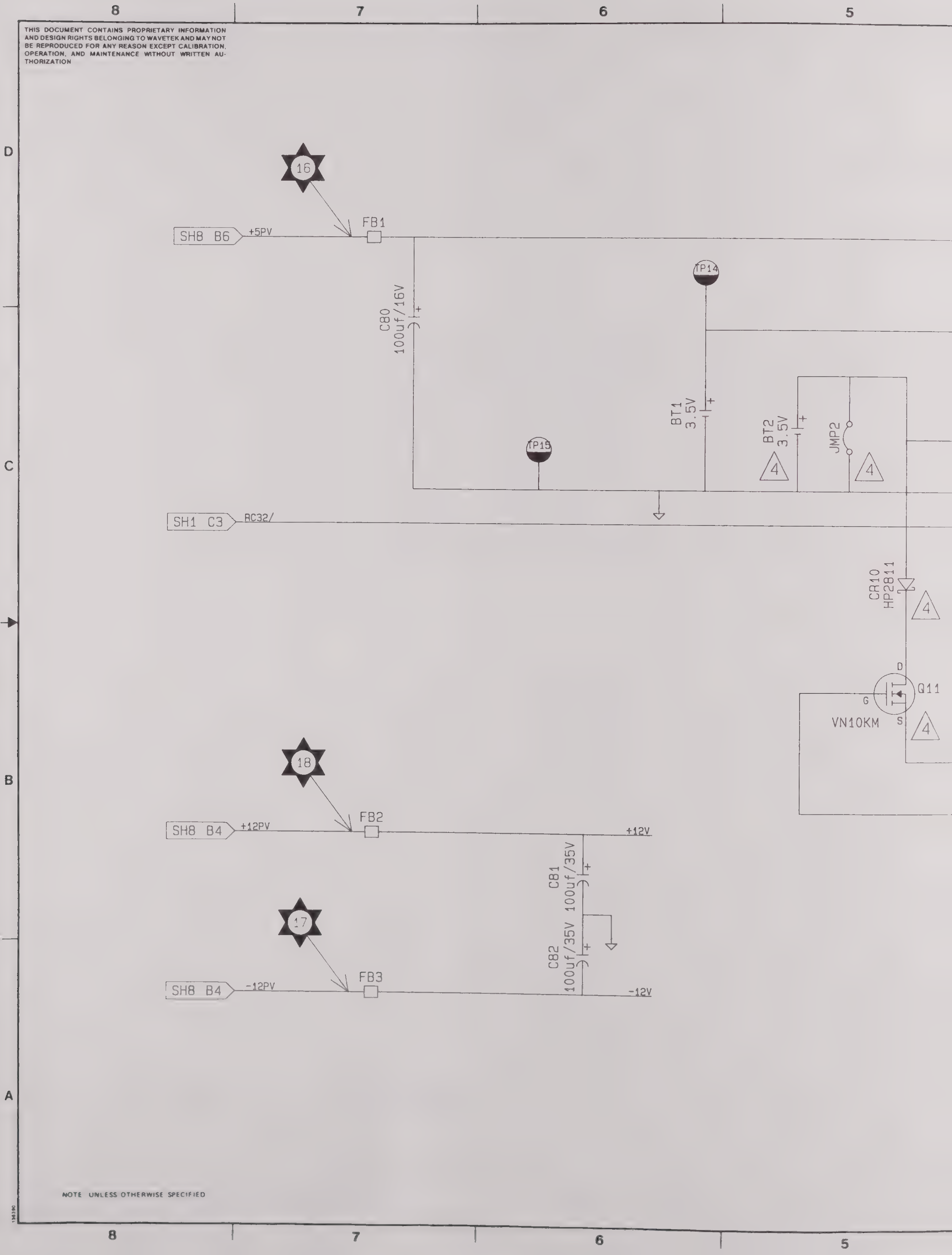
WAVETEK SAN DIEGO • CALIFORNIA

TITLE

SCHEMATIC,
ARB BOARD

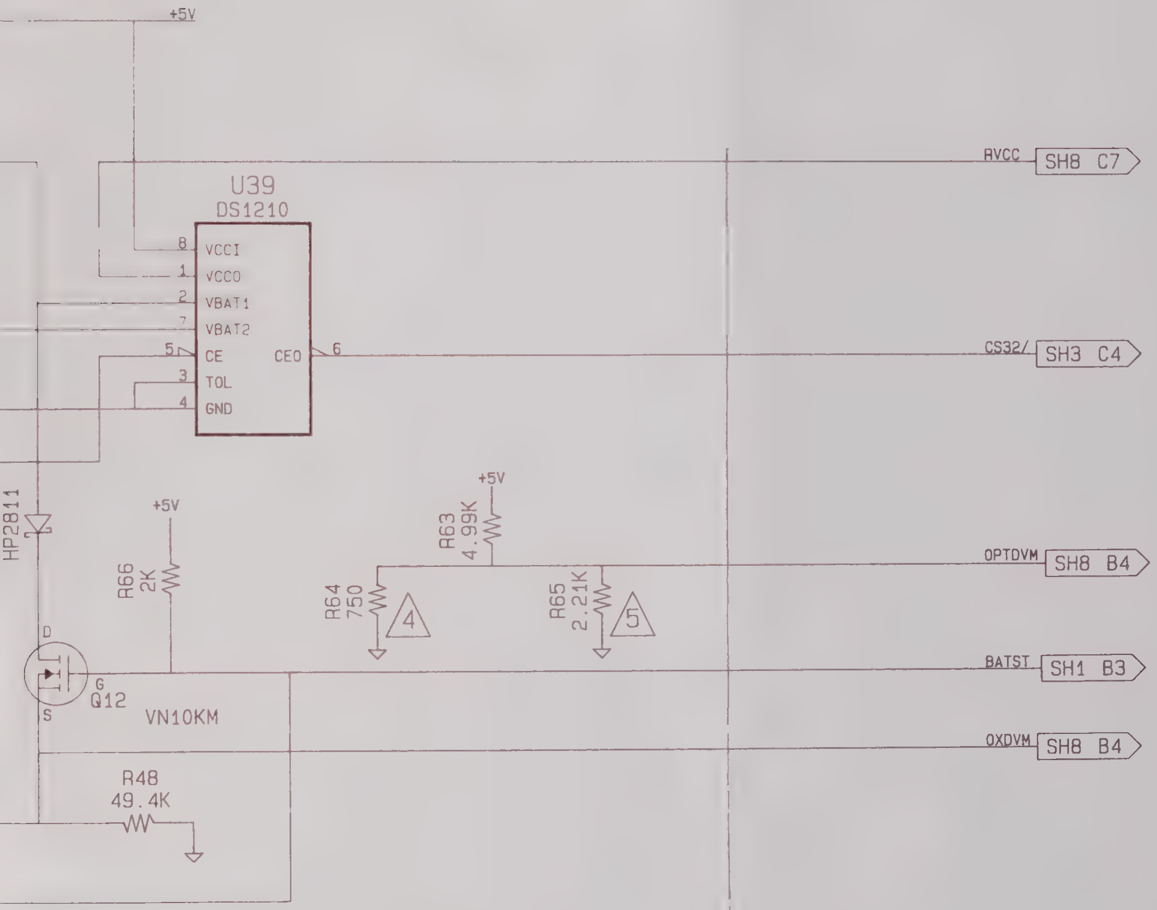
SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3327	A

SCALE MODEL 90/95 SHEET 6 OF 8


8
7
6
5
D
C
B
A
16
SH8 B6
+5PV
FB1
C80
100uf/16V
TP14
TP15
BT1
3.5V
BT2
3.5V
JMP2
4
SH1 C3
RC32/
CR10
HP2811
Q11
D
G
S
VN10KM
18
SH8 B4
+12PV
FB2
+12V
C81
100uf/35V
C82
100uf/35V
17
SH8 B4
-12PV
FB3
-12V

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP



+5V
U39
DS1210
8 VCCI
1 VCCO
2 VBAT1
7 VBAT2
5 CE
3 TOL
4 GND
CEO 6
RVCC
SH8 C7
CS32/
SH3 C4
+5V
R63
4.99K
OPTDVM
SH8 B4
HP2811
+5V
R66
2K
R64
750
4
R65
2.21K
5
D
G
Q12
S
VN10KM
BATST
SH1 B3
OXDVM
SH8 B4
R48
49.4K

CAD JOB #: B051C

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

DRAWN PO FIFER DATE 6/27/90
CHECKED
PROJ. ENGR.
RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:

FRACTIONS	DECIMALS	ANGLES
±	.XX ± .XXX ±	±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

SCHEMATIC,
ARB BOARD

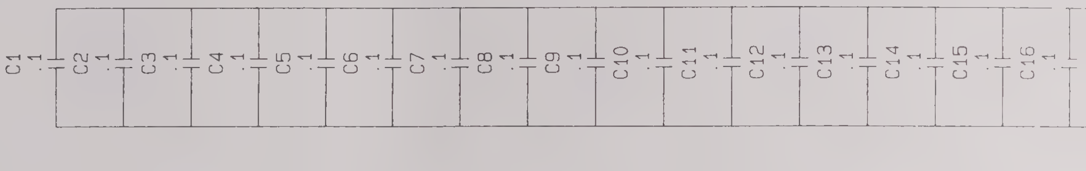
SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3327	A

SCALE

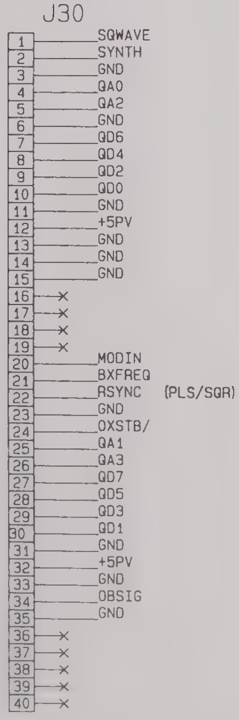
MODEL 90/95

SHEET 7 OF 8

1104-00-3327 A

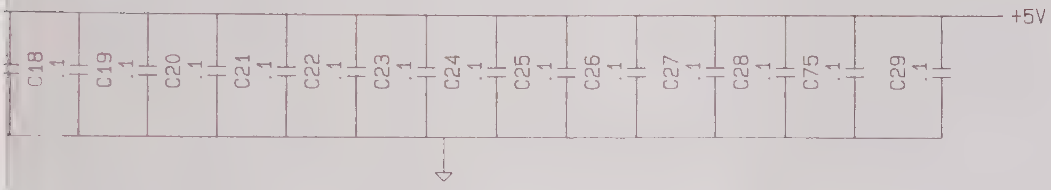

C1 .1
C2 .1
C3 .1
C4 .1
C5 .1
C6 .1
C7 .1
C8 .1
C9 .1
C10 .1
C11 .1
C12 .1
C13 .1
C14 .1
C15 .1
C16 .1

REF DES	U1.U2	U3, U4, U5, U6,	U23, U26	U27, U29	C7, C8	U
DEVICE	74ALS138	74ALS574	74ALS574	74ALS574	74ALS645	74A
RVCC						
GND	8	10	10	10	10	
+5V	16	20	20	20	20	2
-5V						
+12V						
-12V						
BYPASS CAP	C1, C2	C4, C9, C5, C10	C7, C6	C11, C12	C8, C13	C


J30
1 SQWAVE
2 SYNTH
3 GND
4 QA0
5 QA2
6 GND
7 QD6
8 QD4
9 QD2
10 QD0
11 GND
12 +5PV
13 GND
14 GND
15 GND
16 ×
17 ×
18 ×
19 ×
20 MODIN
21 BXFREQ
22 RSYNC (PLS/SQR)
23 GND
24 OXSTB/
25 QA1
26 QA3
27 QD7
28 QD5
29 QD3
30 QD1
31 GND
32 +5PV
33 GND
34 OBSIG
35 GND
36 ×
37 ×
38 ×
39 ×
40 ×

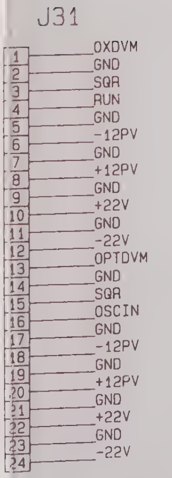
NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP


+5V
C18 .1
C19 .1
C20 .1
C21 .1
C22 .1
C23 .1
C24 .1
C25 .1
C26 .1
C27 .1
C28 .1
C75 .1
C29 .1

J13	U9	U12	U11	U14, U15	U22	U20, 21, 24, 25	U17, U19	U16, U18	U37	U39
DNC2016	GAL20V8-15	74F112	74F08	74F269	PAL16L8	74F574	MB84256A	MB81C78	74LS390	DS1210
							30, 32			
17, 14	20	8	7	7	10	10	16	14	8	4
6, 18	12	16	14	19	20	20		28	16	8
C25	C26	C27	C28	C14, C15	C16	C23, 24, 18, 17	C20, C22	C19, C21	C75	C29

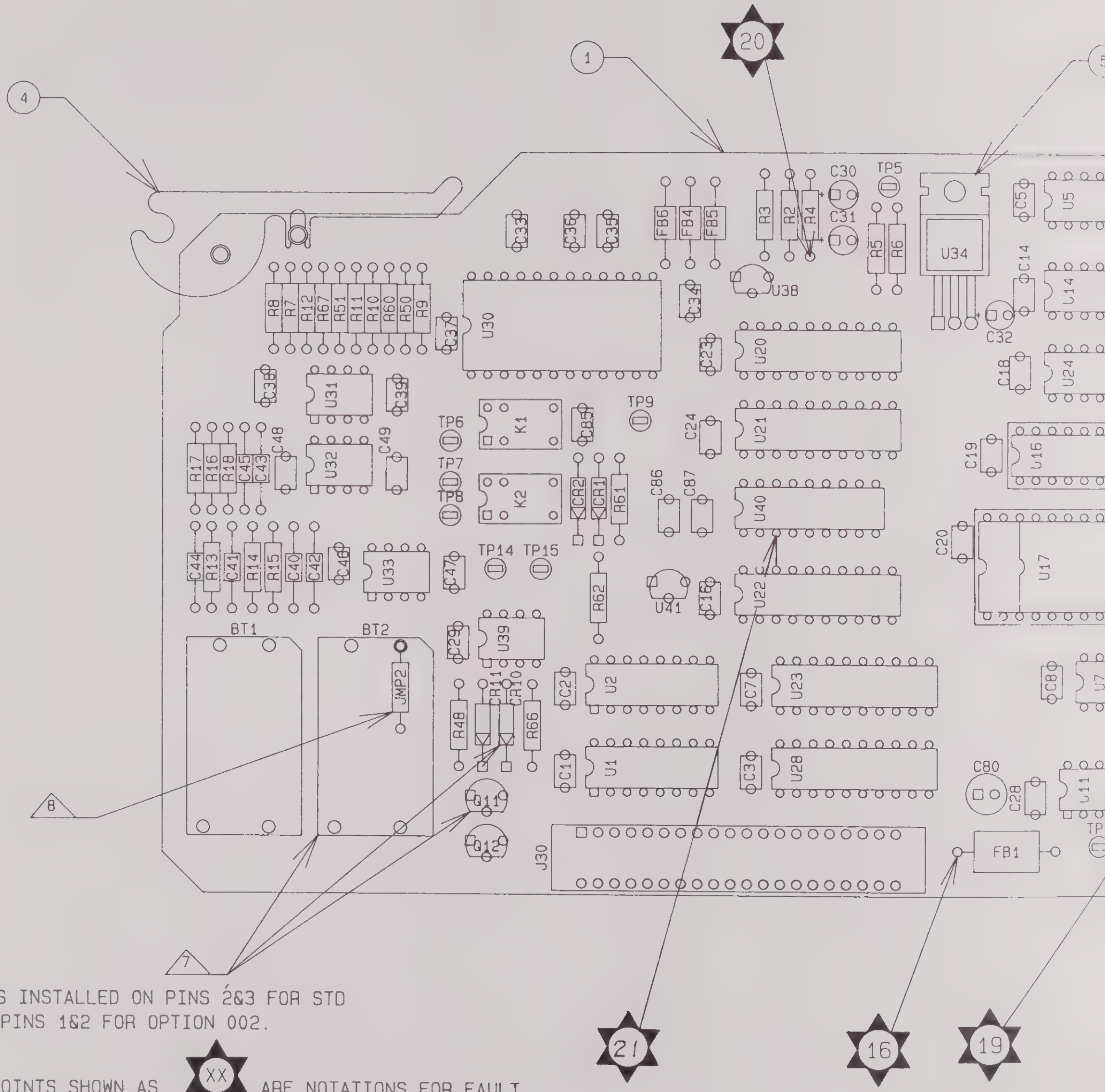
INTERCONNECT AND POWER DISTRIBUTION


J31
1 OXDVM
2 GND
3 SQR
4 RUN
5 GND
6 -12PV
7 GND
8 +12PV
9 GND
10 +22V
11 GND
12 -22V
13 OPTDVM
14 GND
15 SQR
16 OSCIN
17 GND
18 -12PV
19 GND
20 +12PV
21 GND
22 +22V
23 GND
24 -22V

1104-00-3327 A

CAD JOB #: B051C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BO EIFER	DATE 5/14/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE SCHEMATIC, ARB BOARD
	PROJ ENGR.		
	RELEASE APPROV.		
FINISH ~~WAVETEK PROCESS~~	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3327 · REV A
DO NOT SCALE DRAWING			SCALE · MODEL 90/95 · SHEET 8 OF 8



8
7
6
5
D
C
B
1
4
20
U34
U5
U14
U24
U16
U17
U7
U11
C5
C14
C32
C18
C19
C20
C8
C28
C80
FB1
TP5
C30
C31
R3
R2
R4
R5
R6
U38
FB6
FB4
FB5
C33
C36
C35
C34
R8
R7
R12
R67
R51
R11
R10
R60
R50
R9
C37
U30
C23
U20
U21
U40
U22
U41
C16
C24
C86
C87
TP9
C85
K1
K2
TP6
TP7
TP8
CR2
CR1
R61
R62
TP14
TP15
C38
U31
C39
C48
C49
U32
R17
R16
R18
C45
C43
C44
R13
C41
R14
R15
C40
C42
C46
U33
C47
BT1
BT2
JMP2
C29
U39
CR11
CR10
R48
R66
Q11
Q12
C2
U2
C7
U23
C1
U1
C3
U28
J30
TP
8
7
21
16
19

10. JMP1 IS INSTALLED ON PINS 2&3 FOR STD OR ON PINS 1&2 FOR OPTION 002.

9. TEST POINTS SHOWN AS XX ARE NOTATIONS FOR FAULT ISOLATION PROCEDURES IN THE UNIT MAINTANENCE MANUAL.

8. REMOVE JMP2 WHEN INSTALLING OPTION -002.

7. PARTS INSTALLED IN THIS AREA ARE FOR OPTION -002.

6. PARTS INSTALLED IN THIS AREA ARE FOR OPTION -001.

5. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.

4. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

3. MARK ASSEMBLY AND REVISION LETTER IN AREA SHOWN.

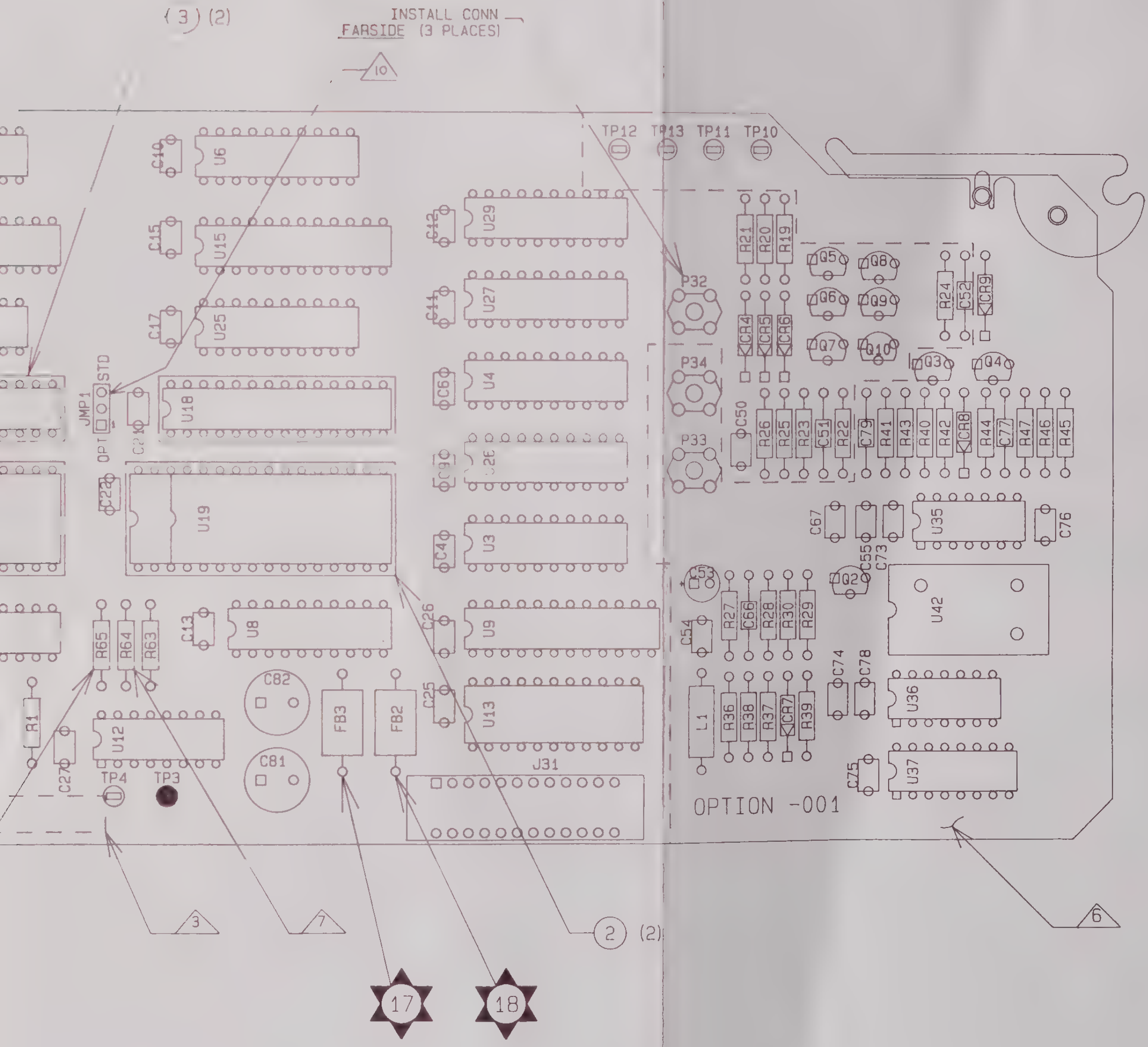
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596.

1. SEE 1104-00-3327 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

REV	ECO	BY	DATE	APP
A	ERO# 10-44		[illegible]	[illegible]
B	91-116	RO	2-1-91	


(3) (2)
INSTALL CONN FARSIDE (3 PLACES)
10
TP12 TP13 TP11 TP10
U6 U15 U25 U18 U19 U8 U12 U29 U27 U4 U26 U3 U9 U13 U35 U42 U36 U37
C10 C15 C17 C21 C22 C13 C27 C12 C11 C6 C9 C4 C26 C25 C50 C51 C79 C77 C52 C67 C55 C73 C76 C53 C54 C66 C74 C78 C75 C82 C81
JMP1 STD OPT
R21 R20 R19 R24 R26 R25 R23 R22 R41 R43 R40 R42 R44 R47 R46 R45 R27 R28 R30 R29 R36 R38 R37 R39 R65 R64 R63 R1
CR4 CR5 CR6 CR9 CR8 CR7
Q5 Q8 Q6 Q9 Q7 Q10 Q3 Q4 Q2
P32 P34 P33
L1 FB3 FB2 J31
TP4 TP3
OPTION -001
3
7
2 (2)
6
17
18

CAD JOB #: B051E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Ro Fifer	DATE 6/27/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED D. FISH	6/29/90	TITLE PCA, ARB BOARD
	PROJ. ENGR. C. Fish	6/29/90	
FINISH WAVETEK PROCESS	RELEASE APPROV. C. Fish	6/29/90	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .02 .XXX ± .010 ANGLES ±1°		SIZE D · FSCM NO. 23338 · DWG. NO. 1101-00-3327 · REV B
DO NOT SCALE DRAWING			SCALE 2:1 · MODEL 90/95 · SHEET 1 OF 1

1101-00-3327 B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D, AUX BOARD	1101-00-3327	WVTK	1101-00-3327	1
NONE	SCHEMATIC, ARB BD	1104-00-3327	WVTK	1104-00-3327	1
C52	CAP, CER, 10PF, 100V, AXIAL	CAC02CG0100J100A	CORNG	1500-01-0006	1
C1 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C2 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C3 C33 C34 C35 C36 C37 C38 C39 C4 C46 C47 C48 C49 C5 C50 C54 C55 C6 C67 C7 C73 C74 C75 C76 C78 C8 C85 C86 C87 C9	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2 SP .2	SR215E104ZAA	AVX	1500-01-0420	52
C45	CAP, CER, 12PF, 100V, 5%, AXIAL	CAC02CG0120J100A	CORNG	1500-01-2000	1
C42	CAP, CER, 150PF, 100V, 5%, AXIAL	CAC02CG0151J100A	CORNG	1500-01-5100	1
C51	CAP, CER, 330PF, 100V, AXIAL	CAC02CG0331J100A	CORNG	1500-03-3106	1
C77 C79	CAP, CER, 47PF, 100V, AXIAL	CAC02CG0470J100A	CORNG	1500-04-7006	2
C66	CAP, CER, 470PF, 100V, 5%, AXIAL	CAC03CG0471J100A	CORNG	1500-04-7100	1
C44	CAP, CER, 56PF, 100V, 5%, AXIAL	CAC02CG0560J100A	CORNG	1500-05-6000	1

WAVETEK
PARTS LIST

TITLE
PCA, ARB BOARD OPT 1 AND 2, MODEL 95

ASSEMBLY NO. 1100-00-3401

REV C

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION
J30	CONN, HEADER, 40 PIN, RECPT, 2X20, .1 C PCMT
2 NONE	SOCKET, DUAL WIPE, 3 PIN
3 NONE	SOCKET, IC, 28 PIN, 30 MIL, DIP
TP13 TP15 TP4 TP9	TEST POINT, BLK, PC
TP1 TP10 TP11 TP12 TP14 TP2 TP3 TP5 TP6 TP7 TP8	TEST POINT, RED, PC
P32 P33 P34	CONN, SUB MIN
U42	OSCILLATOR, TEMP COMPENSATED 10MHZ XTAL, 14 PIN DIP, 0.030 LEADS
4	PC BD EJECTOR
5	RIVET PLASTIC
FB1 FB2 FB3	BALUN CORE, FERRITE, 680 OH
FB4 FB5 FB6	BALUN CORE, FERRITE, OHMS
BT1 BT2	BATTERY, LITHIUM 3.5

WAVETEK
PARTS LIST

TITLE
PCA, ARB BOARD OPT 1 AND 2, MODEL 95

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C41	CAP, CER, 560PF, 100V, 5%, AXIAL	CAC03CG0561J100A	CORNG	1500-05-6100	1
C43	CAP, CER, 82PF, 100V, 5%, COG, AXIAL	SA102A820JAA	AVX	1500-08-2006	1
C40	CAP, CER, 820PF, 100V, 5%, AXIAL	CAC03CG0821J100A	CORNG	1500-08-2100	1
C81 C82	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	2
C80	CAP, ELECT, 100MF/16V RADIAL LEAD, SP .20	NRE101M16V6.3X11	NIC	1500-31-0111	1
C30 C31 C32	CAP, TANT, 1MF, 35V	196D105X0035HA1(OBS)	SPRAG	1500-71-0512	3
C53	CAP, TANT, 22MF, 15V	196D226X9015KA1(OBS)	SPRAG	1500-72-2601	1
1	PCB, ARB BD	1700-00-3327	WVTK	1700-00-3327	1
L1	INDUCTOR, 390MH	2500-08	DELVN	1800-00-0023	1
XJMP1	CONN, HEADER, 3 PIN	929834-01-03	APTRN	2100-02-0196	1
JMP1	JUMPER, FEMALE, 2 POSITION, 0.1 SPACE	929950-00	APTRN	2100-02-0213	1
J31	CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT	102565-7	AMP	2100-02-0255	1

WAVETEK
PARTS LIST

TITLE
PCA, ARB BOARD OPT 1 AND 2, MODEL 95

ASSEMBLY NO. 1100-00-3401

REV C

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION
	750MAH
K1 K2	RELAY, 1 FORMC, 5V, .312H, 296
R27 R30	RES, MF, 1/8W, 1%, 100
R2 R29 R36 R37 R38 R50 R51	RES, MF, 1/8W, 1%, 1K
R62	RES, MF, 1/8W, 1%, 10K
R21 R43	RES, MF, 1/8W, 1%, 1.21
R5	RES, MF, 1/8W, 1%, 124
R7 R8	RES, MF, 1/8W, 1%, 1.62
R23 R4 R66	RES, MF, 1/8W, 1%, 2K
R22 R26 R65	RES, MF, 1/8W, 1%, 2.21
R3 R46 R67	RES, MF, 1/8W, 1%, 249
R20	RES, MF, 1/8W, 1%, 2.49
R11 R12	RES, MF, 1/8W, 1%, 27.4
R61	RES, MF, 1/8W, 1%, 3.01
R16 R17 R18 R6	RES, MF, 1/8W, 1%, 392
R60	RES, MF, 1/8W, 1%, 3.92

WAVETEK
PARTS LIST

TITLE
PCA, ARB BOARD OPT 1 AND 2, MODEL 95

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

…-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
02585-2	AMP	2100-02-0256	1
-3268-84-T	ROBNU	2100-03-0086	2
02103-1	AMP	2100-03-0102	2
104-01-00	COMPO	2100-04-0054	4
104-01-02	COMPO	2100-04-0055	11
48	AMPH	2100-07-0011	3
0B2A1	MONIT	2300-99-0026	1
2-C	BRIT	2800-07-0032	2
-080551-05-0101	FASTX	2800-60-0008	1
3666671	FARIT	3100-00-0017	3
3015111	FARIT	3100-00-0018	3
7P	EAGLE	4000-02-0009	2

ASSEMBLY NO. 1100-00-3401
PAGE 3
REV C

…-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
-M-DC5V	AROMT	4500-00-0034	2
D-1000F	TRW	4701-03-1000	2
D-1001F	TRW	4701-03-1001	7
D-1002F	TRW	4701-03-1002	1
D-1211F	TRW	4701-03-1211	2
D-1240F	TRW	4701-03-1240	1
D-1621F	TRW	4701-03-1621	2
5D-2001F	TRW	4701-03-2001	3
D-2211F	TRW	4701-03-2211	3
5D-2490F	TRW	4701-03-2490	3
D-2491F	TRW	4701-03-2491	1
D-27R4F	TRW	4701-03-2749	2
5D-3011F	TRW	4701-03-3011	1
D-3920F	TRW	4701-03-3920	4
5D-3921F	TRW	4701-03-3921	1

ASSEMBLY NO. 1100-00-3401
PAGE 4
REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R42 R45	RES, MF, 1. 8W, 1%, 46. 4	RN55D-46R4F	TRW	4701-03-4649	2
R40 R47	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	2
R19 R28 R63	RES, MF, 1/8W, 1%, 4. 99K	RN55D-4991F	TRW	4701-03-4991	3
R24 R48	RES, MF, 1/8W, 1%, 49. 9K	RN55D-4992F	TRW	4701-03-4992	2
R25	RES, MF, 1/8W, 1%, 49. 9	RN55D-49R9F	CORNG	4701-03-4999	1
R13 R14 R15	RES, MF, 1/8W, 1%, 5. 49K	RN55D-5491F	MEPCO	4701-03-5491	3
R10 R39 R64 R9	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	4
R41 R44	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	2
R1	RES, MF, 1/8W, 1%, 90. 9	RN55D-90R9F	TRW	4701-03-9099	1
CR1 CR2 CR4 CR5 CR6 CR7	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	6
CR10 CR11 CR8 CR9	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	4
Q10 Q2 Q4 Q5 Q6 Q7 Q8 Q9	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	8
Q3	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906	FAIR	4901-03-9060	1
Q11 Q12	TRANS	VN10KM	INTSL	4902-00-0100	2

WAVETEK PARTS LIST
TITLE
PCA, ARB BOARD OPT 1 AND
2, MODEL 95
ASSEMBLY NO. 1100-00-3401
PAGE 5
REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U34	VOLT REGULATOR	LM337T	NSC	7000-03-3700	1
U38 U41	VOLTAGE REFERENCE DIODE	LM385Z-1. 2	NSC	7000-03-8501	2
U35	COMPARATOR, DUAL DIFFERENTIAL, SENSE AMP	NE521N	SIG	7000-05-2100	1
U31	OP, AMP CURRENT FEEDBACK, 50mhz	EL2020CN	ELAN	7000-20-2000	1
U32	VIDEO BUFFER	HA3-5033-5	HARIS	7000-50-3300	1
U33	OP AMP, HI SLEW RTE, WIDEBND, JFET, STD	MC34081P	MOT	7003-40-8100	1
U30	DAC, 12 BIT, 20MHZ	TDC1012N7-C2	TRW	8000-10-1200	1
U40	DAC, 8, BIT, VOLT, OUTPUT , BUSS COMP, CMOS	PM7224HP	PMI	8000-72-0024	1
U11	GATE, QUAD 2-INPUT AND	MC74F08N	MOT	8000-74-0008	1
U36	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	1
U12	FLIP FLOP, DUAL J-K, NEG EDGE TRIG	74F112PC	NSC	8000-74-0112	1
U14 U15	COUNTER, 8, BIT BINARY, UP/DOWN, 100MHZ	74F269PC	NSC	8000-74-0269	2

WAVETEK PARTS LIST
TITLE
PCA, ARB BOARD OPT 1 AND
2, MODEL 95
ASSEMBLY NO. 1100-00-3401
PAGE 6
REV C

REMOVE ALL BURRS
AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ ENGR.
RELEASE APPROV
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE.
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
ARB BOARD
SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-3401
REV C
SCALE
MODEL 95
SHEET 1 OF 2

115685

D

C

B

A

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U16 U18	SRAM, 128K*8, 120NS, LOW PWR, 600 MIL	HM628128LP-12	HTACH	8006-28-1281	2
U17 U19	SRAM, 32K*8, 35NS, 300 MIL	HM62832P-35	HTACH	8006-28-3235	2
U1 U2	DECODER/DEMUX, 3 TO 8 LINE	SN74ALS138N	TI	8007-41-3800	2
U28	BUF, OCT 3ST OUT, TTL	SN74LS244N	TI	8007-42-4410	1
U37	COUNTER, DUAL 4B BCD, TTL	74LS390PC	FAIR	8007-43-9010	1
U20 U21 U24 U25	FLIP-FLOP, D-TYPE, OCT, W/TRI STATE OUT	74F574PC	NSC	8007-45-7400	4
U23 U26 U27 U29 U3 U4 U5 U6	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	8
U7 U8	TRANSCEIVER, OCTAL BUS W/3 STATE	SN74ALS645A-1N	TI	8007-46-4500	2
U39	BAT, CONTROLLER, 8, PIN, CHIP, ENABLE, I/O	DS1210	DALAS	8100-12-1000	1
U22	PAL, PROG, USES LEA, 8000-16-8000 FOR MOD 90, V1. 5. 0, REF U22	8600-00-0584	WWVTK	8600-00-0584	1
U9	PROG, GAL, USES 1 EA 8000-20-8015FOR MOD90/95 V1. 1, REF U9	8600-00-0636	WVTK	8600-00-0636	1

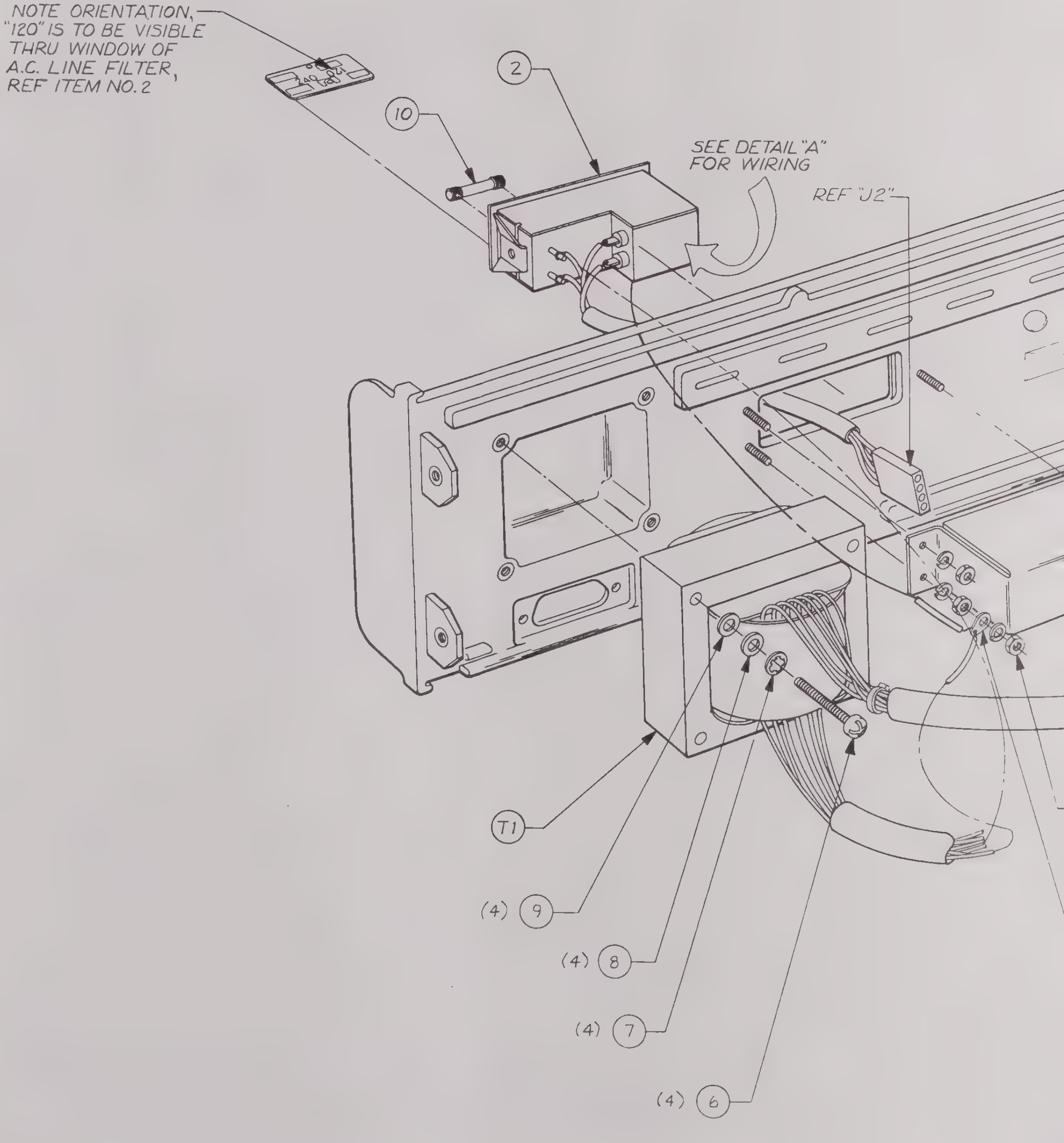
WAVETEK PARTS LIST
TITLE PCA, ARB BOARD OPT 1 AND 2, MODEL 95
ASSEMBLY NO. 1100-00-3401
REV C
PAGE 7

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U13		CLA53047BA	PLESS	8700-00-0005	1

WAVETEK PARTS LIST
TITLE PCA, ARB BOARD OPT 1 AND 2, MODEL 95
ASSEMBLY NO. 1100-00-3401
REV C
PAGE 8

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
DATE
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE.
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE PARTS LIST ARB BOARD
SIZE D
FSCM NO. 23338
DWG. NO. 1100-00-3401
REV C
SCALE
MODEL 95
SHEET 2 OF 2

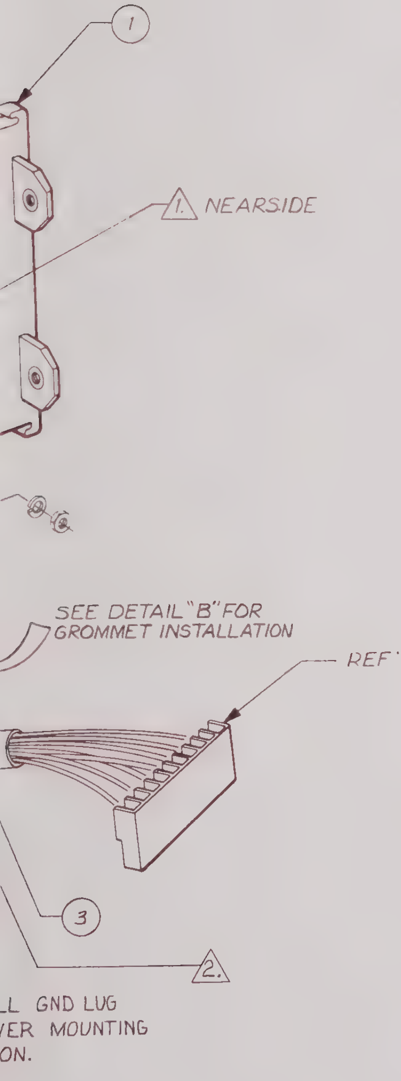

NOTE ORIENTATION, "120" IS TO BE VISIBLE THRU WINDOW OF A.C. LINE FILTER, REF ITEM NO. 2
2
10
SEE DETAIL "A" FOR WIRING
REF "U2"
T1
(4) 9
(4) 8
(4) 7
(4) 6
8
7
6
5
D
C
B
A

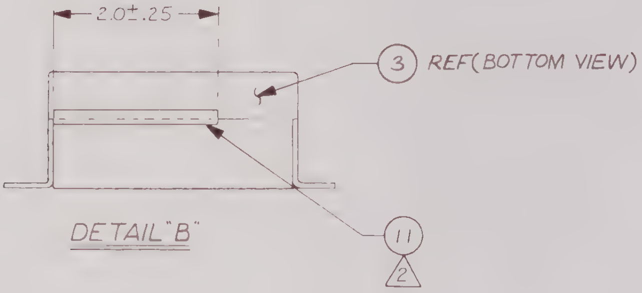
2. INSTALL GROMMET 3200-06-0079 (LESIG PART 924) OR 3200-06-0053 (MINOR RUBBER PART NO. ZX-4064) OR EQUIV. TO SHIELD (ITEM 3) WITH ADHESIVE 1600-03-0013 (LOC TITE PART NO. 414) OR EQUIV.

1. MARK ASSEMBLY NO. "1101-00-3325", LATEST REV, FSCM 23338, PER MIL-STD-130, APPROX WHERE SHOWN.

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ERO NO. 90-381	AD	[illegible]	[illegible]
B	ECO # 90-513	MS	1-12-10	[illegible]

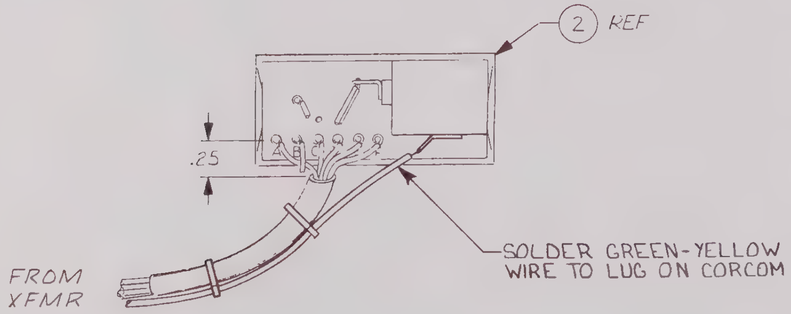

1
1 NEARSIDE
SEE DETAIL "B" FOR GROMMET INSTALLATION
REF "J4"
3
2
LL GND LUG
VER MOUNTING
ON.


2.0±.25
3 REF(BOTTOM VIEW)
11
2

DETAIL "B"

WIRE LIST

XFMR WIRE COLOR	LINE FILTER TERM. MARKING
VIOLET	A
BLACK	C
GRAY	D
WHT/BLK	E
WHT/GRAY	F


2 REF
.25
A B C D E F
FROM XFMR
SOLDER GREEN-YELLOW WIRE TO LUG ON CORCOM

DETAIL A

XFMR WIRE HOOKUP

SEE SEPARATE PARTS LIST

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN SCIAP	DATE 3/7/90	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL — // —	CHECKED D. Buzzell	6/5/90	TITLE ASSEMBLY, REAR PANEL	
	PROJ. ENGR	6/5/90		
FINISH WAVETEK PROCESS — // —	RELEASE APPROV	[illegible]		
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG NO 1101-00-3325	REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90/95 · SHEET 1 OF	

115685

8 7 6 5

D

C

B

A

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D, REAR PANEL ASSY, MODEL 90	1101-00-3325	WVTK	1101-00-3325	1
2	CABLE ASSY, LINE FILTER	1207-00-3011	WVTK	1207-00-3011	1
3	SHIELD, AC CONN	1400-02-3463	WVTK	1400-02-3463	1
NONE	REAR PANEL, MODEL 90	1400-02-5035	WVTK	1400-02-5035	1
NONE	FUSE, 1A, 250V, S-B	MDL 1	BUSS	2400-05-0029	1
4	NUT, HEX, 4-40	MS35649-244	COML	2800-14-4100	4
9	WASHER, #8 FIBER BIN 470	#8 FIBER WASHER	CMRCL	2800-28-8000	4
	SCREW, PAN, CAD I, CROSS RECESS, 8-32 X 2 1/4	8-32 X 2 1/4 PAN	CMRCL	2800-38-8136	4
5	WASHER, LOCK REG, S/S #4	MS 35338-135	CMRCL	2800-45-4000	4
8	WASHER, #8, FLT, SS, THK .050, ID .174, OD .375	2800-46-8000	CMRCL	2800-46-8000	4
7	WASHER, #8, INT TOOTH, LOCK, SS	2800-56-0002	CMRCL	2800-56-0002	4
11	EXTRU, RUBBER, U CHNL, 1/16 INSIDE, 1/8 OUTSIDE	924	LESIG	3200-06-0079	2

WAVETEK
PARTS LIST
TITLE REAR PANEL ASSY
ASSEMBLY NO. 1100-00-3325
REV C
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
T1	TRANSFORMER, POWER, 90/95	5600-00-0050	ENSIG	5600-00-0050	1

WAVETEK
PARTS LIST
TITLE REAR PANEL ASSY
ASSEMBLY NO. 1100-00-3325
REV C
PAGE 2

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING

	DATE
DRAWN	
CHECKED	
PROJ. ENGR	
RELEASE APPROV	

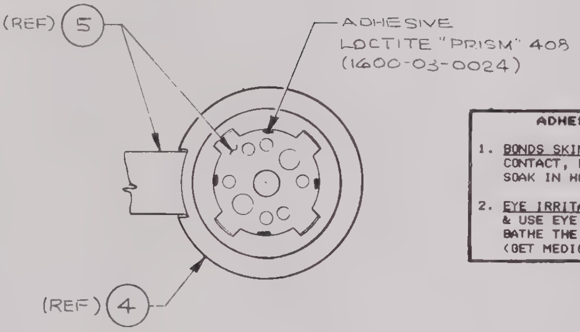
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO • CALIFORNIA
TITLE
PARTS LIST
REAR PANEL

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-3325	C

SCALE
MODEL 95
SHEET 1 OF 1

SIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT
PRODUCED FOR ANY REASON EXCEPT CALIBRATION,
RATION, AND MAINTENANCE WITHOUT WRITTEN AU-
ORIZATION

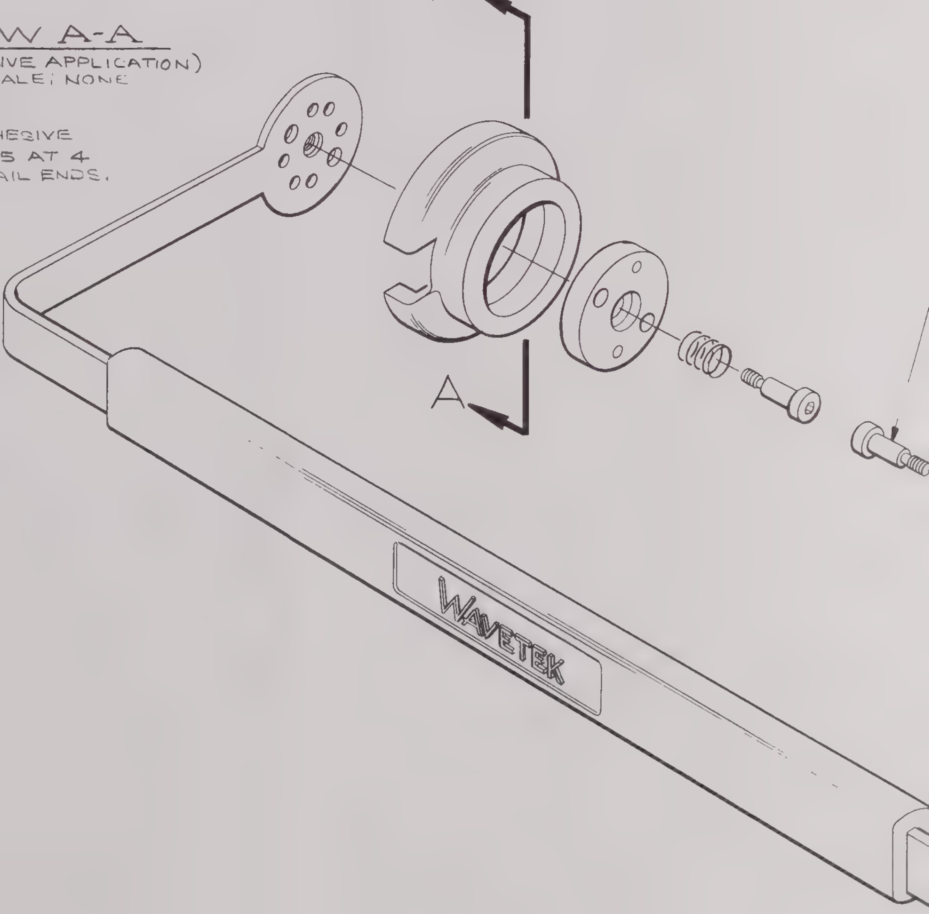


VIEW A-A
(ADHESIVE APPLICATION)
SCALE: NONE

ADHESIVE HANDLING PRECAUTIONS

1. BONDS SKIN IN SECONDS. IN CASE OF BODY CONTACT, FLUSH WITH WATER. TO SEPARATE SKIN, SOAK IN HOT SOAPY WATER.
2. EYE IRRITANT. USE WITH ADEQUATE VENTILATION & USE EYE PROTECTION. IN CASE OF EYE CONTACT, BATHE THE EYE WITH LARGE QUANTITIES OF WATER (GET MEDICAL ATTENTION).

ADHESIVE APPLICATION:
USE MINIMUM AMOUNT OF ADHESIVE (1 DROP) BETWEEN ITEMS 4 & 5 AT 4 LOCATIONS SHOWN ON BOTH BAIL ENDS.



1 MOUNTING SCREWS AND END CAPS ARE INSTALLED AT CHASSIS ASSEMBLY LEVEL. (EACH END)

NOTE UNLESS OTHERWISE SPECIFIED

D
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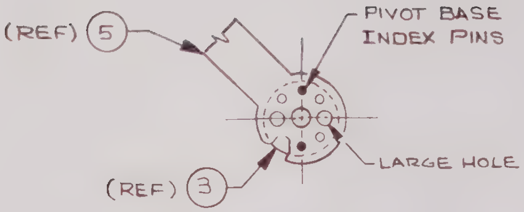
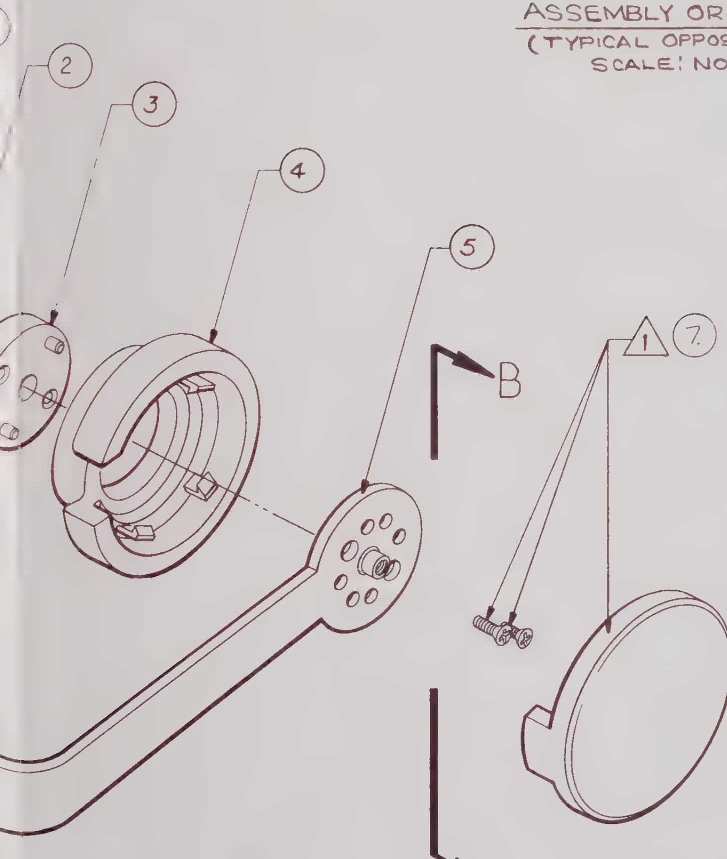
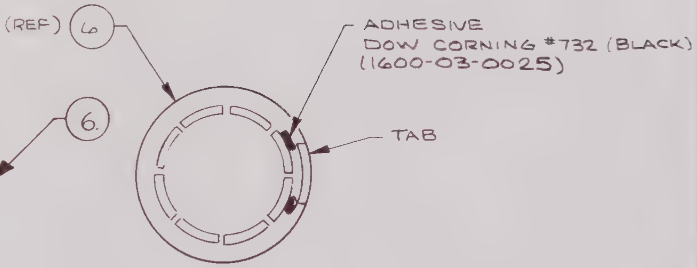
8 7 6 5

REV	ECO	BY	DATE	APP
A	ERO NO. 90-441	AD	4/23/90	
B	ECO # 90-536	MS	9-13-90	


(REF) 5
PIVOT BASE INDEX PINS
LARGE HOLE
(REF) 3

ASSEMBLY ORIENTATION
(TYPICAL OPPOSITE SIDE)
SCALE: NONE




(REF) 6
ADHESIVE
DOW CORNING #732 (BLACK)
(1600-03-0025)
TAB

VIEW B-B
(ADHESIVE APPLICATION)
SCALE: NONE

ADHESIVE APPLICATION: (2 PLACES)
USE MINIMUM AMOUNT OF ADHESIVE APPROX 1/16 INCH DIA x 3/16 INCH LONG 2 PLACES AS SHOWN. ASSEMBLE PARTS WITHIN 5 MINUTES AFTER ADHESIVE APPLICATION.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D.COOPER	DATE 511-90	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	CHECKED	6/25/90	TITLE ASSEMBLY TILT BAIL	
	PROJ. ENGR.	6/25/90		
FINISH WAVETEK PROCESS	RELEASE APPROV.	6/29/90		
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS ±/ DECIMALS .XX ± / .XXX ± / ANGLES ± /		SIZE D · FSCM NO. 23338 · DWG. NO. 1201-00-3392	REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90/95 · SHEET 1 OF 1	

115685

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NOTE UNLESS OTHERWISE SPECIFIED

APPENDIX A
PRODUCT SPECIFICATIONS

A.1 MODEL 95

The Model 95 is a rugged 1mHz to 20 MHz programmable, synthesized Arbitrary/Function Generator. The function generator produces predefined sine, triangle, and square waveforms. While the arbitrary waveform generator (Arb) supplies user-defined waveforms. Function generator and Arb waveforms can be continuous, triggered, gated, burst, AM (amplitude modulation), SCM (suppressed carrier modulation), FM (frequency modulation), or sweep. The two main outputs (balanced and unbalanced) supply the selected waveform at levels from 1mVpp to 30 Vpp.

The Arb generator lets the user to define up to four functions (waveforms). The unit stores these waveforms in its battery-backed memory (RAM). Each of the four Arb waveforms may be 2 words to 8K words horizontal by 12 bits (4096 points) vertical; also see Option 002. Edit the Arb waveforms using point, line, or three point edit methods. Plus, the Model 95 can insert dc, triangle, square, ramp up, ramp down, sine, cosine, inverse sine, or inverse cosine within a waveform.

At frequencies above 20Hz (all functions in continuous, AM, and SCM modes) the Model 95 phase locks its function generator to its own internal frequency synthesizer (internal phase lock). The internal synthesizer improves the frequency accuracy to ±(10ppm + 1.5 ppm/°C); also see Option 001. This internal frequency synthesizer also acts as an internal trigger source for the trigger, gate, or bust modes. Also the Model 95 can phase lock to an external source (same conditions as internal phase lock). When external phase locked, the Model 95 allows the phase of the output to be shifted ±180°.

A.2 SPECIFICATIONS

A.2.1 Waveforms (Functions)

Programmable sine, triangle, and square; variable symmetry for pulse and ramp waveforms; arbitrary waveforms; and dc.

Sine Distortion

Sine function at all outputs :

<1% (-40dB) THD 1 mHz to 20 Hz;
<0.5% (-46dB) THD 20 Hz to 100 kHz.

Arb Sine Waveform, Max. sample frequency and data points for sine wave, 50 kHz filter:

<0.18% (-55dB) THD to 100 kHz.

Unbalanced Output, 50Ω and 75Ω, no harmonics above:

-40 dBc, 100 kHz to 2 MHz,
-30 dBc, 2 MHz to 6 MHz,
-25 dBc, 6 MHz to 20 MHz.

Time Symmetry

With fixed 50% time symmetry the accuracy is <±(0.2% + 5 ns). Time symmetry is variable from 5% to 95% in 1% steps to 2 MHz. Between 2 MHz and 20 MHz the time symmetry limits linearly decrease to a fixed 50% at 20 MHz. Accuracy is <±(1% + 5 ns).

Square Transition Time

The transition time (rise/fall) is <9 ns, 10% to 90%, unbalanced output into 50 Ω impedance.

Aberrations

Overshoot and ringing is <(5% + 20 mV) of the peak to peak amplitude.

Triangle Linearity

10% to 90% nonlinearity:

±1%, 2 mHz to 100 kHz;
±2%, 100 kHz to 2 MHz;
±10%, 2 MHz to 5 MHz.

A.2.2 Operational Modes

Continuous

In this mode, the Model 95 supplies a continuous waveform at the selected frequency. The unit automatically selects its internal synthesizer at frequencies above 20 Hz.

Triggered

In this mode, the Model 95 remains quiescent at trigger baseline of selected function until a trigger event occurs. The Trig/Freq In signal, Manual Trigger, GPIB trigger command, or internal trigger starts the trigger event. This event initiates a single waveform at the programmed frequency and, after completing the waveform, returns the generator to the quiescent baseline. Accuracy of triggered waveform period is <±3%.

Gated

In this mode the Model 95 functions the same as the Triggered mode, except the generator runs continuously while the trigger event is true. The generator starts and stops in the quiescent state, and the Model 95 always completes its last cycle. Gate outputs initiated by the internal synthesizer have an approximate 1:1 on/off cycle.

Burst

In this mode, the Model 95 functions like the Triggered mode, except that the number of cycles generated, when triggered, is programmable from 1 to 1,000,000. The generator starts and stops in its quiescent state.

Amplitude Modulation (AM)

In this mode the Model 95 functions like the continuous mode except an external signal modulates the amplitude of the Model 95's output (carrier). The external signal can modulate the Model 95 from 0 to 100%. In this mode, the Model 95 displays the average amplitude; the Continuous amplitude must be <7.5 Vpp in order to select the AM mode.

Suppressed Carrier Modulation (SCM)

In this mode, the Model 95 functions like the AM mode, except the Model 95 suppresses the output level to 0V with no external signal supplied. Three scale factors (Vout/Vin) aid in determining the input to output signal level. SCM can only be selected when the Continuous signal level is <7.5 Vpp.

Frequency Modulation (FM and VCG)

In the FM mode, an external signal controls the frequency of the generator. Connecting a dc level to the Trig/Freq In connector shifts the generator to a frequency based on the magnitude of the level. Connecting an ac signal to the Mod In deviates the frequency of the generator about its programmed frequency. The Model 95 only can be frequency modulated a maximum of three decades on a fixed range. Internal or external phase lock is not selectable in this mode.

Sweep

In this mode, the Model 95's frequency varies between start and stop frequencies. The unit linearly or logarithmically sweeps the frequency up to three decades on a selected range. The Model 95 provides five sweep modes: sweep start, sweep stop, continuous sweep, triggered sweep, or manually sweep. Sweep time is programmed from 100 ms to 3600s. Start/Stop frequency accuracies are <±3% on the top decade of the sweep and ±5% on the lower two decades of the sweep. All 50% symmetrical waveforms can be swept.

A.2.3 Frequency

Range

1 mHz to 20 MHz,
20 Hz to 20 MHz, synthesized,
1 mHz to 1 MHz, 600Ω or balanced output.

Resolution

4 digits

Accuracy

±10 ppm (20 ±5°C) synthesized:
    20 Hz to 20 MHz Continuous, AM, or SCM modes.
±3% of setting non-synthesized:
    1 mHz to 20 Hz in Continuous, AM, or SCM mode;
    1 mHz to 20 MHz, in Triggered, Gated, or Burst mode.
±3% of setting at 100:1 of range , linearly increasing to ±13% at 1000:1 of range in FM or Sweep mode.

Stability

VS temperature:
    ±2 ppm/°C for synthesized (0°C to 50°C);
    <100 ppm/°C for non-synthesized.
VS time:
    ±20 ppm/year for synthesized,
    ±0.5% for non-synthesized within 24 hours;
    ±0.1% for non-synthesized within 10 minutes.

Internal Phase Lock

The Model 95 can be phase locked at frequencies >20 Hz (Continuous, AM or SCM mode) to an internal crystal referenced frequency synthesizer which improves the generator's frequency accuracy and stability.

External Phase Lock

The Model 95 phase locks (frequencies above 20 Hz: Continuous, AM, or SCM mode) to an external source. Model 95 measures the external signal, sets the generator's frequency, and locks the generator to the source. The external source controls the generator's frequency, stability, and purity.

Also, external phase lock permits programmable phase shift (±180° or ± π radians) with 1° resolution. Phase lock accuracy (50 Hz to 10 MHz) is ±(4° + 20 ns) accuracy. If the external source has dc offset, the Model 95 ignores the offset.

A.2.4 Amplitude

Range

1 mVpp to 15 Vpp terminated into selected output impedance;
2 mVpp to 30 Vpp into an open circuit.

Resolution

4 Digits: 2 mVpp to 20 Vpp Open Circuit (minimum 1 mV),
1 mVpp to 10Vpp Terminated ;
4 1/2: 20 Vpp to 30 Vpp Open Circuit,
10 Vpp to 15 Vpp Terminated.
Offset waveforms may reduce amplitude resolution.

Accuracy

Percent of settings for all functions at 1 kHz:
±(2% + 1 mV), to 100 mVpp terminated;
±(2% + 2 mV), to 1 Vpp terminated;
±(2% + 10 mV), to 15 Vpp terminated.

Flatness (50Ω or 75Ω)

Relative to 1 kHz:
- Unbalanced 50Ω
  - <2 MHz
    - ±0.3 dB, sine and square;
    - ±0.5 dB, triangle.
  - 2 MHz to 20 MHz
    - ±0.75 dB, sine and square;
    - ±1.5 dB, triangle.
- Balanced 135Ω
  - <100 kHz
    - ±0.3 dB, sine.
  - 100 kHz to 1 MHz
    - ±0.75 dB, sine.

A.2.5 Offset

Range

±7.5 V terminated;
±15 V open circuit.

Resolution

4 digits; programming both offset and amplitude may reduce resolution.

Accuracy

±(2%of reading + 1 mV), to 9.99 mV terminated;
±(2% + 2 mV), to 999 mV terminated;
±(2% + 10 mV), to 7.5V terminated.

A.2.6 Outputs

Sync Output

Sync Out is a female BNC connector which supplies a TTL compatible synchronizing pulse output. The sync signal is at programmed frequency and symmetry and in phase with the square function. Output level is >2 Vpp to <0.4 Vpp into 50Ω termination. The 10% to 90% transition times are less than 13ns. When using Arb functions, the Sync Address key sets an Arb Address.

Sweep Output

Sweep Out is a female BNC connector,which supplies a 0 to +5V ramp to indicate sweep position. Source impedance is 600Ω. Sweep Output is active only with the sweep modes.

Unbalanced Output

Unbalanced output is a female BNC connector which is the source of programmed waveform at selected frequency, amplitude, symmetry, and offset. Source impedance is 600Ω ± 1% to 1 MHz, 50Ω ± 1%, or 75Ω ± 1% to 20 MHz. The unbalanced output can not be used with the balanced output.

Balanced Output

Balanced outputs are dual "banana jack" connectors which provide differential outputs. A universal binding post provides a signal common "center tap" connection. Source impedance is programmable as 135Ω ± 1% or 600Ω ± 1% to 1 MHz. The balanced output can not be used with the unbalanced output.

Z-Axis Output

Z-Axis Out is a rear panel BNC connector for scope Z-Axis (intensity) modulation during Arb editing. Select the Z-Axis characteristics to match the scope's Z-Axis input. The Model 95 produces an output of 150 mVp to 4 Vp (50Ω termination) with positive pulse and selectable polarity (logic sense not amplitude).

A.2.7 Inputs

Trigger/Frequency Input

Trig/Freq In serves two functions. In trigger modes, it accepts trigger source. The source can be TTL (dc to 20 MHz) or bipolar (0.6 Vpp to 30 Vpp, 20 Hz to 20 MHz (default)). Minimum pulse width is 50 ns. Trigger source is hardware selectable; refer to paragraph 2.4.6 of the *Model 95 Operator's Manual.*

In phase lock , Trig/Freq In accepts the signal that phase locks the Model 95 to the external source. The Model 95 measures the frequency, sets the unit to match the source frequency, and phase locks the generator to the source. Model 95 phase locks range from 20 Hz to 20 MHz in the Continuous, AM or SCM modes. The input signal must be a sine wave or bipolar signal (600 mVpp to 30 Vpp).

Input impedance is 10 kΩ ± 2%.

Modulation In

Mod In, a female BNC connector, serves as the modulation input for FM (VCG), AM, and SCM. Input impedance is 10 kΩ ±2%. Bandwidth is dc to 1 MHz.

Maximum input level is ±20 Vpp (into 10 kΩ).

FM Mode: In FM an external signal provides linear control of waveform frequency around the programmed frequency. A ±10V input signal causes a 1000:1 (three decade) frequency change on the selected frequency range. An ac signal varies the frequency around the programmed frequency. A dc level shifts the generator to its new frequency. VCG bandwidth is dc to 100 kHz limited by 0.06 V/μs maximum slew rate. FM bandwidth is dc to 100 kHz deviation rate; with maximum envelope distortion of 1.78% (-35 dB). The Model 95's VCG circuit limits the bandwidth to 100 kHz. Envelope distortion is measured using 10 MHz carrier frequency, 1kHz modulation frequency and 1 MHz (10%) depth (sine wave modulation).

AM Mode: In the AM mode an external signal provides linear control of waveform amplitude around the programmed amplitude value. Displayed amplitude dependent scale factor specifies approximate Vpp (into 10kΩ) required for 100% modulation. AM bandwidth is dc to 1 MHz; with a maximum envelope distortion of 2% taken with 1MHz carrier frequency, 1 kHz modulation frequency and 70% AM (sine wave modulation).

SCM (Suppressed Carrier Modulation): In the SCM mode, an external signal linearly controls the waveform's amplitude about the zero carrier level. The Model 95 displays a scale factor (2 V/V, 0.2 V/V, or 0.02 V/V) which defines the amount of Mod In signal level to produce a SCM output level. SCM bandwidth is dc to 1 MHz. Maximum envelope distortion is 2% (1 MHz carrier and 1 kHz modulation).

A.2.8 Display

The Model 95 contains a 16 digit, Vacuum Florescent Display (VFD) with 14 segment, alphanumeric characters and 11 mm character height. The display shows all selectable parameters, parameter name, numeric value and the unit of measure. In addition, the display shows GPIB messages, various utilities, maintenance, and diagnostic information.

A.2.9 GPIB Programming

Address

The Model 95 accepts GPIB addresses of 0 to 30 (default is 9). Addresses are front panel selectable and retained in battery backed memory.

Subsets

SH1, AH1, SR1, RL1, PP0, DC1, DT0, C0, T6, L4, TE0, LE0 and E1.

A.2.10 Arbitrary Waveform Generator

The Model 95's Arbitrary Waveform Generator (Arb) allows the user to create and store up to four unique waveforms. The Model 95 transfers the selected Arb waveform from storage RAM to the active RAM. The storage RAM contains four waveform blocks of up to 8K points with start and stop addresses, sync position and a Z-Axis marker. The Model 95 samples the Arb waveform in the active RAM using a clock derived from the function generator's frequency/period. The waveform may be from 2 samples to the full 8K samples in width. The RAM's battery allows the Model 95 to retain waveforms with the power off. The unit accepts Arb waveforms via the GPIB which the unit stores in its active RAM. These waveforms can be edited and stored in memory.

Horizontal Resolution: 2 words to 8K words per waveform for each of four waveforms.

Vertical Resolution: 12 bits (4096 points)

Analog Filter: Two pole active Bessel filter, programmable as no filter, 5MHz corner, and 50 kHz corner.

Digital Filter: A smoothing function that acts like a single pole, low pass filter which alters waveform data. Eight filter weights adjust the smoothing algorithm. The Model 95 displays the equivalent bandwidth.

Flatness: ±0.5 dB referenced to 1 kHz sample waveform. Waveform: 10 point 2 MHz sine wave (20 MHz sample frequency), no filter or the 5 MHz cut-off filter .

Transition Times: <20 ns for a full amplitude step (no filter programmed).

Editing: The Model 95 offers four methods of editing the Arb waveforms: point, line, three-point, and block.

Point editing allows the user to change a single point without affecting the other points.

Line editing allows the user to "draw a line" between two user-defined points (address/data). The Model 95 erases all previous data between the points.

Three-point allow the user to pick a point between left and right cursors and alter the waveform by "pulling" the point around.

Block edits allow the user to place a "standard" waveform (dc, triangle, square, ramp up, and ramp down, sine, cosine, inverse sine, and inverse cosine) between left and right cursors. Use any of the other edit methods to change the block waveform. In block edit mode, the amplitude and offset keys change the relative amplitude and offset. Also in the block edit mode, the Model 95 allows inversion of the selected part of the waveform.

Arb Sync: Sync Out (TTL) pulse marks a position within the Arb waveform block The Sync Address key selects the sync address. The Model 95 stores the sync address with the Arb waveform.

Z-Axis Out: Z-Axis Out, a rear panel BNC connector, provides a Z-Axis (intensity) output during Arb editing. The Model 95 allows selection of Z-Axis characteristics to match the scope's Z-Axis input: 100 mVpp to 4 Vp (50Ω termination) positive pulse with selectable polarity (logic sense).

Trigger, Gate, and Burst of the Arb Waveform: Arb waveforms can be triggered, gated, and burst the same as the function generator. A single cycle of the Arb waveform is the time between the start and stop addresses.

A.3 OPTIONS

001: Frequency Reference — This option improves the accuracy and stability of the Model 95's reference oscillator. This option consists of an adjustable crystal (TCXO) with a ±1 ppm performance over the operating temperature range. The Option 001 also includes an external reference input connector and reference output connector. The reference input accepts a 10 MHz, TTL or Bipolar signal which overrides the internal reference. The reference output supplies10 MHz, TTL pulses which can drive a 50Ω termination.

002: Extended Arb RAM — This option expands the Arb waveform RAM. It increases the active RAM from 8K to 32K. This option also enlarges the storage RAM.

003: Handles and Rack Adapter — This option consists of a pair of handles and rack adapters. Rack adapters allow mounting of the Model 95 in a standard 19 inch rack.

004: Extended Cards – This option supplies a set of extender cards which provide access to the daughter boards during maintenance.

Recommended Spare Parts - A recommended spare parts package for the Model 95 can be obtained from Wavetek by ordering Wavetek part number 1200-00-3463.

A.4 GENERAL

A.4.1 Physical Specifications

Dimensions

35.6 cm (14.in.) wide, 13.3 cm (5.219 in.) high and 43.2 cm (17 in.) deep.

Weight

About 7.7 kg (17 lb.) net; 11.8 kg (26 lb.) shipping.

Power

90 to 108, 108 to 126, 198 to 231, or 216 to 252 Vrms; 48 to 440 Hz; 1 phase; <110 VA.

A.4.2 Environmental Specifications

The Model 95 conforms to MIL-T-28800C, class 5.

Temperature Range

0°C to +50°C for operation;
–40°C to +70°C for storage.

Warm Up Time

Allow 20 minutes for specified operation at temperature of last Auto Cal ±10°C. Auto Cal should be performed when the ambient temperature has changed.

Operational Humidity

11°C to 30°C at 95% relative humidity;
31°C to 40°C at 75% relative humidity;
41°C to 50°C at 45% relative humidity.

Altitude

To 10,000 ft. (3050m.) for operation;
To 15,000 ft. (4570m.) for non-operating.

Vibration (Operating)

Vibration level of 0.013 in. from 5 to 55 Hz (2g acceleration at 55 Hz.).

Shock (Non-operating)

40g, 9 ms half-sine wave.

Bench Handling (Operating)

4 in. or point of balance drop, any face, solid wooden surface.

Electromagnetic Compatibility

The Model 95 has been tested to MIL-STD-461A Notice 4 (EL) and meets the emission and susceptibility requirements of CE02, CE04, CS02, CS06, RE02, RE02.1, and RS03.

APPENDIX B
PHASE CALIBRATION

PHASE CALIBRATION USING AN OSCILLOSCOPE

This procedure provides an alternate method of Model 95 phase calibration. Simply use the following steps in place of Steps 16, 17, 18, and 19 of the calibration procedure (section 4).

Step 16 Adjust Phase 0°

1. The Model 95 displays PHASE 0 XXXXX where XXXXX represents a calibration value. Connect the test equipment as shown in figure B-1.

2. Set the signal source controls as follows:
   Set Function to Sine.
   Frequency to 2.01 kHz.
   Output Level to 5Vpp.

3. Set the scope controls as follows:
   Trigger to channel 1.
   Adjust Channel 1 and 2 gain and offset controls so identical superimposed wave forms are displayed.
   Select channel 2 Invert.
   Select 1 and 2 Add.

4. On the Model 95,
   Adjust the Knob to null the waveform on the scope.
   Press the TRIG FREQ key. Verify that the display flashes CALIBRATING for then displays PHASE +180 XXXXX. Pressing TRIG FREQ key stores the calibration value in internal memory.

Step 17 Adjust Phase +180°

1. The Model 95 displays PHASE +180 XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure B-1. Do not change the signal source.

2. Set the scope controls as follows:
   If necessary, adjust Channel 1 and 2 gain and offset controls so identical superimposed waveforms are displayed.

3. On the Model 95,
   Adjust the Knob to null (minimum displayed signal) the added waveform on the scope display.
   Press the TRIG FREQ key advance to the next step. Verify the display flashes CALBRATING and then displays PHASE – 180 Y XXXXX. Pressing TRIG FREQ key stores the calibration value in internal memory.

Step 18 Adjust Phase -180°

1. The Model 95 displays PHASE -180 XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown

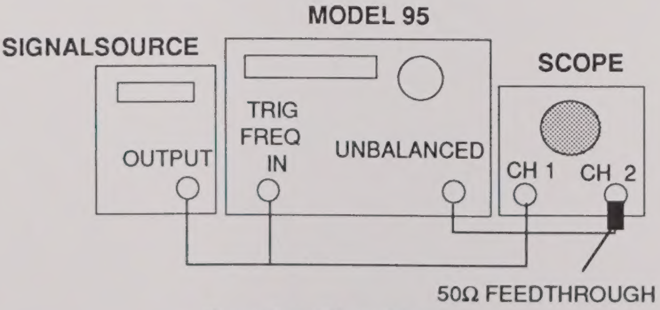

Figure B-1. Phase Setup

in figure B-1. Do not change the signal source. The scope should not need adjustment.

2. On the Model 95,

   Adjust the Knob to null (minimum displayed signal) the waveform on the scope display. Press TRIG FREQ key to advance to the next step. Verify that the display flashes CALIBRATING and then displays SQ PHASE 0 XXXXX. Pressing TRIG FREQ key stores the calibration value in internal memory.

Step 19 Adjust Square Phase 0°

1. The Model 95 displays SQ PHASE 0 XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure B-1. Do not change the signal source.

2. Set the scope controls as follows:

   Turn off Add.

   Observe the sine wave reference on channel 1. Trigger on channel 1.

   Observe the square wave on channel 2.

   Superimpose the sine over the square wave.

   Increase the gain of channel 1 (sine) by 10.

   Using the scope's controls, adjust channel 1 for 0Vdc offset.

   Using the scope's horizontal time and trigger slope, set the negative-going zero crossing of the sine wave and square wave to occur at the center of the graticule. Magnify the center of the display by X10.

3. On the Model 95,

   Adjust the Knob to null so the square's transition passes through the sine's zero crossing point.

4. Set the scope as follows:

   Change the trigger slope to display the positive-going transition. If an error exists, split the difference between the two slopes using the Model 95s knob.

5. On the Model 95,

   Press the TRIG FREQ key to advance to the next step. Verify the display flashes CALIBRATING and then displays CONFIDENCE. Pressing TRIG FREQ key stores the calibration value in internal memory.

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